Radiation Effects on Current Field Programmable Technologies

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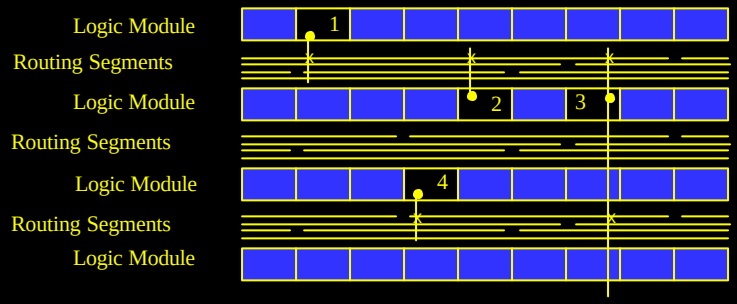
Summary

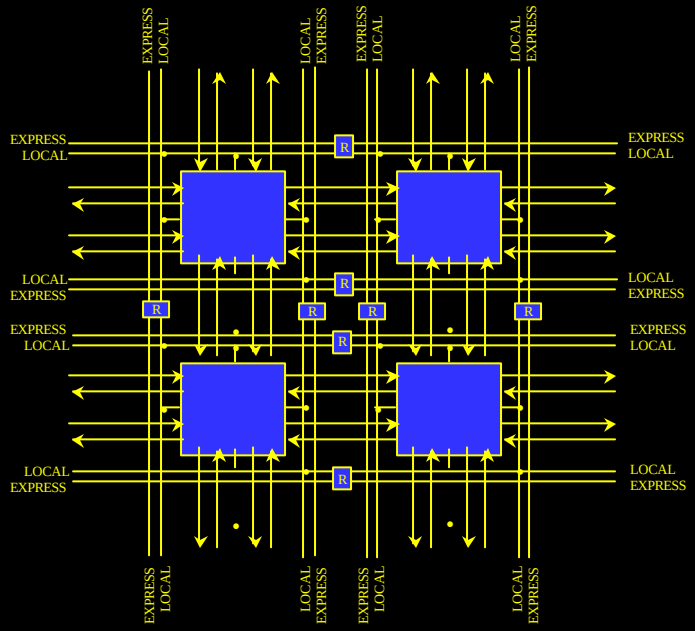
I. Scope of Presentation
II. Device Categories
III. Radiation Performance
    A. Configuration Technologies
    B. Fabrication Considerations
    C. Design
    D. Architectural Features
IV. Conclusion

Basic Architecture

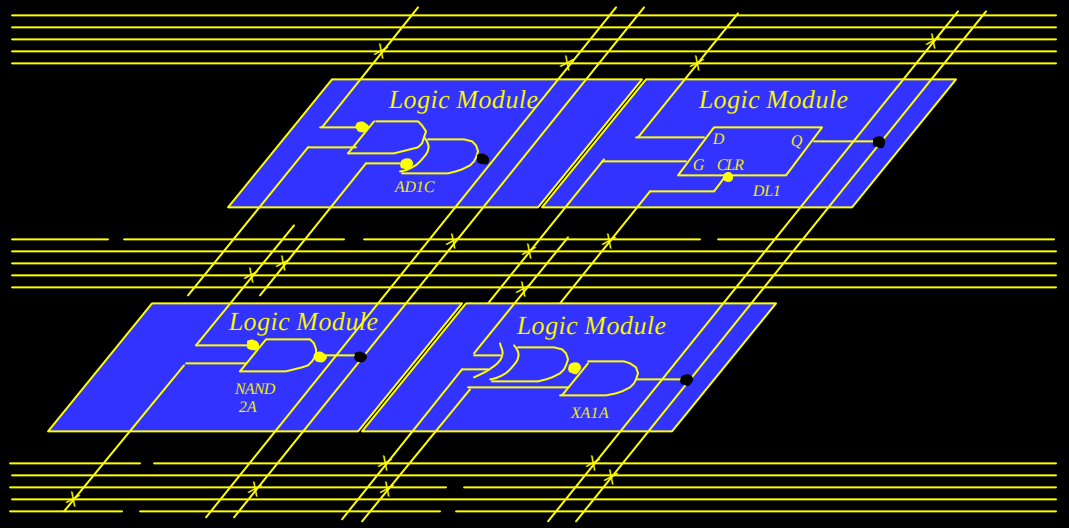


Channeled FPGA Architecture

A Sea of Gates Architecture
Has the Routing Network
Above The Logic Array



Atmel Architecture - Lowest Level

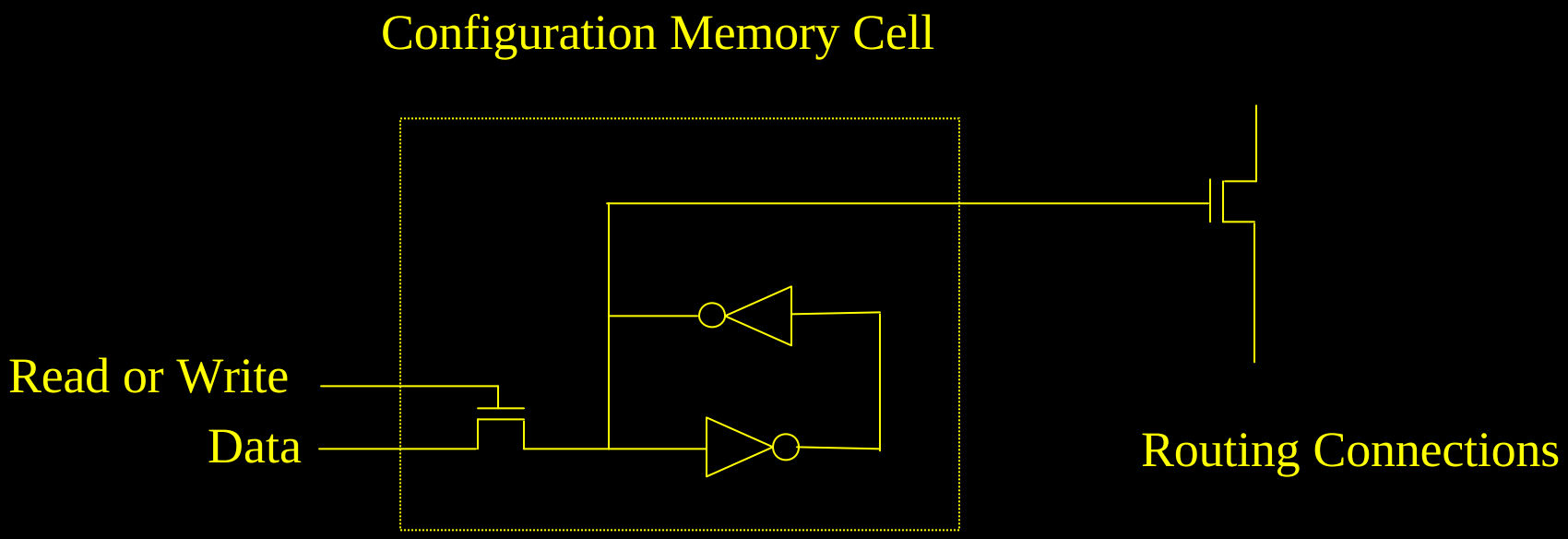


Actel Architecture

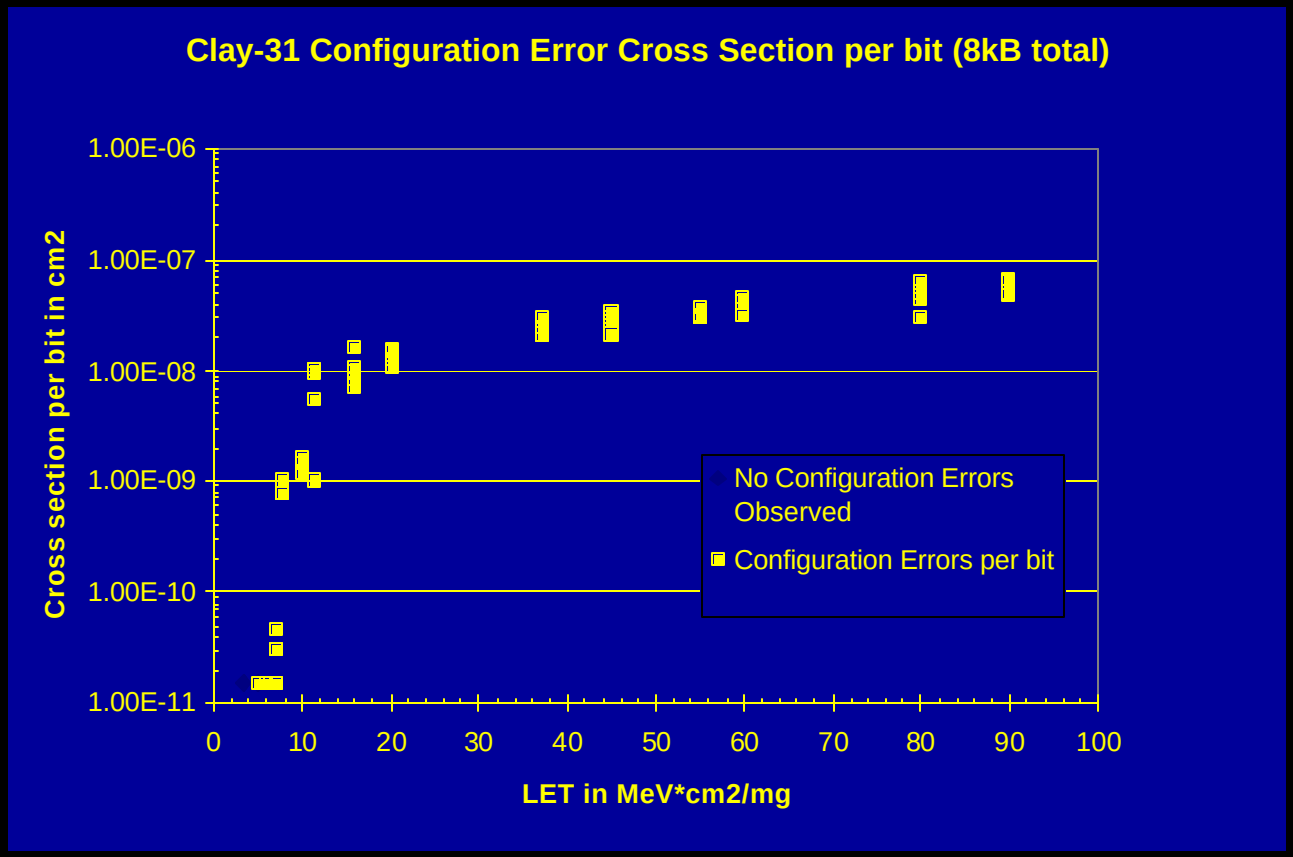
Device Categories

- Programmable Substrate
- PLD/CPLD
- Field Programmable Gate Arrays
  - SRAM
  - Non-Volatile
  - Antifuse
    - Amorphous Silicon
    - Dielectric
- LPGA/One-Mask
- Mask-Programmed ASIC

SRAM Switch Technology



SER - Single Event Reprogramming



SER Cross Section detected by function failure.
This curve serves as a lower bound.

FPGA Configuration Memory

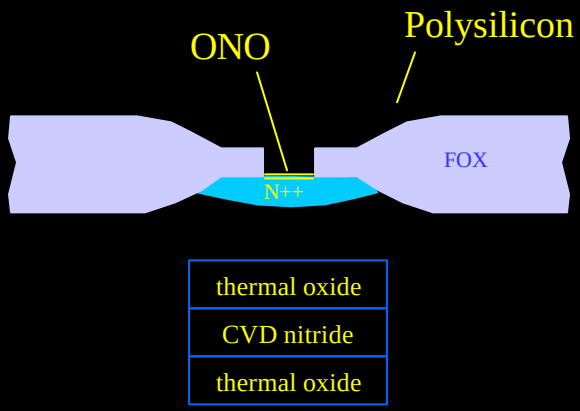
A14100A	905 ← Hardwired Off (MODE PIN)
AT6010	131,000
XC4020	329,000
XC6216	173,000
2C26	274,000

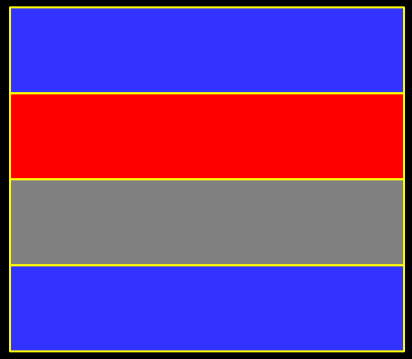
- This Device Class Typically Has 1-2,000 User Flip-Flops
- Configuration Memory Increases SEU Cross Section
  By ~ 2 Orders of Magnitude

Antifuse Radiation Effects

- Unprogrammed Reliability is the Key Concern
  - Both Dielectric and Amorphous Silicon Can be Damaged
- Manufacturers: Actel, L-M, Pico Systems, Quick Logic, UTMC
- Circuits and Instrumentation Techniques for Characterization
- Investigated Failure Thresholds and Cross Sections
  - Improvements in Antifuse Design
  - Effects of Materials
- Failure Analysis Techniques and Results

Switch Technology





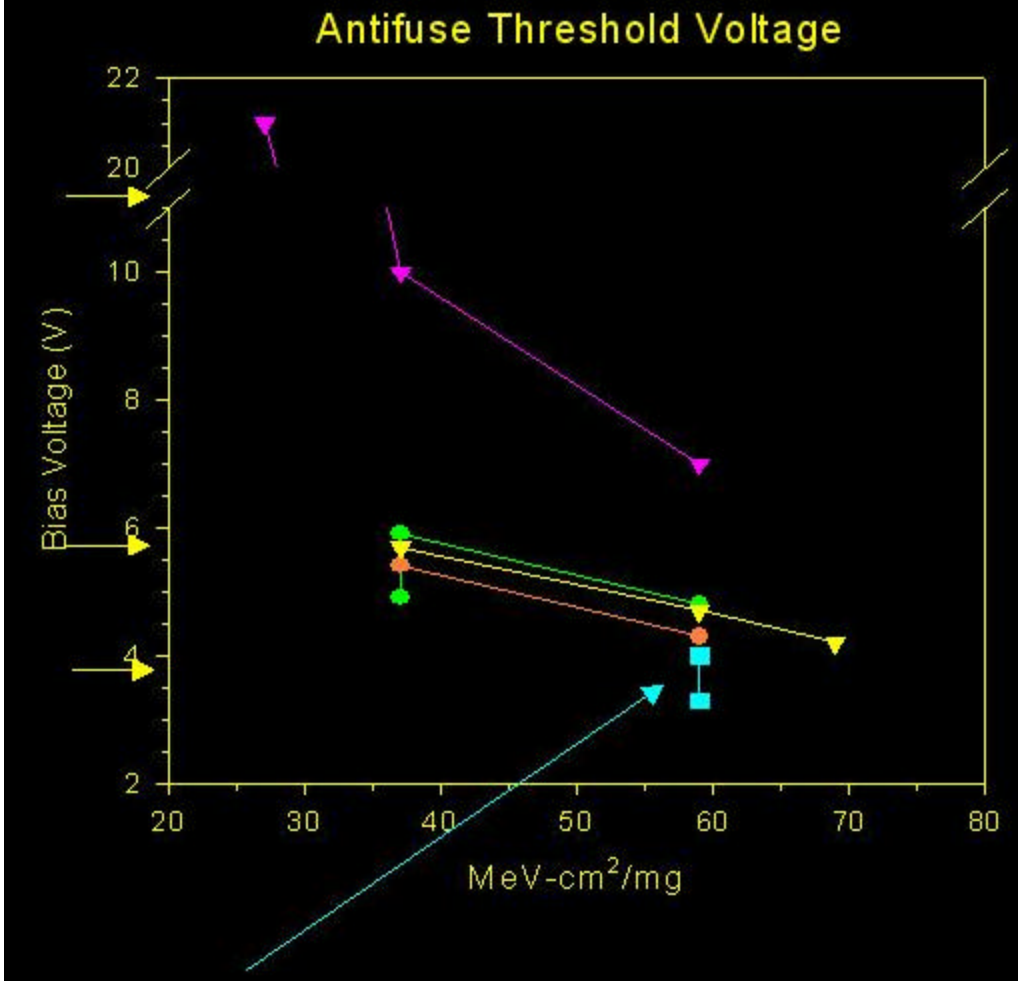
Metal - 3 Top Electrode
Amorphous Silicon
Dielectric
Metal - 2 Bottom Electrode

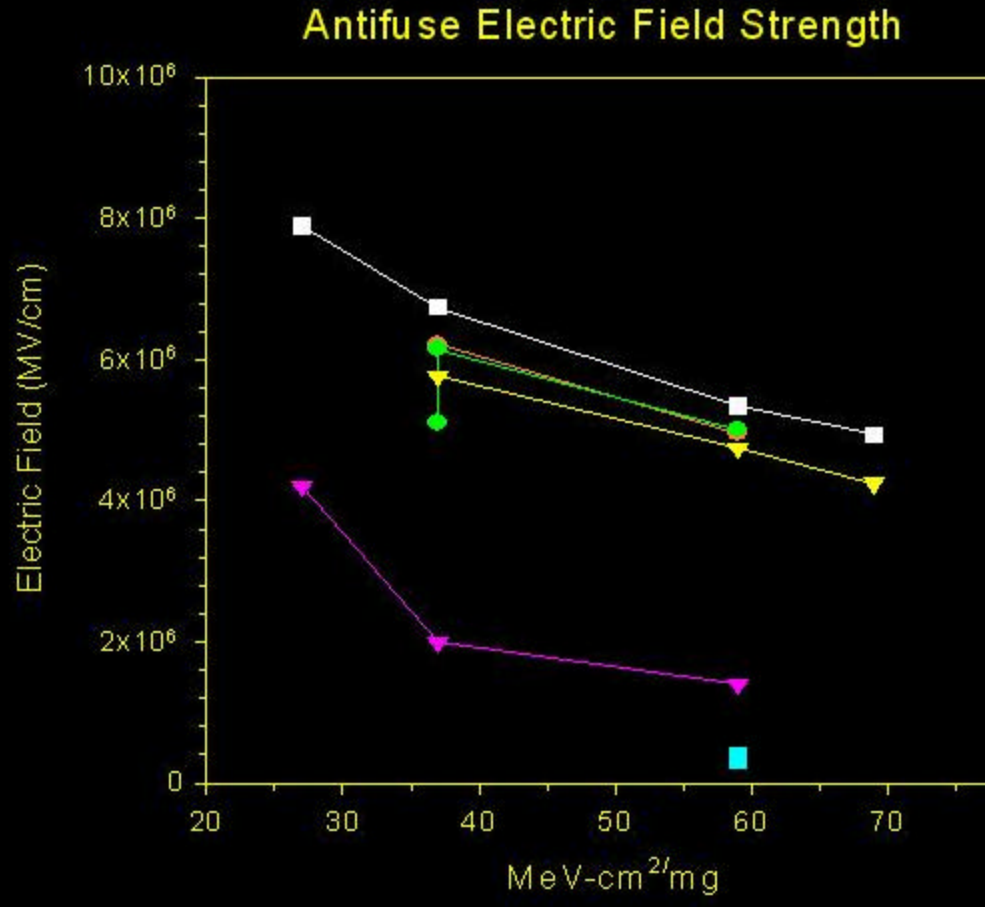
ONO Antifuse
Poly/ONO/N++
Heavy as doped Poly/N++
Thickness controlled by
CVD nitride
Programs ~ 18V
Typical Toxono ~ 85 Å
RH1280 Toxono = 99 Å
R = 200 - 500 ohms

TD Amorphous Silicon Antifuse
'Pancake' Stack Between Metal 2 and 3
Designed for 3.6V Operation in Sea Of Gates FPGA

'Logic' Devices Program at ~ 10V
'Substrate' Devices Program at ~ 30V
Thickness ~ 500 - 1000 Å
R = 20 - 100 ohms

Antifuse Failure Thresholds

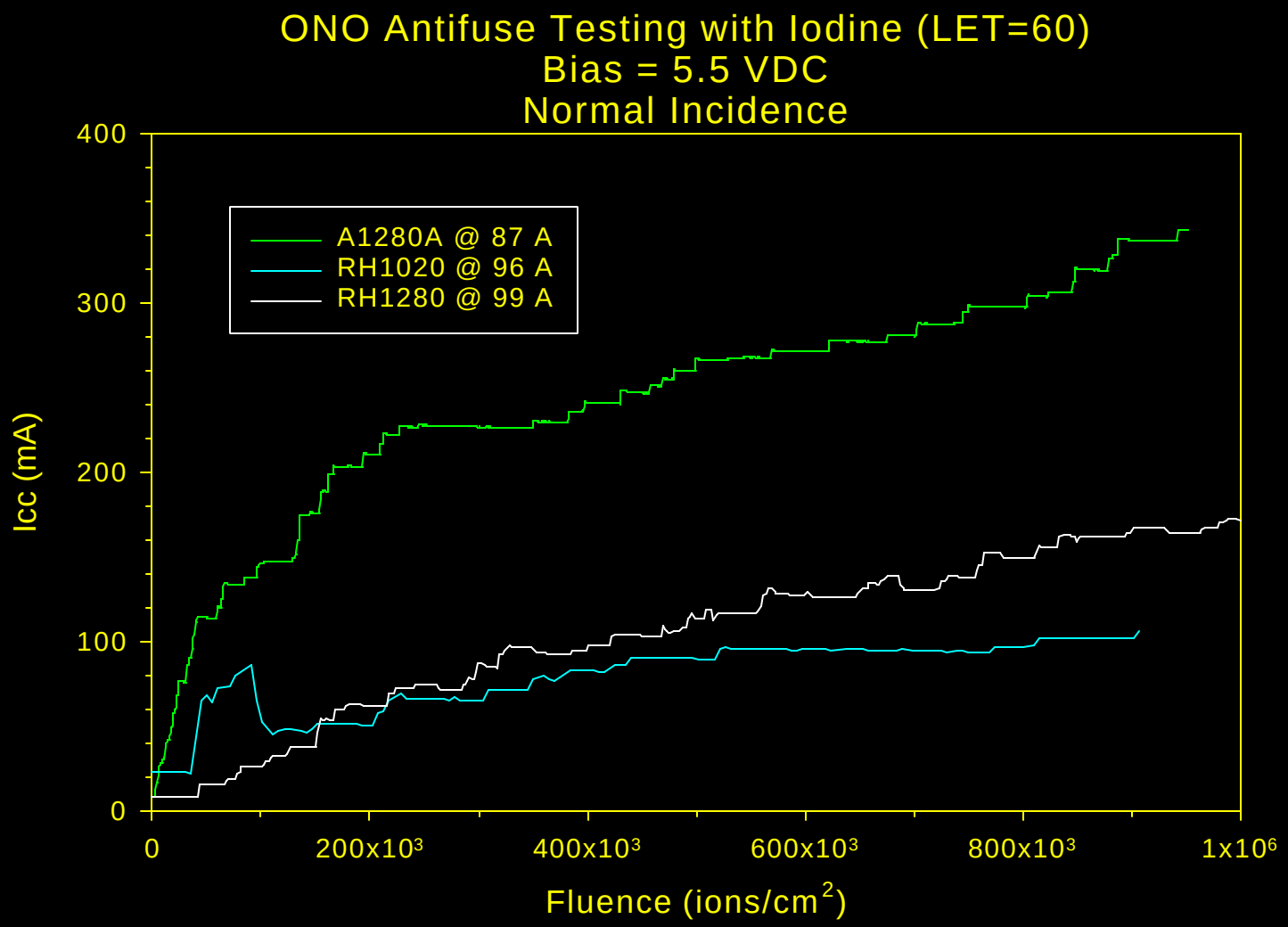




Two processes were used for this 3.3 V device
Process 1 failed immediately @ 3.3 VDC
Process 2 didn't fail @ 4.0 VDC

- A1280A (87 A)
- RH1020 (96A)
- RH1280 (99A)
- Pico-amorphous (500A)
- TD-amorphous (1000A)
- SiO_2 - reference

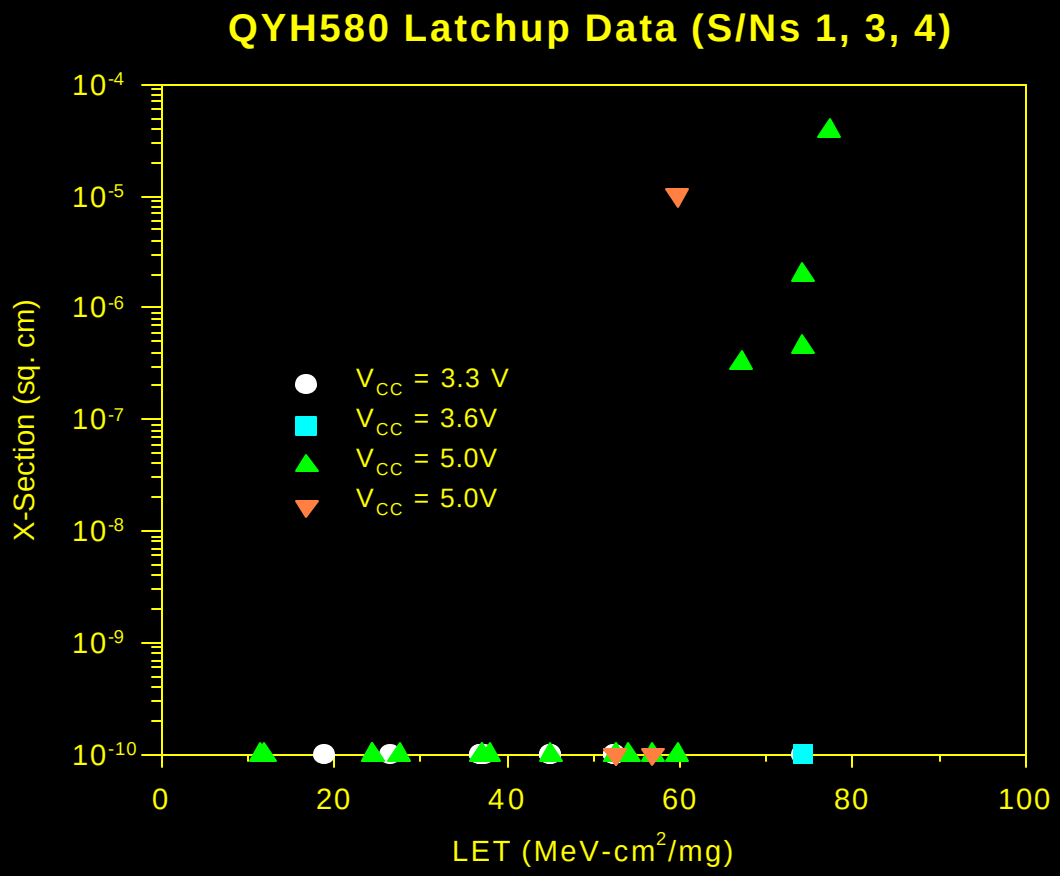
Dielectric Antifuse Cross Sections



Latchup Performance

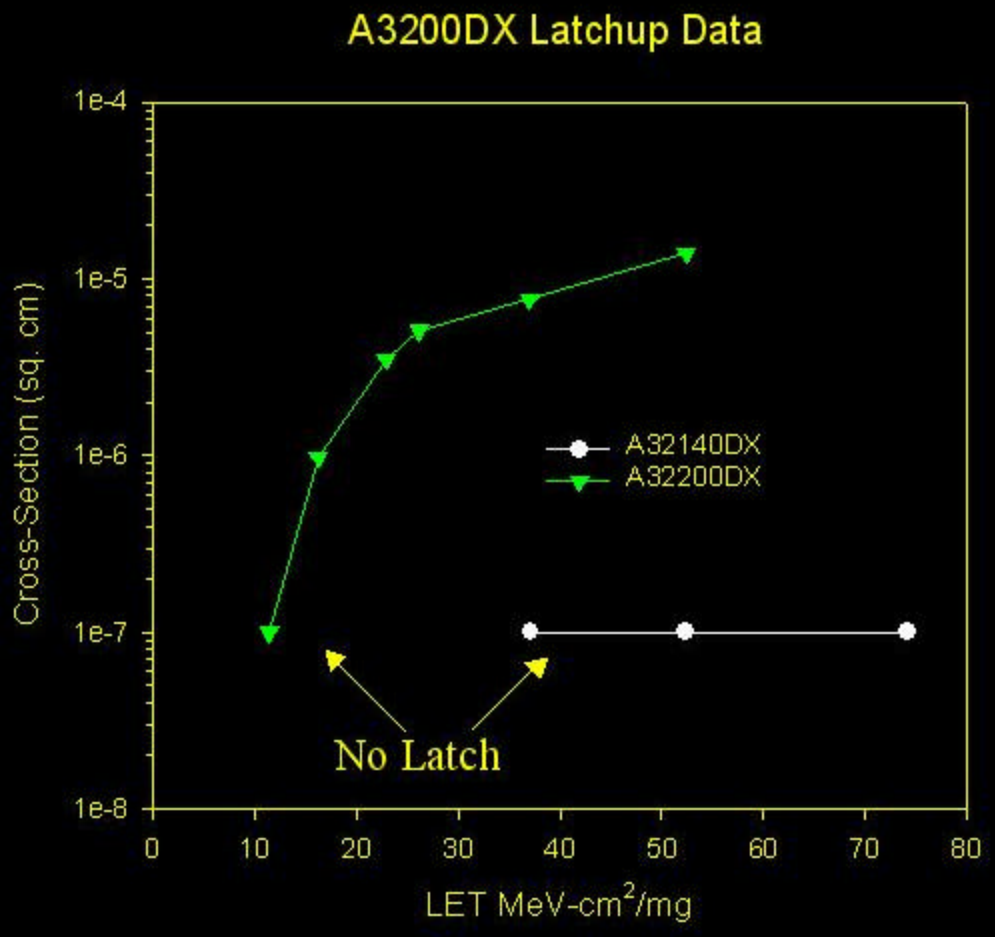
Latched		Not Latched
A1020B/TI	~ 22	RH1020
A1020B/MEC	27-37	A1280XL (0.6, 0.8)
A32200DX	11-16	A32140DX
AT6002	~ 11	A1460A, A14100A
QYH580 @ 5.5V	~ 60	QYH580 @ 3.6V
GF10009K	< 12	CLAy-31
2C40	< 7.8	KJ911
pASIC 1	< 60	MKJ911
XC3090	4-7	

Latchup Susceptibilities - Bulk



- 0.8 um Bulk Process
- High Latchup Threshold @ 5.0 V
- No Latchup Detected @ 3.6 V

Latchup Susceptibilities - EPI



A32200DX Readily Latches
A32140DX No Latchup

0.6 um Epi Process
Epi Thickness: 8.5 - 9.0 um
For Two Lots Tested

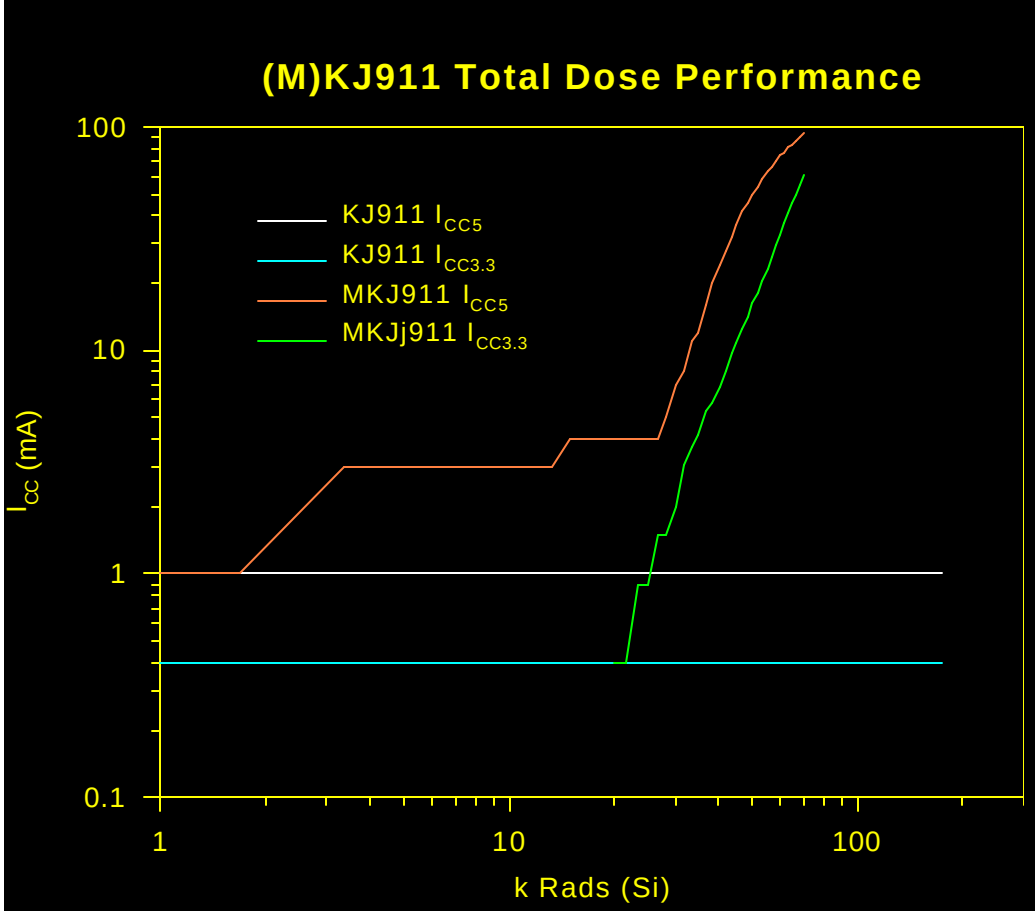
A32200DX: SRAM
A32140DX: No SRAM
SRAM Structure Lacks
Guard Rings

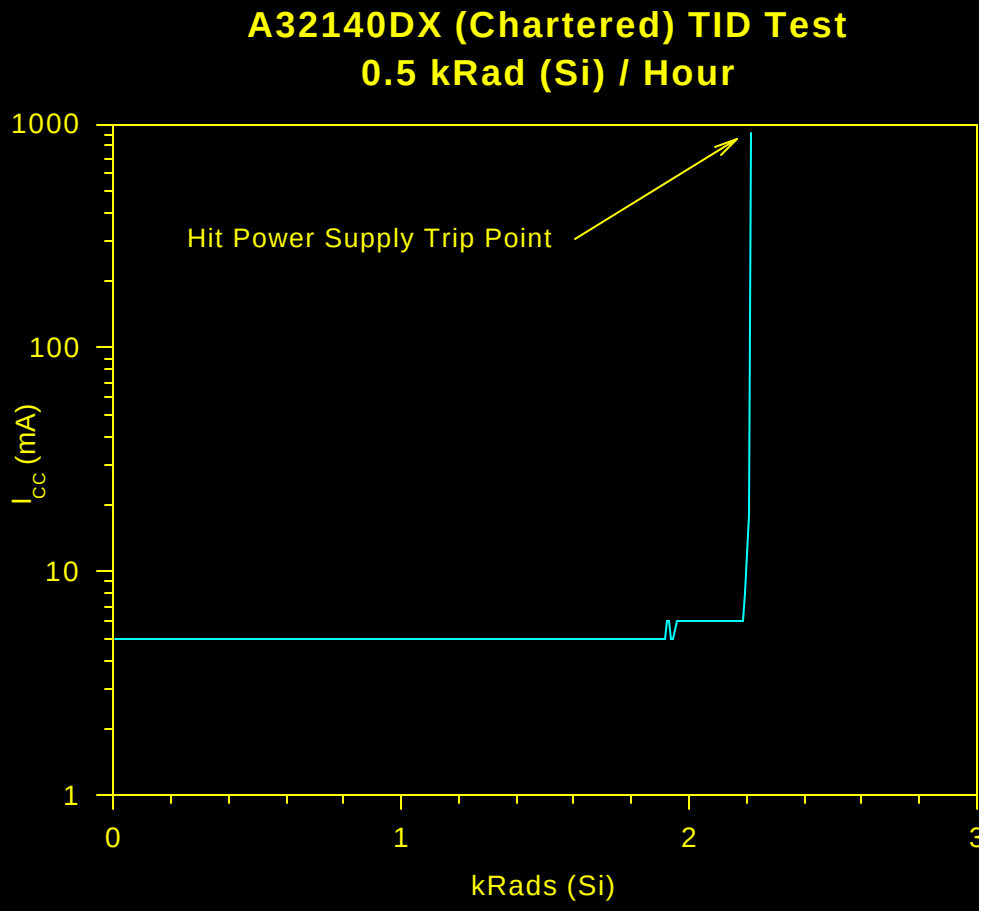
Total Dose Performance

Recent Device Capability in kRads (Si)		
A1280A	1.0 ?m (MEC)	~ 7
A1280XL	0.8 ?m (WIN)	< 3
RH1280	0.8 ?m (L-M)	> 300
A1280XL	0.6 ?m (CH)	< 3
Act 3	0.8 ?m (MEC)	15-50+
Act 3	0.8 ?m (WIN)	< 5
A32140DX	0.6 ?m (CH)	< 3
MKJ911	0.6 ?m (MEC)	30-50
KJ911	0.6 ?m (L-M)	> 200
QYH580	0.8 ?m (CHIPX)	~ 15

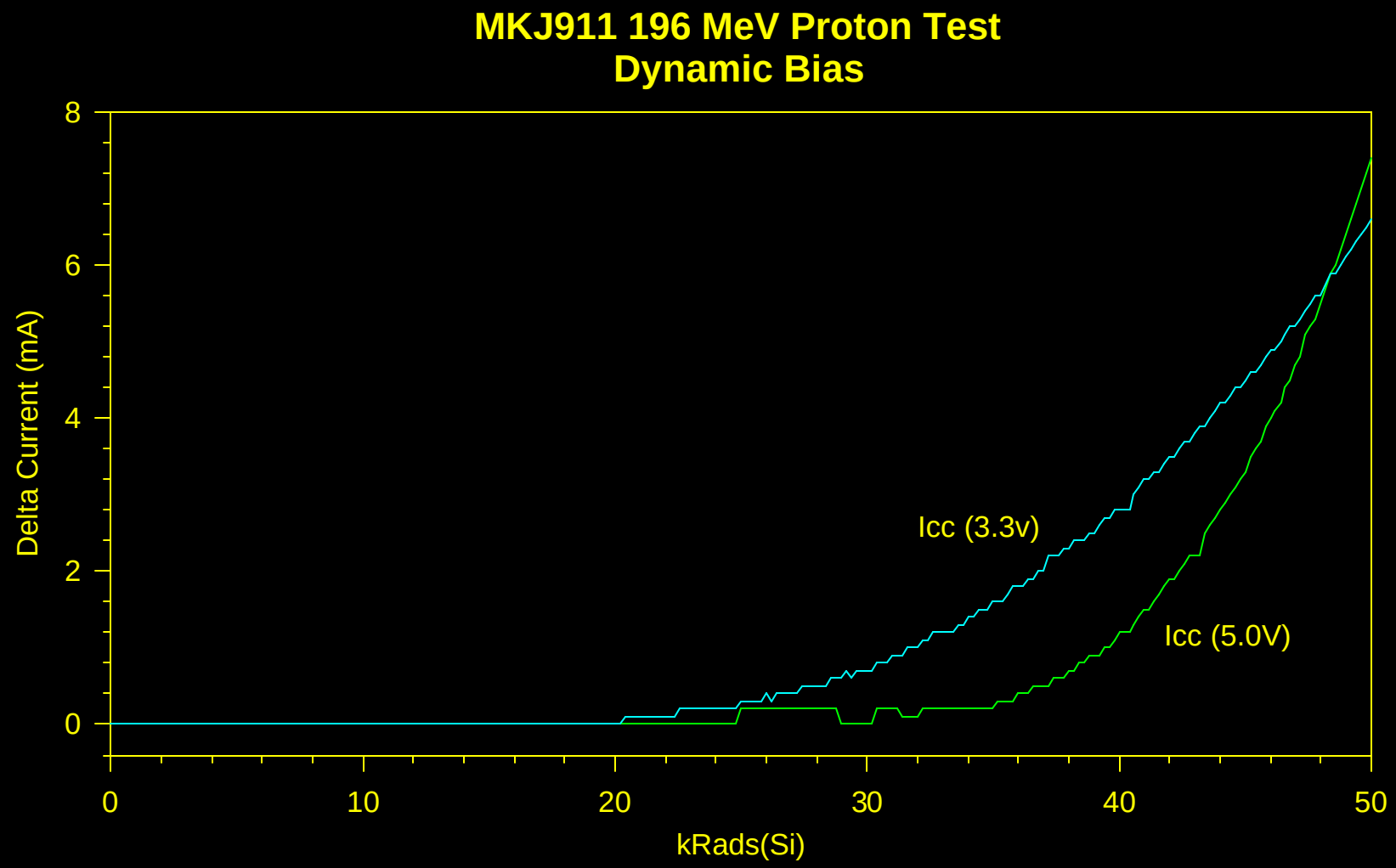
- Act 1, Act 2 Data
- Testing with Protons
- Charge Pump Investigation
  - Internal Measurements
- Design vs. Process
  - A1020Z

TID: Recent Devices





Proton Test: Recent Devices

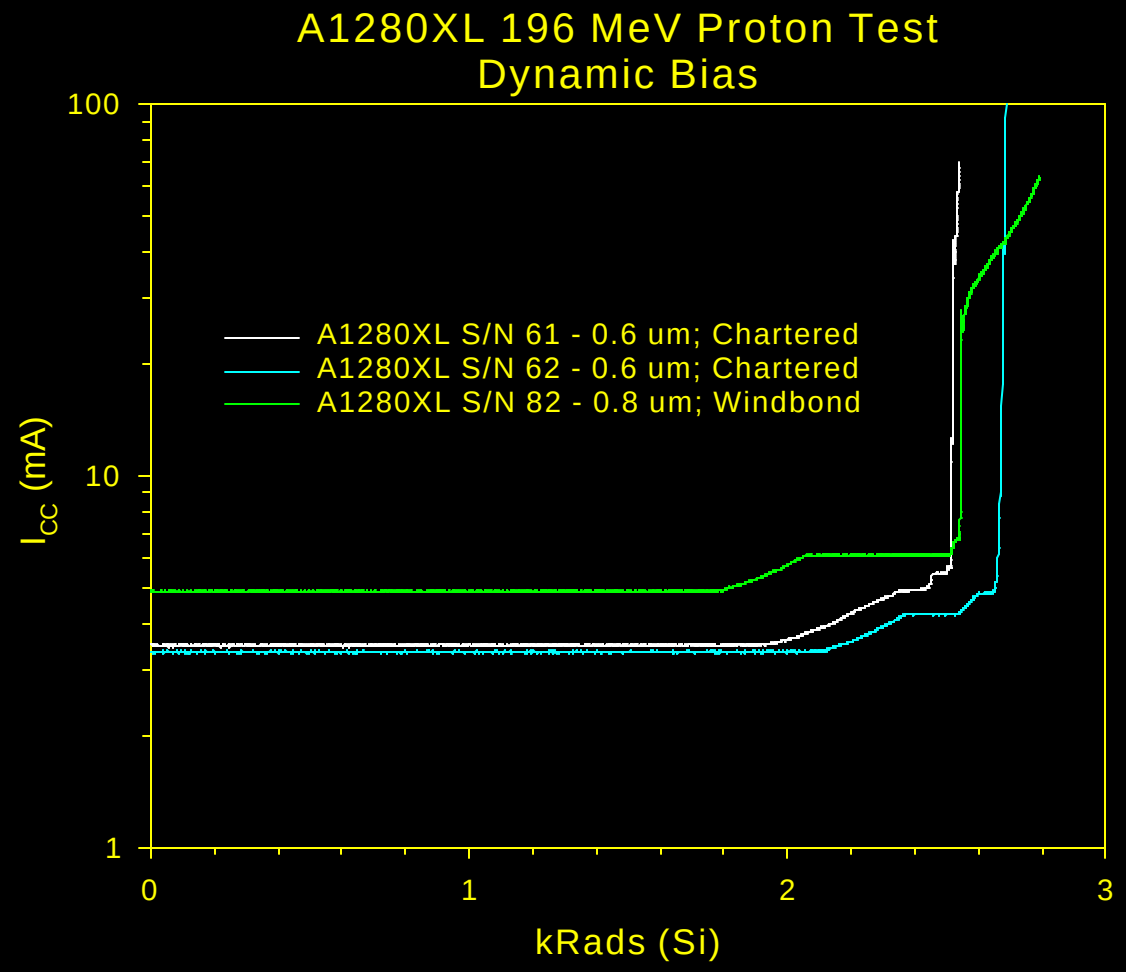


Total Fluence = 810 x 10^9 protons/cm^2

Zero upsets over the course of the test.

rbk 11/21/96

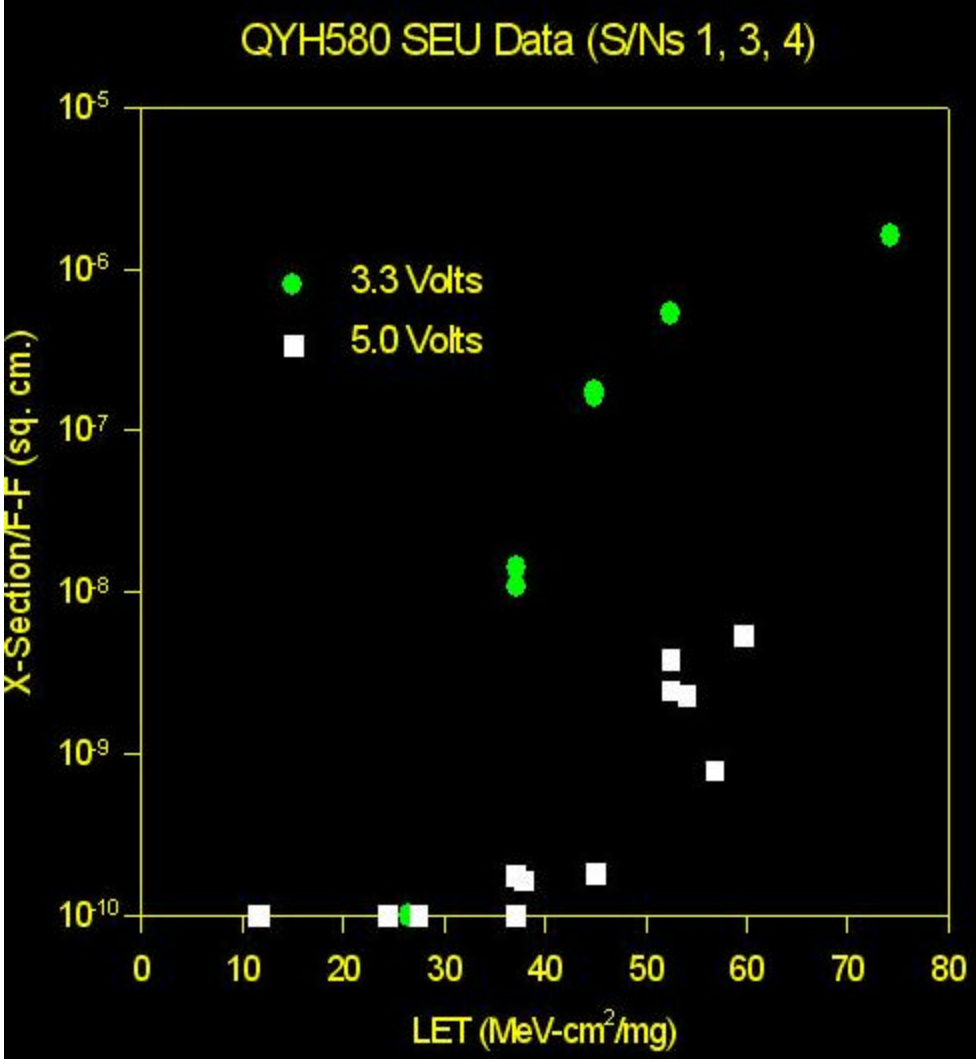
Proton Test: Recent Devices

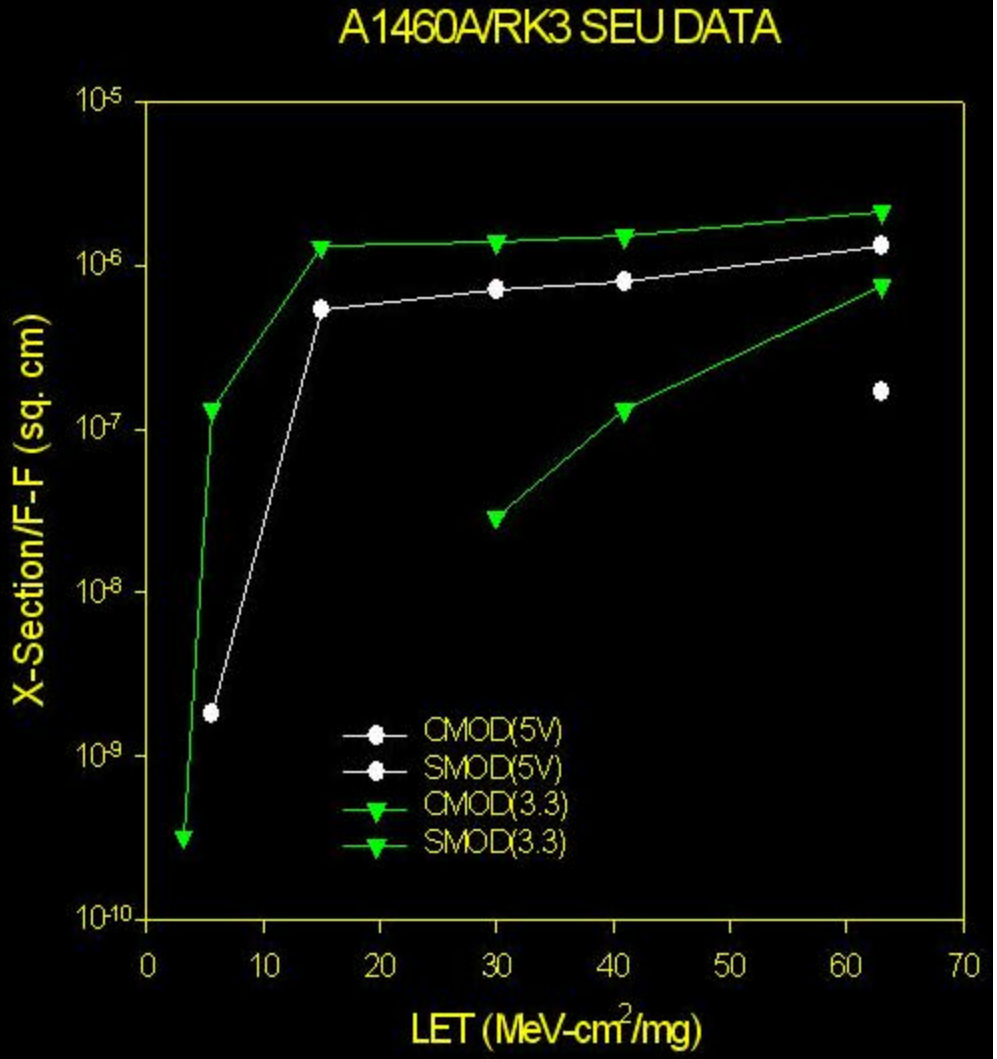


Sensitivity to Protons

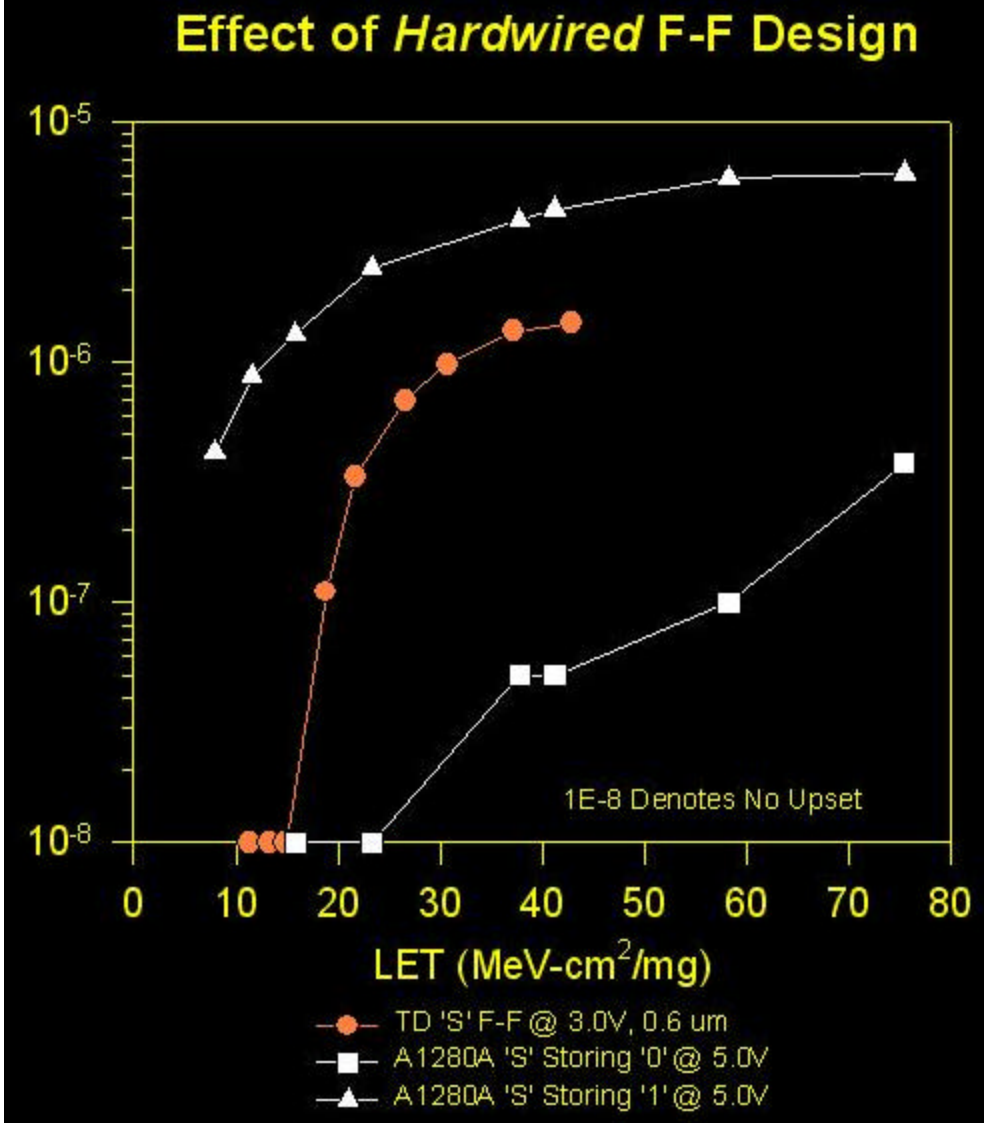
Upset	Likely To Upset	No Upset
A1280XL ‘S’ (0.6, 0.8)		A1280XL ‘C’, I/O
RH1280 ‘S’ (0.8)		RH1280 ‘C’, I/O
		A1280 (1.2 um)
		A1280A (1.0 um)
A1460A ‘S’, I/O (0.8)	Act 3 ‘S’, I/O (0.6)	A1460A ‘C’ (0.8)
A14100A ‘S’, I/O (0.8)		A14100A ‘C’ (0.8)
CLAy-31 (0.8)	XC3090 (0.65)	MKJ911 (0.6 um)
AT6002 (data) (0.8)	- LET_{TH} ~ 4-7	
	2C04 (config)	QYH500 3.3, 5.0V (0.8)
	- LET_{TH} < 7.9	- high LET_{TH}

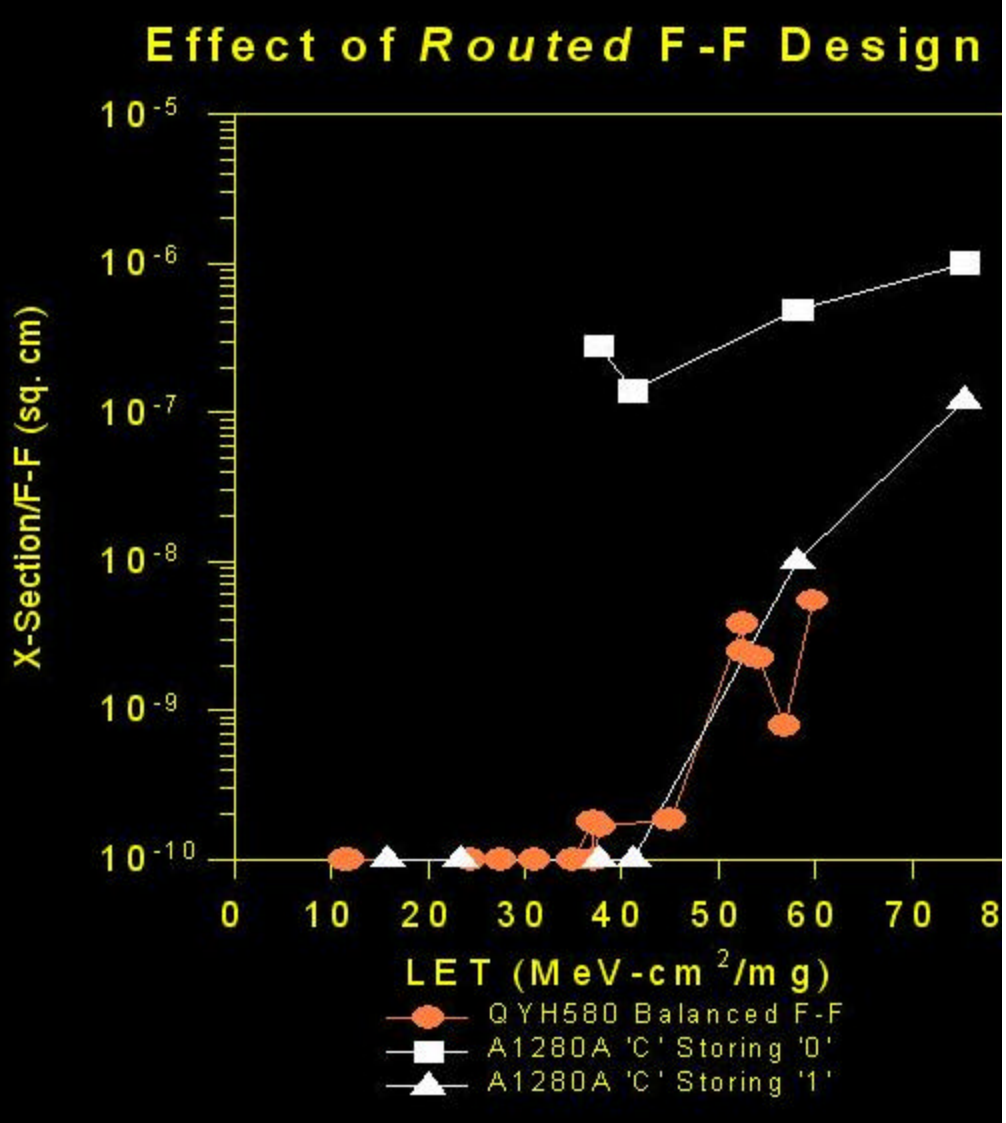
SEU: 5V vs. 3.3V Performance





Flip-Flop Design

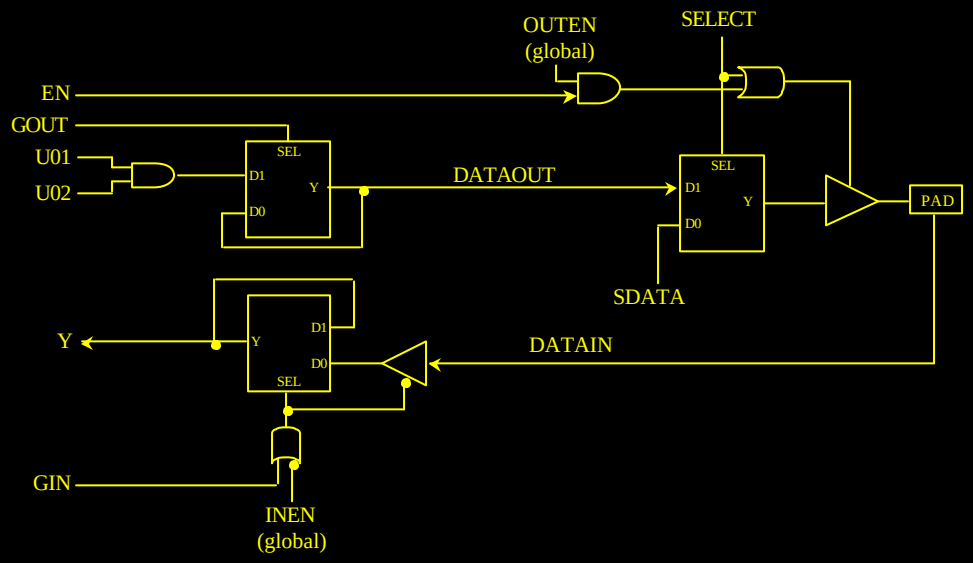




Architectural Features

- Configuration Storage Technology
  - ‘Soft’ SRAM Requires Monitor & System Protection
    - Input pin ? Output Pin
    - Internal Driver Fights (Routing, Tri-State Bus)
    - State of the Device: i.e., Programmed, POR
- Higher Complexity Structures
  - I/O Modules
  - XC6216: Bit Controls Clock On/Off
- DFT/IEEE JTAG 1149.1 Boundary Scan
  - State Machine Controls Mode of Device
  - Potential For Failure/Damage Modes
  - Hard Reset **Should** Be Implemented

I/O Module Architectures



Act 2 Input/Output Block

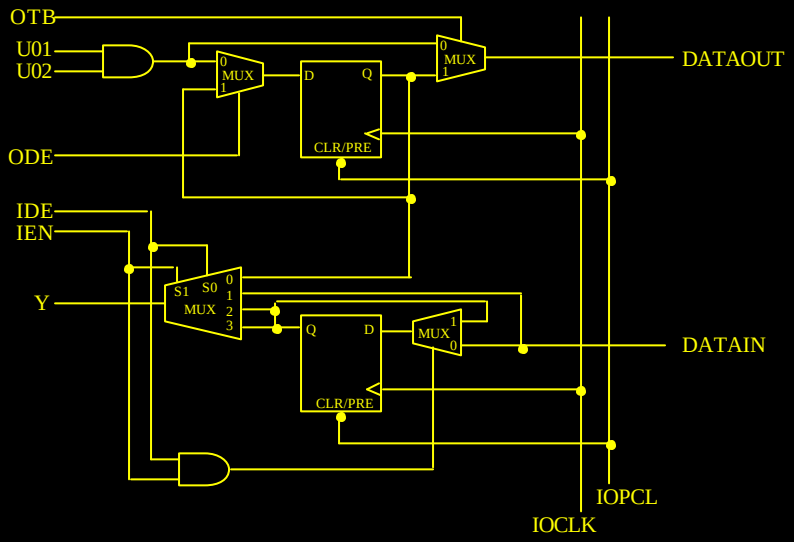
Act 1: No Storage

Act 2 Latch: LET_{TH} ~ 20's

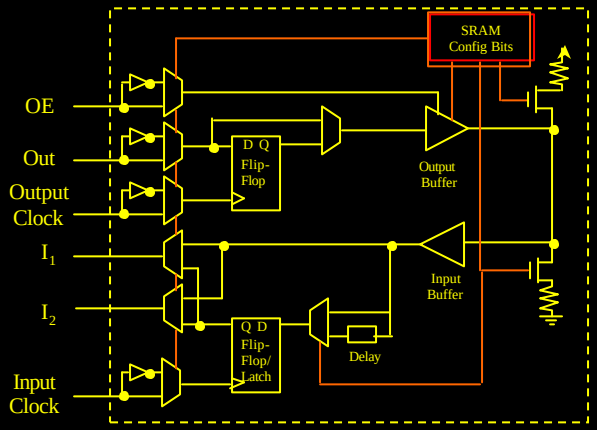
Act 3 Reg: LET_{TH} ~ 10

XC4000 (SRAM config)

- input or output
- pullup/pulldown
- slew-rate control
- input delay
- etc
- LET ~ 4-7

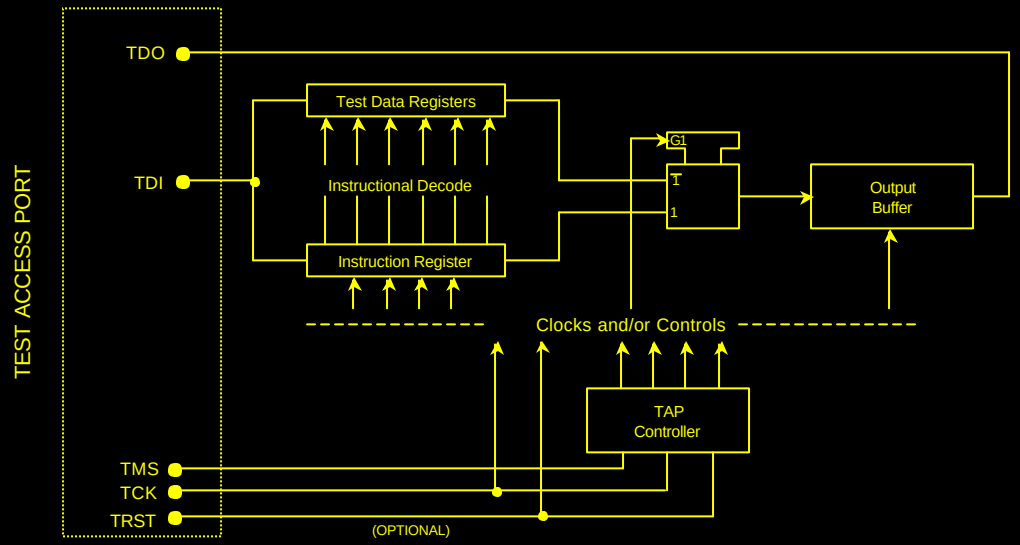


Act 3 Input/Output Block

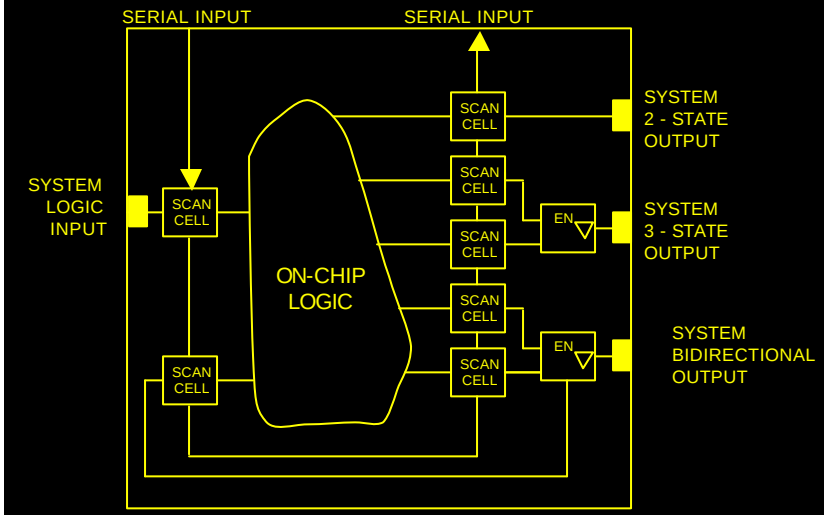


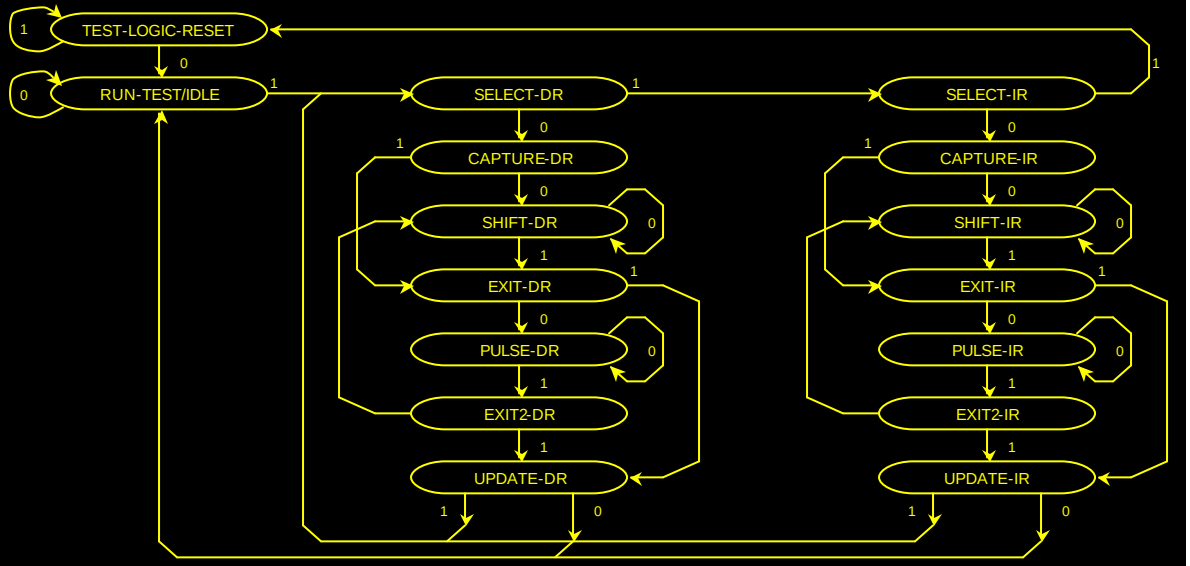
XC4000 and XC4000A Families
Input/Output Block

IEEE JTAG 1149.1

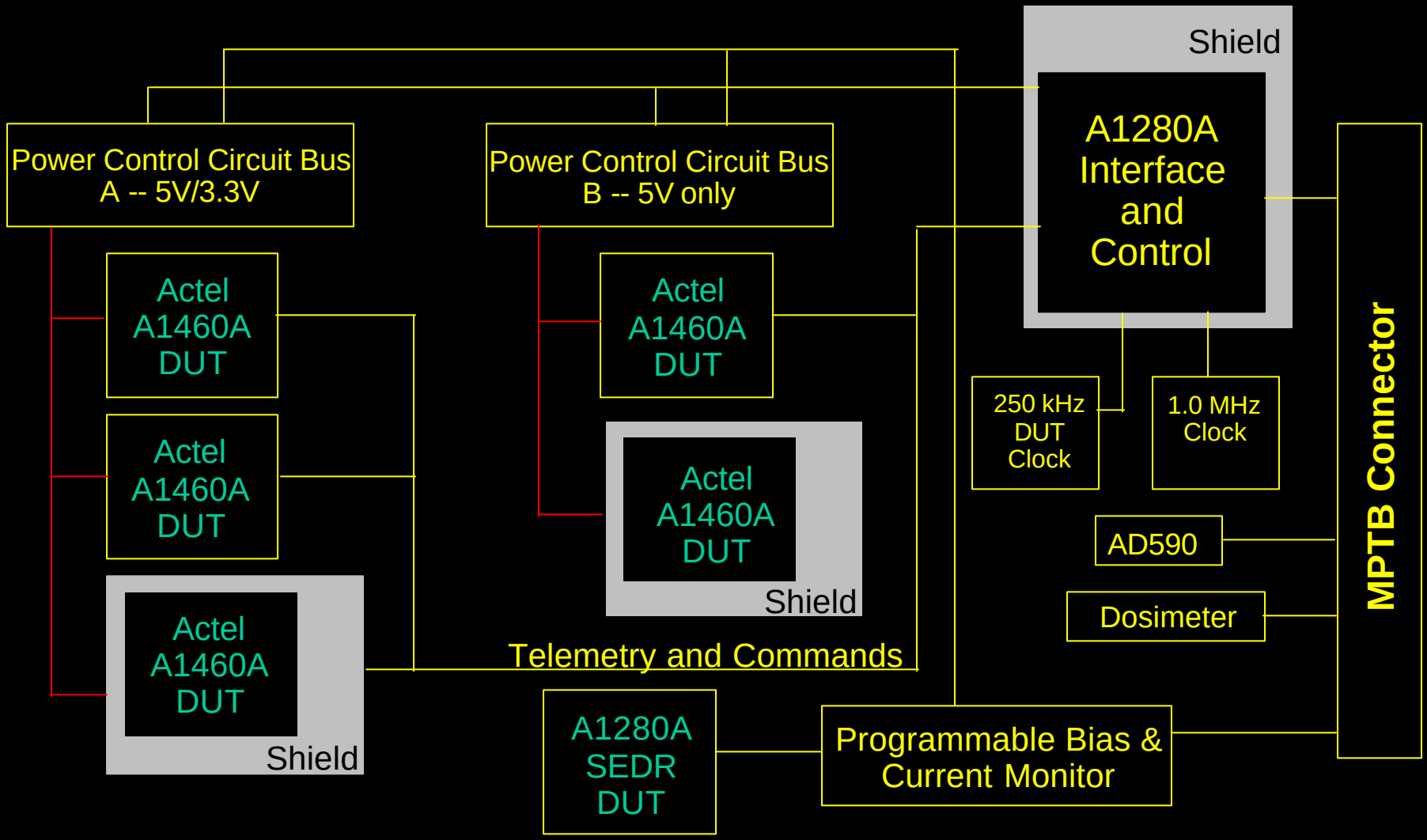


- Boundary Test Standard
- On All Modern FPGAs
- Can Command Each Pin as an Output (EXTST)
- Variety of Test Modes
- Optional Hard-wired Reset

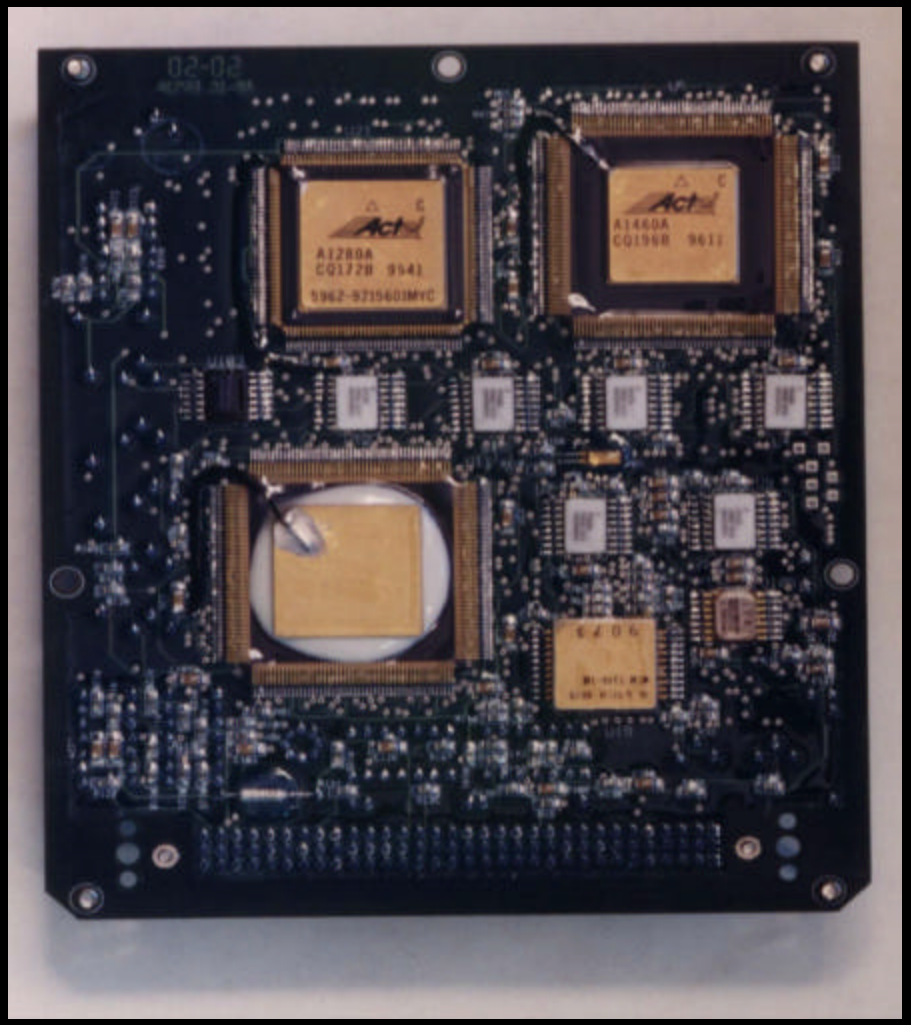




In-Flight Radiation Experiment



MPTB FPGA Board



Conclusions

- Scaling vs. Process vs. Voltage vs. Design
  - Many ‘Rules of Thumb’ Fail
  - Testing and Analysis Required
- New, Modern Architectural Features
  - Increase Rad Effects and Affect System Reliability
  - May Introduce New Failure Modes
- COTS Circuit Structures and Radiation
  - ‘Qualification By Similarity’ Can Fail
  - Screening Procedures for Antifuses Critical
- Test Methods Must Be Continuously Updated