



Alpine
Microsystems

Silicon Based SiP

Beyond SoC

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SOC vs SiP

- System on Chip Technology relies on novel IP and Integration Strategies
 - IC Tools
 - Methodologies
 - Homogeneous Semiconductor Material

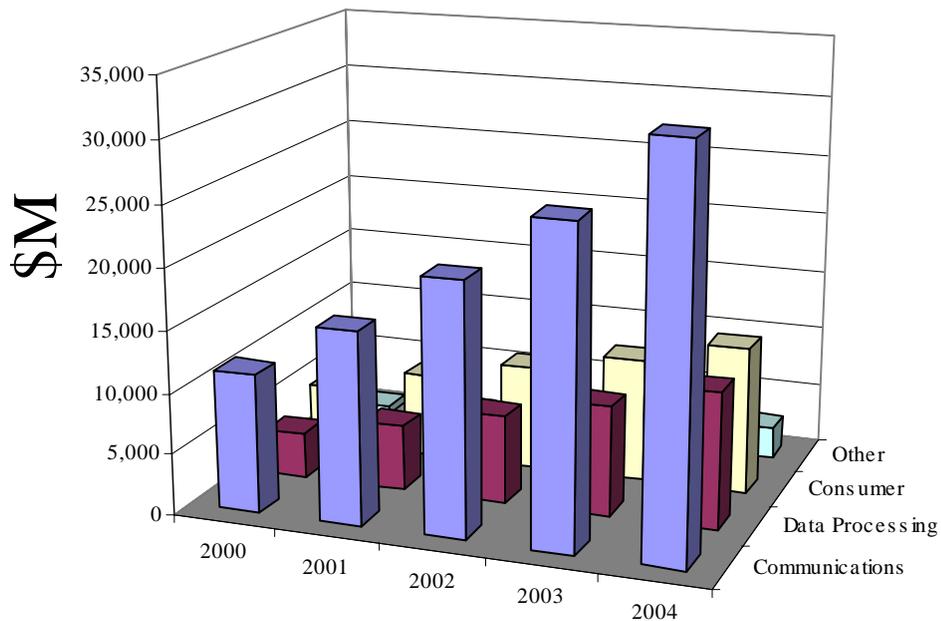
- System in Package Technology leverages existing Integration Strategies
 - MCM / PCB Tools
 - Methodologies
 - Heterogeneous Semiconductor Materials

- In the 80's, ASICs displaced TTL
- In the 90's ASIC methodology fundamentally changed the way ICs were designed
- In the next few years, System in Package technology will fundamentally change the way **ICs and systems** are designed and manufactured.

Target Markets

Alpine's flexible solution addresses the fastest growing markets

System Level ASIC/ASSP Market



- DP / Consumer
 - Notebook PC
 - Portable digital
- Communications
 - LAN/WAN switching
 - Electro-Optic PHY

Source, Gartner Group, 2000

Market Requirements

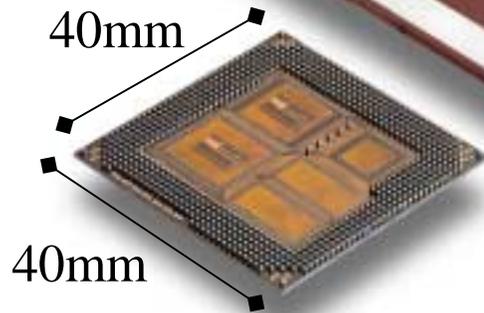
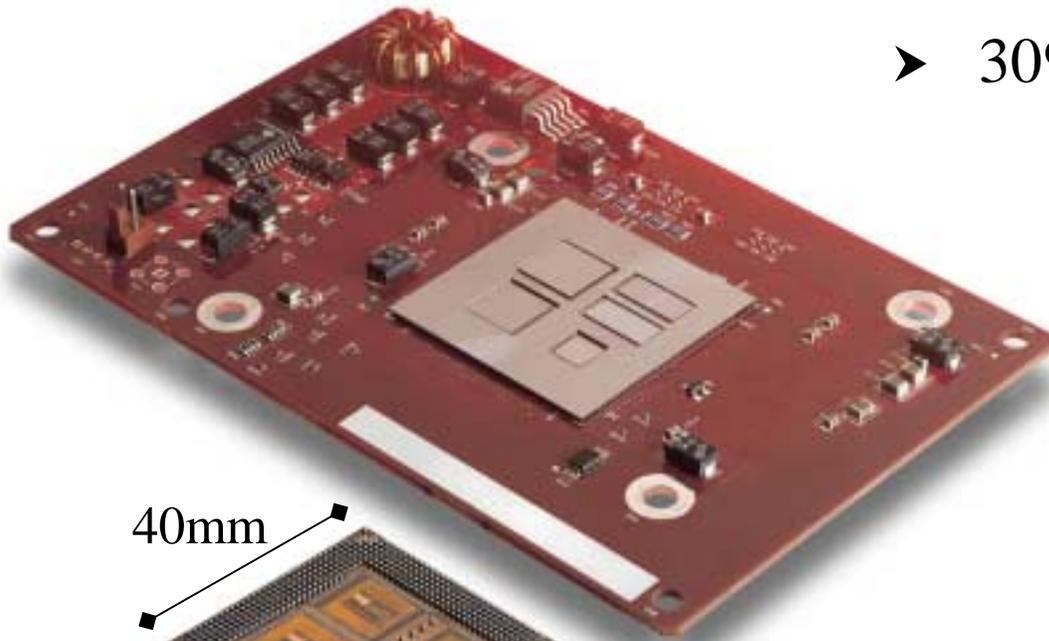
Alpine's SiP solution solves critical requirements

- Higher bandwidth
- Reduced system cost
- Fast, economical design flow
- Increased functionality
- Reduced footprint, power, noise
- High testability



Example: Desktop CPU

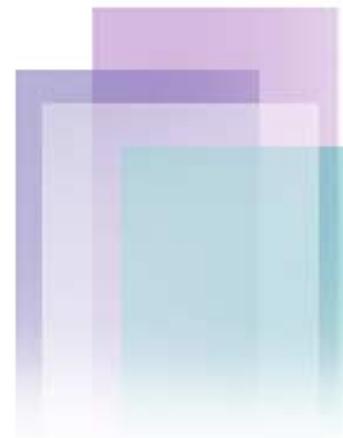
Integrate multiple ICs to eliminate PCB interconnect & area



➤ 30% increase in performance

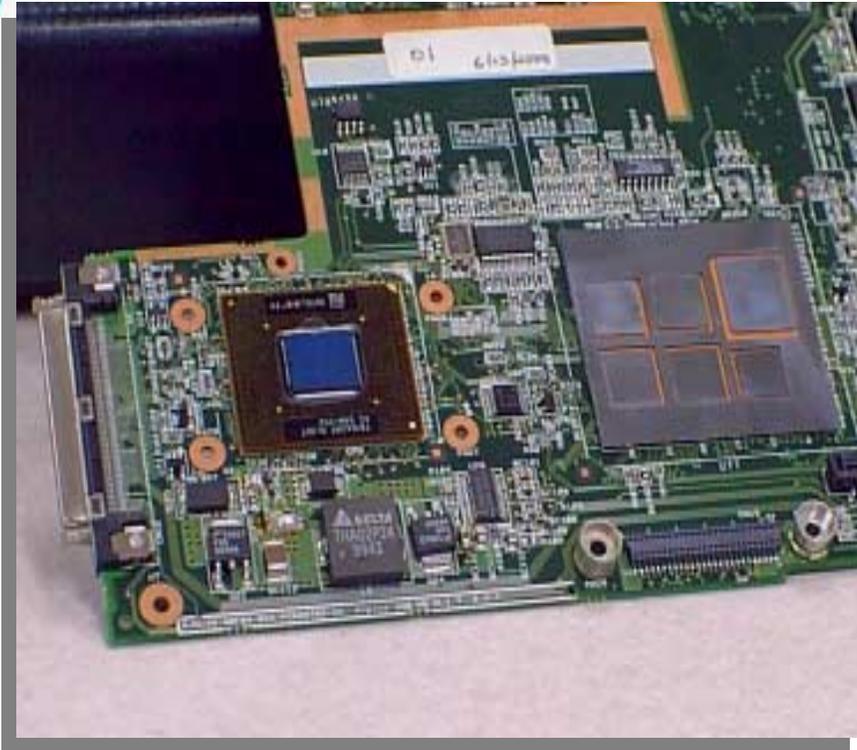
➤ 30% power decrease

➤ EMI attenuation



Example: Notebook PC (*after*)

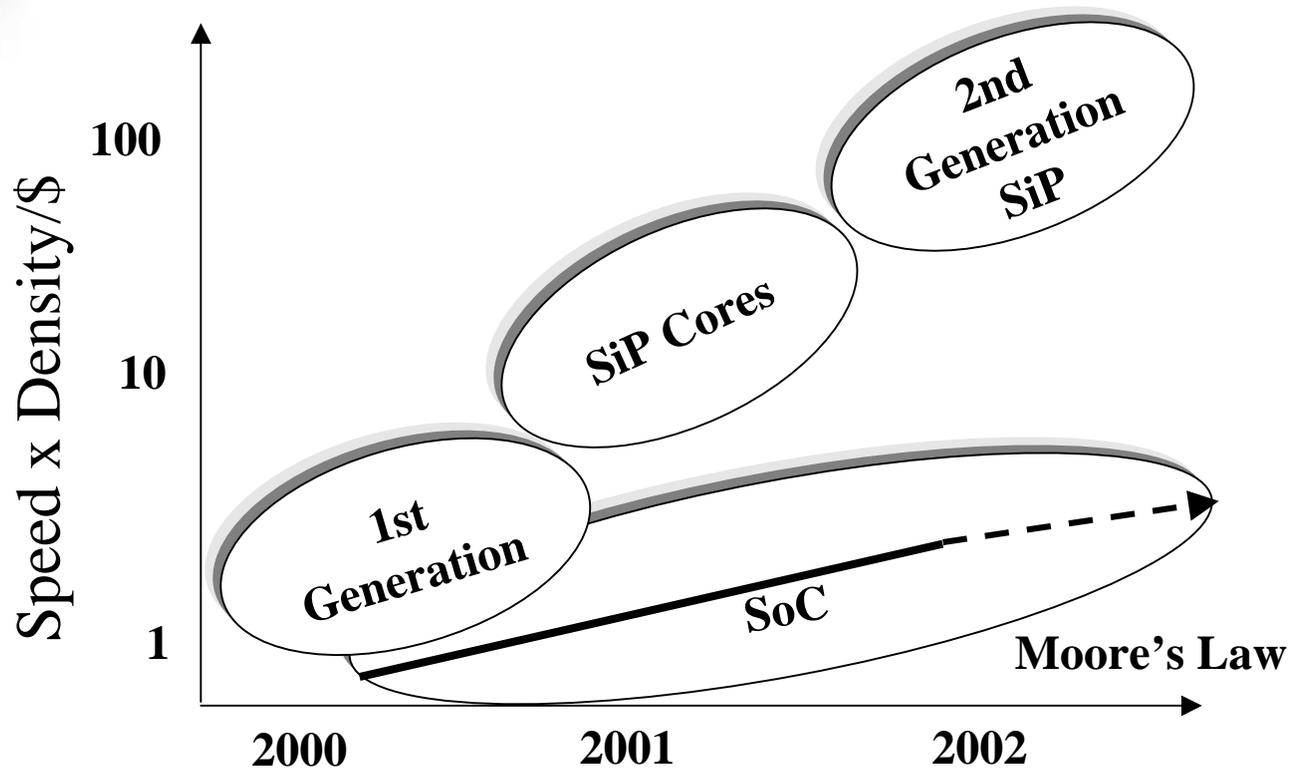
Solution: *Eliminate components from motherboard*



- ▶ Lower system cost
 - 5 fewer packages
 - 2 fewer routing layers
 - 900 fewer solder joints
 - 35 fewer passives
 - No DIMM socket
- ▶ Lower power by
 - 475 mWatt

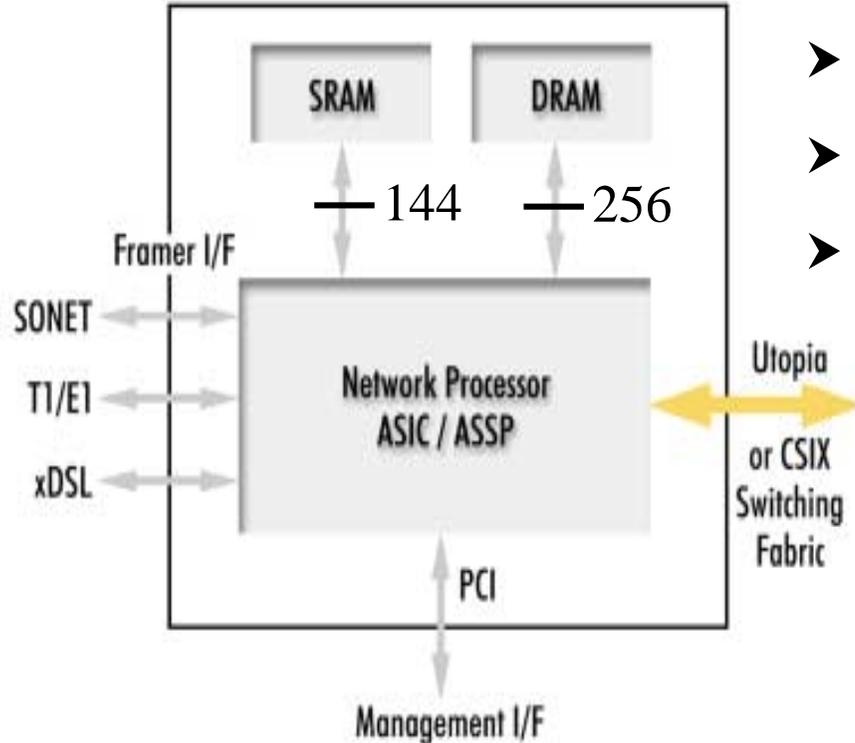
Alpine SiP Roadmap

System complexity is growing at a greater rate than SoC and PCB based solutions - SiP solves this issue.



Optimized Cores

SiP optimization of ICs creates breakthroughs in system cost and performance

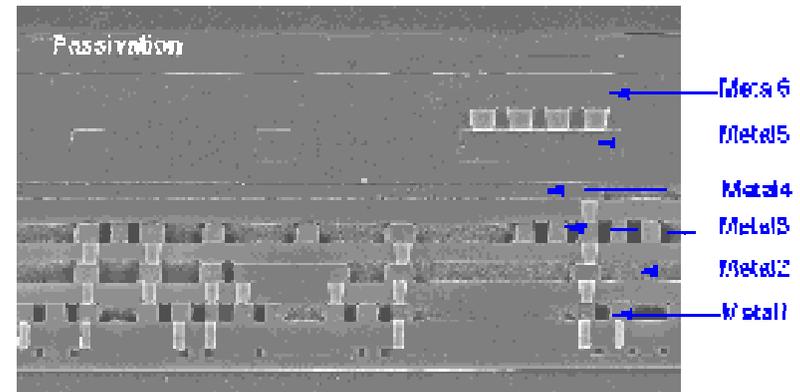


- High speed, low voltage I/O
- High density I/O
- Simplified IC processing
- Reduced IC area

Alpine SRAM Core

SRAM bandwidth benefit of embedded solution in a silicon part

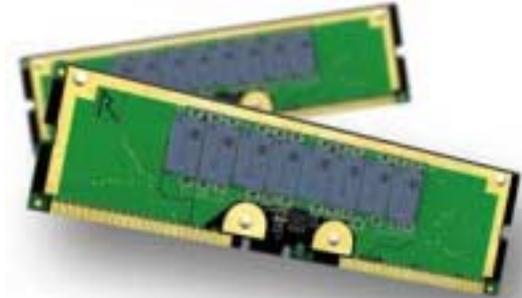
- High capacity
 - 9Mb (128k x 36 x 2)
- High bandwidth
 - 25GB/s peak bandwidth
 - Dual port
- Current technology
 - 0.18 μ m
 - samples Q2/2001



Alpine DRAM Core

DRAM bandwidth benefit of embedded solution in a silicon part

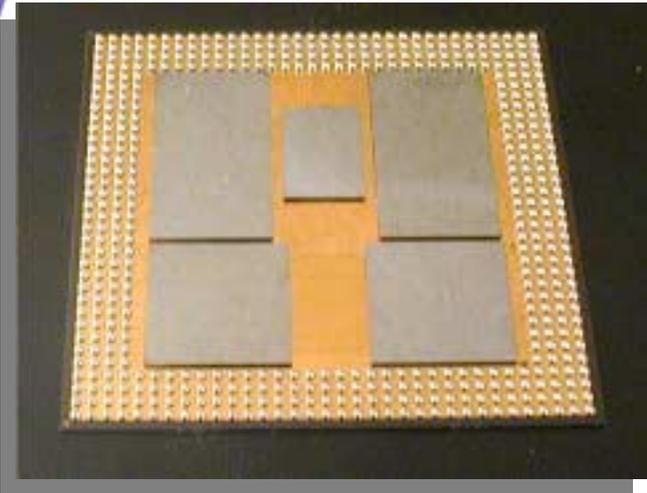
- High capacity
 - 64Mb (512k x 32 x 4)
- High bandwidth
 - 12GB/s peak bandwidth (10x RAMBUS)
 - Quad port (16 bank) concurrent access
- Current technology
 - 0.17 μ m from memory partner
 - samples Q2/2001



Architecture

Patented solution for multi-chip integration

- Chip-sized routing substrate
 - High yield, small footprint



- Silicon BGA
 - High performance package
 - Low profile form factor
- Integrated passive components
 - Increase performance and value

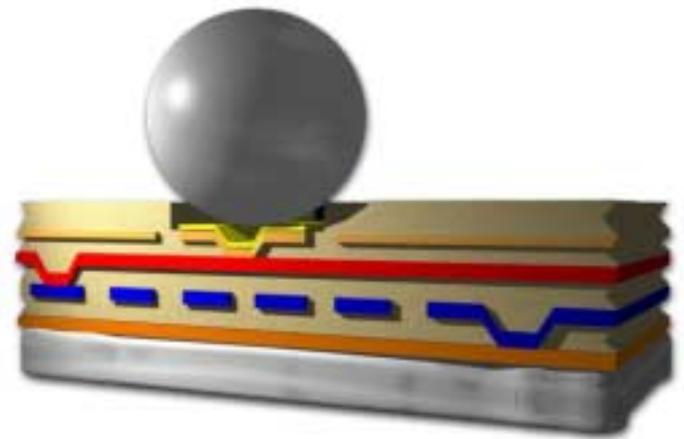
Wafer Processing

Applying IC technology to interconnect

- Microelectronic fabrication
 - Low cost, high density routing
 - 25 μm trace and via pitch

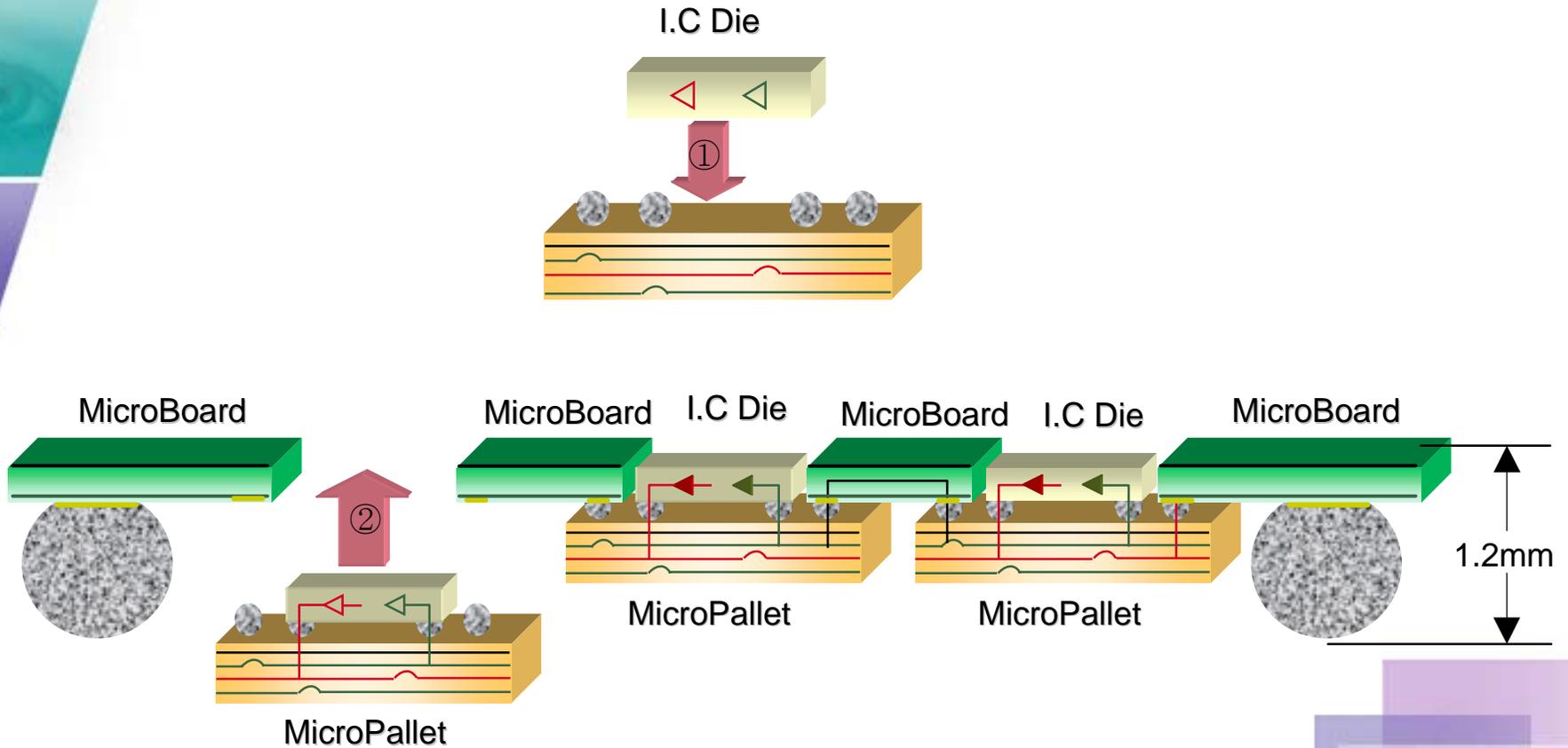
- High speed copper routing
 - 50 Ω transmission line
 - <100pS / cm propagation delay

- Integrated solder bump
 - 125 μm I/O pitch = >5000 I/O per cm^2



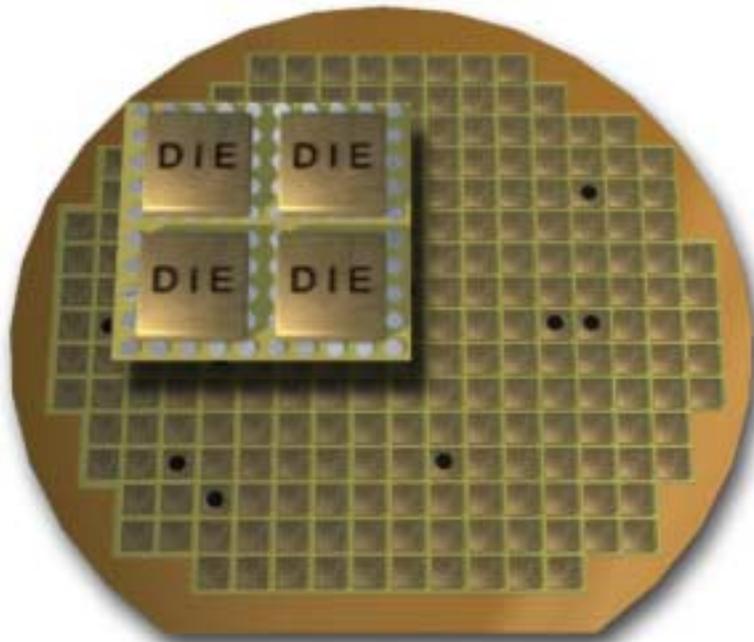


Assembly Technology



Assembly & Test

Wafer level solution to optimize yield



- ▶ Wafer level handling
 - Eliminate bare die damage
- ▶ Wafer level flip-chip attach
 - High throughput process
- ▶ Wafer level test
 - Eliminate compound yield loss



Interconnect Hierarchy

Alpine's MicroBoard substrate enables higher speed and density than SoC, with design time similar to PCB

	PCB	MicroBoard	SoC
Performance	1	100	10
Complexity / \$	1	50	10
Design Time	1	1 - 2	10



Interconnect Hierarchy

Alpine's SiP solution solves the cost and complexity limitations of traditional multi-chip approaches.

	MCM/L	Alpine SiP	MCM/C
Performance	1	40	10
Interconnect Density	1	5	2
Known Good Die	yes	no	yes
Design Time	1	1 - 2	5