# Reliability of Copper Metallization

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## Introduction

In a review paper written a few years ago, Cu metallization was characterized as "Always was and always will be the wave of the future". (1) Cu is finally here and in all probability, it is here to stay. Copper is becoming the metallization of choice for high performance microcircuits. It is conceivable that in the near future it may become difficult, if not impossible, to avoid copper. Copper is a very different material than Al that has been the standard IC metallization for the past thirty years. The metallurgy of the two materials will be discussed as well as the reliability challenges facing us in its use.

## Why do we want Copper in the first place?

The reason Cu is so desirable at this point in the development if the integrated circuit is its *low resistivity*. RC delays are the gating factor in limiting the performance of a digital circuit. The lower the resistance, the faster the circuit. Of all the metals in the periodic table, there are only 4 that have resistivities low enough for use in ICs. These are the Noble Metals and Al. All the other metals are significantly higher in resistivity than these four and therefore unsuitable for use in IC technology.

Cu is one of a class of materials known as the "Noble Metals" which also include Ag and Au. The Noble Metals, Group IB (column) in the periodic table, are characterized by weakly held valence electrons surrounding a tight heavy stable core. These weakly held electrons are very mobile and therefore all of the Noble Metals exhibit remarkably good conductivity. The three best normal conductors in nature are silver (1.60  $\mu\Omega$ -cm), copper (1.67  $\mu\Omega$ -cm) and gold (2.3  $\mu\Omega$ -cm). Aluminum is 4<sup>th</sup> on the list at 2.69  $\mu\Omega$ -cm. (All resistivity figures are at 20C)

## Noble Metallurgy

The Noble Metals are physically quite similar and as a result very similar chemically. There is also a logical progression in their response to their environment.

The Noble Metal phase diagrams represent this similarity. The Ag/Au system is perhaps the best example known of a perfect solid solution with a single solid phase. The 2 phase "slushy" regime near the melting temperature is even remarkably narrow, thus Ag and Au atoms have a difficult time telling each other apart. The Au/Cu system at high temperature is similar, but there are a few ordered alloy phases that can appear as the temperature is lowered and you have the patience to wait for the sluggish solid state reaction to occur. Only the Ag/Cu system is different, this being a simple eutectic with substantial solid solution on either side.

All the Noble Metals are FCC, mechanically weak in the unalloyed state and excellent electrical and thermal conductors. These common traits are due to their very similar electronic structures. Each is characterized by a heavy core of very tightly bound electrons that effectively shield the outer electrons from the positive nucleus leaving them relatively free. When condensed into a crystal, the outer electrons are almost totally given up to the Fermi sea. Therefore the Fermi surfaces of each of these elements are very nearly spherical. For one, this leads to the close packed FCC structure shared by all the Noble Metals and also contributes to their electrical and mechanical properties.

#### Silver

Ag has the lowest room temperature resistivity of any metal (1.60  $\mu\Omega$ -cm). Silver, then would be our logical first choice for conductor metallization, if it were not that there are properties that have made it less desirable than the others. Most importantly, Ag is a VERY fast diffuser in dielectrics, especially in the presence of an electric field. The rapid diffusion is because diffusion in the field is as an ion, and not as an atom. As an ion, Ag is very much smaller than when in the atomic state and can easily pass through the relatively open structure of the dielectric. The mass transport mechanism is not classical solid state vacancy diffusion like it is in metals, and therefore extremely fast. This is not only true for Ag, but applies to Au and Cu as well, but for Ag, it appears to be more important.

Compared to aluminum, copper offers ~37% reduction in resistivity, and this is significant. The difference in resistivity between copper and silver is only ~5% percent and the difficulties in processing and maintaining Ag as a conductor are very great indeed. Therefore, there is a significant driving force to change from Al alloys to Cu or Ag, but little to use silver in preference to Cu.

#### Gold

Au is "most noble" of the Noble Metals in that it does not corrode in any common environment, will not oxidize and will not even tarnish as silver will. Gold, however, has many of the same problems as Ag, in that it is a very fast diffuser in dielectrics, for the same reasons. Gold is also a "lifetime killer" in silicon devices, making it absolutely necessary that it not come into contact with devices. If corrosion were the major criterion for choice of a conductor material, gold would be the best candidate. However, the problem with gold is that its resistivity is not much different than pure Al, and therefore there is no compelling reason to choose it. For this reason, if we need to deal with the problems of noble metallurgy in our processing, we may as well take the least noble of the three, but the one that is the best compromise.

### Copper

Copper exhibits many of the same problems of the other two noble metals, but has the distinct advantage in that its resistivity is substantially better than Au and only slightly worse than Ag. This coupled with the diffusion through dielectrics, much faster than Al, but not as fast as Au or Ag makes Cu the best compromise. In addition, there is a well established and well understood Cu deposition technology that can be adapted.

Cu is best applied by electroplating. With the use of "leveling agents" or additives that slow the deposition of Cu, remarkable coverage of deep high aspect ratio trenches can be achieved. The concept is that the additives are large molecules that do not move as readily as the Cu ions in the plating bath and have a difficult time diffusing into the deep trenches encountered in the damascene process. As a result, during deposition, there is much less additive in the trenches as there is on the planar surface. Therefore, the plating is more rapid in the trenches that on the surface, leading to the "leveling" that is needed for multi-level IC designs. With these techniques, very high quality Cu metallization conductors can be produced at very small dimensions and retain almost theoretical bulk resistivity values.

The only fly in the ointment is the need for a barrier. Cu is a noble metal and, as such, readily diffuses through dielectrics. In order to obviate this problem, a liner or barrier metal is needed to

keep Cu from diffusing through the interlevel dielectrics. This becomes even more important with the use of organic low-k dielectrics we will soon be seeing in the marketplace.

With lower resistivity, higher average currents are possible and in fact desirable from a performance standpoint. At first thought, Cu should be up to the task. When a metal conductor carries very large current densities, it is subject to failure from a failure mechanism known as electromigration. Electromigration occurs when diffusing metal atoms are bombarded by conducting electrons and effectively push the metal atoms in the direction of electron flow. Since electromigration. Because of its higher melting point (1083C vs. 660C), copper diffusion should be much slower than in Al, which *should* permit higher currents to be carried in otherwise equal conductors with acceptable reliability. It *should* be superior to Al in resisting electromigration failure.

As we will see, however, this advantage may be somewhat of an illusion. There are significant material properties that have made Al alloys more electromigration resistant than we might have expected, especially in the fine line regime, and make Cu less of an advantage over Al than we had hoped for.

## The differences between Aluminum and Copper

In most contemporary integrated circuits, Cu is not used as the conductor material. The microelectronic industry recognized early on that Cu was a difficult metal to process and that Al was conductive enough, at the time. This was OK in the early days of integrated circuit (IC) development, but as performance increased, the demand for lower resistance came along with it.

Pure Al is approximately 60% more resistive than Pure Cu. Pure Al, however, is hardly ever used either. Only in the lowest performance circuits is pure Al even considered. Al alloys are almost exclusively used instead. Al-Cu, the alloy most employed as a conductor, is more than twice as resistive as pure Cu. The reason for using alloys regardless of the effect on resistance is that pure Al was found to be susceptible to a failure mechanism known as electromigration.

Electromigration is the mass transport of metal atoms due to the momentum exchange resulting from collisions of conducting electrons and defects (such as vacancies and grain boundaries) in the metal conductor. This is a form of diffusion. Due to its low melting temperature, diffusion is relatively easier in Al than most other metals and since thin film conductors have a fine grain size, a large fraction of the cross section is composed of fast grain boundary diffusion pathways. This combination made Al very susceptible to electromigration damage.

In order to mitigate this problem, the practice of alloying the Al with Cu was adopted. The conventional wisdom has been that the addition of small amounts of Cu slows down the Al grain boundary diffusion. This has been challenged recently, leaving the mechanism a matter of speculation. Whatever the reason, the addition of Cu increased the time to failure by about 2 orders of magnitude but also raised the resistivity of the conductor substantially. In the language of the microelectronics industry, the Al/Cu alloy was called "copper doped aluminum" and has served it well for over thirty years.

As chip speeds increased and the design features became smaller and smaller, there was an increased need for a conductor metal with lower resistance than Al/Cu alloys. The only candidates for this were the noble metals.

Not only the electrical properties, but the chemical and mechanical properties of all materials are determined by their electronic structure. Features of the electronic structure make the Noble Metals relatively unreactive compared to other elements. In particular, they are not very susceptible to oxidation. Au is well known for this property, but even Cu, the most reactive of the trio, does not oxidize readily. When it does, it forms a weak oxide that tends to show poor adhesion to the metal surface. Al, on the other hand reacts violently with oxygen and, once formed is remarkably stable. It is so stable that pure Al does not exist as a free metal in nature. It is always combined. In fact, it is so difficult to free Al from its oxides that, although it is one of the most common elements in the earth's crust, metallic Al was not available for use until the latter part of the 19<sup>th</sup> century. It was so difficult and therefore so expensive to isolate that Napolean reserved Al tableware for his most important guests. Everybody else got gold.

Unlike the oxides of Cu, Al oxide is not only extremely stable, but it is adherent, continuous and just about impervious. The mechanism for the oxide formation and growth is the diffusion of oxygen through the oxide. The diffusion is very slow. As a result, a very thin oxide film (~ 60A) is formed on any Al surface that makes the rest of the structure resistant to further oxidation. This physical process is referred to as a "self-limiting oxide growth" or "self-passivation". The oxide acts not only as a barrier to oxidation, but also as an effective diffusion along the oxide/Al interface is difficult due to the god chemical/mechanical bond at the interface. This just about eliminates what is usually the fastest mass transport, surface diffusion. For these reasons, Al alloys have proven to be a very forgiving class of materials, suitable as a conductor in integrated circuit manufacture. The alloys are relatively conductive, stable, and extremely process-error tolerant.

Cu does not possess such cooperative properties. Cu is an excellent conductor, but its poor quality oxide doesn't afford the protection that  $Al_2O_3$  does, and, furthermore, Cu diffuses readily through silica glass and polymer dielectrics. Al, again due to its affinity for oxygen, does not appear to diffuse readily at all.

Cu also has a very troublesome property that Al does not possess. It is a very effective poison for Si devices, being know as a "Lifetime Killer". Therefore, the Si devices must be protected from Cu atoms diffusing into the single crystal chip. This must be accomplished either through preparation of the dielectric layers between the metallization and Si or by some diffusion barrier. Often a refractory metal, such as Ti or some exotic alloy or pseudo-alloy like Ti:W is used for this purpose. If the underlying diffusion barrier is not properly applied, there will be serious problems, much more serious than if Al were in contact with Si. Al/Si reactions are not as damaging to the circuit and occur at much higher temperatures. Cu is such a fast diffuser in Si, that if contact were made at low operational temperature, serious damage to the circuit would result.

For our needs as reliability engineers, these material properties become very important in the way we deal with Cu metallization. Al, being so forgiving, does not need to be watched as closely. We can make small mistakes from day to day and the Al conductor will be immune to these variations. Small variations during processing of Cu metallization may have big effects on the final product. Although Cu may be superior to Al alloys when everything goes right, it needs to be watched carefully.

### **Electromigration Performance**

The differences in electromigration performance between Cu and Al are the subject of much disagreement. Common wisdom would indicate that Cu should be much better with respect to electromigration performance than Al. As stated previously, electromigration is basically a diffusion phenomenon, and whatever will slow down diffusion will slow down electromigration. The activation energy for diffusion is correlated with the melting temperature of metals with similar crystal structure. Both Al and Cu are FCC metals, so Cu and Al should have activation energies for diffusion that are directly proportional to the relative absolute melting temperatures. In fact, this is roughly true. The puzzling thing is that when electromigration kinetic studies were performed with Cu conductors, the activation energy for failure was found to be substantially less than that anticipated, on the order of that for Al alloys.

In the following tables, measured activation energies and times to failure for Cu electromigration are presented and compared to recent Al/Cu data. Extrapolated MTF for NIST structures is calculated using the values in the reference and n=2 kinetics. For via terminated structures n=1 kinetics are used. For those cases where a measured activation energy is not available, the MTF is extrapolated using 0.8 eV for Cu and 0.9 eV for narrow line Al/Cu.

Activation	MTF	Temp	) j	MTF (5x10 <sup>5</sup> ,100C)	Remarks	Ref.
Energy (eV)	(hrs,°	K,MA/	cm <sup>2</sup> )	(years)		
	650	250	2.5	468	280 nm wide lines to via	17
	90	250	2.5	65	280 nm wide lines to via	17
	1300	250	2.5	936	810 nm wide lines to via	17
	440	250	2.5	317	410 nm wide lines to via	17
	430	250	2.5	310	410 nm wide lines to via	17
1.1					Vias	18
0.81					Vias	19
0.8	6	375	3	158	Via	23
	4	290	2	8	Via no liner	26
	20	290	2	40	Via with oxidized Ti liner	26
	100	290	2	202	Via with thin unoxidized Ti liner	26
	600	290	2	1215	Via with thick unoxidized Ti liner	26
0.90	10	250	2	14	Vias in 0.25 um lines	24
1.08	12	250	2	81	Vias in low-k dielectric	24
	23	250	2	32		27
All Cu				Range 8 to 1215	$Median = 250  \sigma = 1.5$	
All Al/Cu				Range 14 to 81	$Median = 32  \sigma = 0.9$	

#### Table I

Electromigration performance of via terminated structures for Cu and recent narrow line Al/Cu metallization.

Activation	MTF	Temp	j	MTF (5x10 <sup>5</sup> ,100C)	Remarks	Ref.
Energy (eV) (hrs, <sup>c</sup>		K,MA/	$cm^2$ )	(years)		
0.79	1.3	342	8.7	710		2
0.66	NA				IBM	3
0.95 to 1.3	10	350	2	2575 to 203214		4
0.86 to 1.26	NA				Large grained (1.26 eV)	5
0.8	NA				IBM Large Grained	6
0.81	28	250	8	1124	Pd <sub>2</sub> Si/Plated Cu	7
NA	160	250	8	6424	TiW/CVD Cu	7
0.54	167	250	8	603	TiW/CVD Cu (oxide passivated)	8
0.54	17	250	8	61	TiW/CVD Cu	8
0.32	33	250	8	17	TiW/CVD Cu/CVD W	8
0.41	22	250	8	25	TiW/CVD Cu	9
NA	135	161	10	204		10
NA	8	200	8	45	0.6 μm line width	11
NA	100	200	8	563	0.2 μm line width	11
0.69	362	200	6	556	Ti/CVD Cu	12
0.28	56	200	6	6	TiN/CVD Cu	12
1.06	191	250	6	40,116	TiN/PVD Cu	12
0.67	127	200	6	171	3 um wide PVD	25
0.60	157	200	6	133	0.5 um wide PVD	25
1.02	2430	200	6	3092	0.85 um wide PVD	25
0.9						21
0.81	19	200	8	114	CVD (200)	22
0.86	83	200	8	693	CVD (111)	22
0.89	278	200	8	2827	Electroplated (111)	22
	27	393	6	25,184		23
0.91	500	239	2	1984		13
	100				Al/Cu 3 μm wide	
0.72		241	2	85	Al/Cu 5 μm wide/grain boundary	13
NA	9000	250	1	12,600	Al/0.5% Cu narrow lines (high $\sigma$ =1.5)	14
0.94	702	250	3	12,640	Ti/Al/Cu narrow lines with CMP	15
All Cu				Range 6 to 200,000+	Median $t_{50} = 583$ $\sigma = 2.60$	
All Al/Cu				Range	Median $t_{50} = 5000 \sigma = 2.36$	
				85 to 12,500+		

Table II

Cu and recent Al/Cu electromigration data for "NIST" type structures not terminated in a via. Note that although Cu electromigration can be much better than Al/Cu, it can also be much worse

The data shown in Tables I and II produce a consistent picture of the relative performances of Cu and Al/Cu metallization. In both cases we can see that the Cu performance is much more variable than the Al/Cu performance. This is expected as explained in the following sections of this report. For lines not terminated in vias (not a realistic situation), Al/Cu appears to have an advantage on average, but the Cu can be MUCH better. It can also be much worse. For the lines terminated in vias (a much more realistic situation) the greater variation in Cu performance is also present, but the average performance is considerably better than with Al/Cu. This can be easily explained from the fact that Cu vias are Cu whereas Al/Cu vias are W. W provides an absolute flux divergence and a source of high stress. Both of these contribute to early failure. The dual damascene Cu vias, on the other hand, have a weak liner that produces a flux divergence, but cannot withstand the stresses of the mechanically robust W vias and are not as effective as diffusion barriers.

What is important is that the spread in lifetimes for Cu is rather large. The lognormal sigma is calculated at over 2.5. If this distribution holds to 3 sigma, we can expect there to be at least a 1% chance of obtaining a VERY poor lot, with a median time to failure in the field of no more than a year at typical microprocessor use conditions. A similar spread in the lifetimes of Al/Cu was found, but the order of magnitude larger median time to failure somewhat mitigates this problem.

It should be noted that the data in the tables would be representative of undifferentiated parts made by a variety of processes by a variety of vendors. If the best processes and vendors could be chosen, the distribution would be expected to be much tighter and represent much less of a problem.

Note also that the high sigma presented above and used in this calculation is in effect very unrealistic. The high sigma found by mixing the data from a number of vendors produces a very pessimistic view of the reliability that is not reflective of the actual expected performance. The high sigma is in effect an illusion. The real performance would be better characterized by testing parts from a single vendor and characterizing the reliability in this way. Several vendors could be separately tested, with the reliability of each of them estimated. The sigmas will undoubtedly be tighter and the extrapolation to small numbers (necessary in real reliability estimates) will be not only better but more realistic.

Note that although the best performance was with Cu, the lowest values for Cu lifetime are substantially lower than those for Al/Cu. Note also that if we were to use the median MTF values, we would conclude that Cu was not as reliable as Al/Cu. It could also be argued that recent Al/Cu data from bamboo structures where there is no grain boundary diffusion indicates that we do not need Cu for reliability, Al/Cu is good enough. However, the electromigration limited reliability of an integrated circuit is more dependent on the via performance than the line performance. This is because the via represents a flux divergence and obeys different kinetics. Lines obey Black n=2 kinetics where the lifetime is inversely proportional to the square of the current density. Vias and contacts obey n=1 kinetics where the lifetime is proportional to the inverse of the current density. Here is where Cu metallization shows a clear advantage. Although when it is bad, it is worse than Al/Cu, the average performance of Cu vias is markedly better than Al/Cu

The reason for the relative performances of Cu and Al/Cu is presented in the following tutorial.

## **Diffusion Pathways**

The primary diffusion pathway in any material is a function of temperature and the microstructure of the material. In these regards Cu and Al alloys differ considerably, and this is believed to be responsible for much of the difference in electromigration behavior. Let us examine the following illustration.

Consider a thin film conductor as shown schematically in cross section below

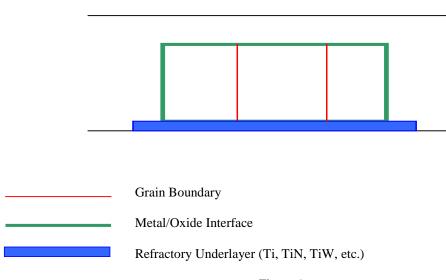


Figure 1

Schematic of a thin film conductor in cross section with an underlying barrier but no ARC layer.

The total mass transport is the sum of the separate quantities of mass moving through the lattice, the grain boundaries and the interfaces. I have chosen the example of a metal film with an underlying barrier metal, but without a capping layer such as an anti-reflective coating (ARC). The generalization to the situation where there are two interfaces with refractory layers is elementary.

What makes things interesting is that the temperature dependence of each of the three diffusion paths shown above is different. Diffusion, regardless of the pathway is "thermally activated", which means that the kinetics follow the Arrhenius relation. (Most, but not all, physical processes are thermally activated.) The Arrhenius relation is characterized by a pre-exponential (A) and an exponential term;

$$Rate = A \exp\left(\frac{-\Delta H}{kT}\right) \tag{1}$$

where A is in units of the rate that we are characterizing,  $\Delta H$  is the activation which is the amount of energy needed for the desired event to occur, T is the absolute temperature and k is Boltzmann's Constant, a conversion factor that relates temperature to the average thermal energy of elements in the system. We can see from eqn (1) that the rate of a thermally activated process can be quite sensitive to temperature, depending on the value of the activation energy. It is customary throughout the industry to represent energy in terms of electron volts/atom (eV). 1 eV is the energy that is gained by a single electron when it is allowed to respond to a potential of 1 volt. For energy in eV and for temperature in Kelvins, Boltzmann's Constant, k, is ~8.62 x  $10^{-5}$  ev/°K. Typical diffusion activation energies range from a few tenths to a few eV depending on the material and pathway.

The activation energies for diffusion along the different pathways available vary in an important manner. In most materials, the diffusion activation energies follow a hierarchy. Lattice diffusion has the highest  $\Delta H$  and is the slowest pathway, interfaces have somewhat lower  $\Delta H$  values and surfaces are the easiest and most rapid diffusion pathway with the lowest activation energy. A special interface in pure materials is the grain boundary. This is called a homogeneous interface where the interface is between small crystals, called grains, of the same material, but oriented differently. Grain boundaries are regions of disorder and therefore a faster diffusion pathways. Other interfaces, called heterogeneous, can have activation energies either higher or lower than the grain boundary. Experimentally determined activation energies for conductors used in the microelectronics industry, are presented in the following table.

Metal or Alloy	Grain Boundary	Interface (Typical)	Lattice	Surface
Al Al/Cu	0.6 eV 0.7 eV	? 0.9 to 1.0 eV		NA NA
Cu	1.2 eV	0.8 to 1.2 eV	2.1 eV	0.7 eV

#### Table III

#### Activation energies for diffusion along the important mass transport pathways.

In Table III there are a few important observations that can be made. The addition of Cu to Al increases the activation energy for diffusion along grain boundaries, but decreases the lattice activation energy. The surface diffusion in Al and its alloys is unavailable since this is blocked by the oxide. The interfacial activation energies are for those that have been measured in electromigration experiments for metals deposited onto TiN and would vary considerably depending upon what the interface was made of. If the process employs some other material, the interfacial diffusion may have no relation to anything shown here and would need to be individually determined.

Of the greatest importance is the observation that the activation energy for diffusion along some Cu interfaces may actually be lower than that for Al alloys. It is also important to note that the interfacial activation energy for Cu diffusion appears to generally be less than the grain boundary activation energy, in contrast to the case with Al alloys. This translates into a fundamental difference in the electromigration behavior.

The total mass transport through the cross section of Figure 1 would be the sum of the products of the mass flux in each of pathways and the cross sectional areas of the respective pathways. The effective diffusion coefficient is expressed as

$$D_{eff} = \frac{\left(A_{gb}D_{gb} + A_{int}D_{int} + A_{latt}D_{latt}\right)}{A_{gb} + A_{int} + A_{latt}}$$
(2)

where the A's are the *relative* cross sectional areas of the grain boundary, interface and the lattice as denoted in the subscripts. For illustration, we will assume a 0.5  $\mu$ m thick film that is 2  $\mu$ m wide with two grain boundaries on average contained in the cross section. The grain boundaries and the interfaces are assumed to be approximately two atoms thick, being composed of the atoms on either side of the boundary/interface. Thus, the thickness of these pathways will be approximately 0.5 nm. The relative cross sections of the assorted pathways are shown in the table below.

	Lattice	Grain Boundary	Metal/Refractory	
Boundaries			Interface	Interface
•			0.004	0.0045
2	0.997	0.0005	0.001	0.0015
1	0.9973	0.00025	0.001	0.0015
0	0.9975	0	0.001	0.0015

#### Table IV

Relative areas of the diffusion pathways for a  $2\mu m$  wide 0.5  $\mu m$  thick film containing 2, 1, and no grain boundaries.

At the low temperatures used in integrated circuits, Al diffusion is primarily along grain boundaries when they are available or at Al/metal interfaces when a bamboo or near bamboo structure has been obtained. From Table IV we can see why this is so. Grain boundary diffusion will dominate only if the grain boundary diffusivity is more than ~200 times the lattice diffusivity, if two grain boundaries are present, and ~400 times if only one grain boundary is present. Interfacial diffusion will dominate when the diffusivity ratios are approximately 100 or 65 depending on the interface.

Since the diffusion coefficients in eqn.[2] are thermally activated, (See eqn.[1]) the relative contributions of the different pathways will be a sensitive function of temperature. At operating temperatures (generally <100C), the conditions outlined above are satisfied for Al alloys and grain boundary transport will dominate. The measured diffusion activation energy for temperature ranges chosen near 100C will be that of the grain boundary. However, at higher temperatures, the differences between the exponential terms will become less and less as the temperature is raised. Eventually, the difference in the exponential terms will be less than the difference in the relative areas and lattice or interfacial diffusion will dominate the mass transport. When the logarithm of the diffusion coefficient is plotted against the reciprocal temperature (an Arrhenius plot) the slope of the line that results is proportional to the activation energy. This behavior is reflected in a "kink" in the plot or a curvature at the transition temperature. Below this temperature, for electromigration or any other diffusion controlled process, grain boundary activation energies will be measured and above that temperature lattice diffusion activation energies will be measured. In Cu, where the grain boundary, interfacial and surfaces are all active as diffusion pathways, the Arrhenius plot may not produce a straight line at all, but a curve reflecting this complex behavior.

At low temperature, electromigration in Al alloys is dominated by a) grain boundary diffusion, and b) when at high temperature, by lattice diffusion. At very low temperatures, it would be dominated by surface diffusion, if the surface were available, but it isn't. Therefore, at operational temperatures, Al electromigration is always dominated by grain boundaries or interfaces. In Cu conductors, however, the situation is somewhat different. Not only is the Cu oxide not a "good" one as it is in Al, but Cu itself does not adhere well to other oxides. This, too is a function of the reactivity of the material. Good oxide formers tend to adhere to oxides, whereas poor or mediocre oxide formers, like Cu, do not. Therefore, the metal/oxide interface, which is largely eliminated as a pathway for mass transport in Al is quite active in Cu.

Note from Table III that if we were to shut off this interface like we can with Al, Cu diffusion would be extremely slow and, by inference, electromigration would be much less of an issue. This is the major problem with Cu metallization and one of the reasons there has been so much contradictory evidence in the literature concerning Cu electromigration performance. **It appears that the quality of this interface, with respect to its ability to act as a diffusion pathway, is sensitive to process variations.** Sometimes it is shut off and at other times it is not. Within the same laboratory we have seen widely varying results emerge, depending upon when the study was performed. Times to failure can vary over orders of magnitude and the activation energy can vary between about 0.5 eV to over 1 eV. Even lower figures have been measured for the activation energy, but it is likely that these measurements suffer from some sort of experimental error, and my personal opinion is that they can be disregarded, but not ignored.

This sensitivity of the reliability to the processing history is a warning that Cu must be watched closely. Lot to lot variations, even an issue with the more process tolerant Al metallization, may be severe. When the Cu/oxide interface behaves well, electromigration performance is far superior to Al alloys, but if it is not behaving, the performance is no better than Al/Cu. In fact, for very narrow bamboo structure lines, where grain boundary diffusion is not available, Al alloys may actually perform better than Cu on average, especially if the interface cannot be controlled.

From these arguments, we can see that it is not automatic that Cu is better than Al alloys for electromigration resistance. In order to insure that a particular Cu metallization is up to the job day after day, periodic testing should be performed. If the vendor of a product made from Cu doers not have this information available, it might be a good idea to find a vendor who does. In addition, it is essential that a careful kinetic study be performed to insure that the surface or metal/oxide interface has been shut off. If the activation energy for failure is low, on the order of 0.7 to 0.8 eV, a high diffusivity interface is providing mass transport. If the activation energy is higher, on the order of 1.2 eV or higher, the surfaces have been shut off and mass transport is proceeding either via grain boundaries or some other more diffusion resistant interface. However, just because you might have measured this activation energy for today's product, it does not mean that tomorrow's Cu will be the same. Small process changes will most likely have a significant effect on diffusion.

A kinetic study should be performed during development at the very least, and should be repeated whenever any process change that may alter the nature of the underlying barrier metal is implemented. Diffusion along heterogeneous interfaces has not been studied in many systems, and just about anything can be expected. With many various metallization systems being considered with Cu, the interfacial diffusion can be expected to vary widely. Therefore, it is important to ensure that any potential suppliers of parts utilizing Cu have performed tests of this type.

## Oxidation

We have already discussed the differences in the way that Al and Cu interact with oxygen. Because of the protective oxide that forms on Al alloys, no special precautions with respect to atmosphere have ever been needed during accelerated electromigration testing. Al can safely be tested in air, even at elevated temperatures. Cu, on the other hand, oxidizes rapidly at high temperature in air. Cu will even oxidize in relatively good vacuums, especially if there is the slightest amount of water vapor present. This oxidation can be mistaken for electromigration if you are not careful. Cu oxide is not a good conductor, and when it does form, the available metal is reduced in cross section and the resistance rises. This can look very much like electromigration induced void growth.

In the earliest days of Cu electromigration studies, this author was embarrassed by precisely this particular property of Cu. A test was performed with a number of Cu lines and the experiment was conducted in the same manner as with Al alloys. The data looked great. Even the kinetic study looked fine. There was a 1/j<sup>2</sup> failure dependence and the activation energy was on the order of 1 eV. The resistance grew gradually at first then there was a catastrophic increase until an open circuit was formed. Had I never looked at the failed samples in a microscope, I would have been sure that I had nice, well-behaved, Electromigration failure, as well as a valid kinetic study. The results looked so good that I would have had no problem using the data to evaluate the process. However, when I looked at the samples. I noticed that all the failures were at the ends of the test stripes where they contacted the bond pads. My first assumption was that I'd used too high a current density and was causing temperature gradient failures, but then I noticed that damage was severe on both the anode and the cathode. What was unusual also was that the damage appeared to be guite extensive along the entire line connecting the bond pad and not as localized as temperature gradient induced failures appear. It was then that I discovered that I was not investigating electromigration at all, but was inadvertently studying the oxidation of Cu. The oxidation reaction appeared to follow an Arrhenius relation with an ~1 eV activation energy, and the  $i/i^2$  current density dependence was due to the effect of Joule heating on the oxidation rate. I never figured out whether the rate-limiting step was the diffusion of oxygen or oxidation itself, but, since this was not what I was interested in. I just recognized my mistake and went on with my work and corrected the error.

It is important, therefore, to insure that the Cu is not allowed to oxidize during electromigration testing. Care must be taken to do this properly. Testing in a reducing atmosphere may not be appropriate. If hydrogen is used, another effect will occur. Hydrogen has been observed to slow diffusion in many metals, including Al and Au, so this should not be used as a method to reduce oxidation unless it is to be used during actual operational. This is rarely, if ever, proposed.

Stressing in a nitrogen atmosphere may help in reducing the effects of oxidation, but it is imperative that the  $N_2$  be absolutely dry. Water vapor can oxidize Cu and if even the slightest amount of water vapor is present in the nitrogen, it will produce oxidation.

One way that has been used to reduce oxidation with some success is to cover the Cu metallization with a silicone based protective material. The silicones do not break down at normal testing temperatures (~200C) and appear to protect the Cu surface from oxidizing. This may be the simplest and most cost effective procedure in most cases. Polyimides have also been used for similar applications successfully.

If the Cu is covered with an interlevel or passivating glass layer, the stripe under the glass is protected, but the bond pad is not. This is what got me into trouble when I first investigated copper over a decade ago. (see box) The bond pad will oxidize, then the oxygen will diffuse along the Cu surface under the glass and oxidize the Cu line. The bond pad must be protected from oxidation to get valid results for the electromigration performance of Cu and Cu alloys.

## Wafer Level Testing of Cu Metallization

Wafer level testing has become popular because it promises to provide data much more rapidly and without the packaging costs associated with more traditional testing. There are problems with wafer level testing of any kind that is beyond the scope of this monograph and the interested reader is referred elsewhere. (16) The problems with wafer level testing of Cu are similar to those we have with conventional testing outlined above. One of the biggest problems is keeping Cu from oxidizing or corroding during the test. In packaged tests, this is easier to deal with by applying some kind of covering to keep the Cu away from the air. In a wafer level test, however, it is not clear how this can be easily accomplished using hot chucks and wafer probes.

Fast tests, like the SWEAT test pose another problem. Keep in mind that these problems also exist for Al alloy testing and there is nothing in the nature of Cu that should make the situation any different. The majority of these fast tests depend on Joule heating to provide the super-accelerated conditions to promote failure. The flux divergence responsible for the failures is caused by the temperature gradients induced by the Joule heating. Under real use conditions, we don't see this type of temperature gradient and this particular flux divergence is not present. If failures during the test are due to this, then, they are not the same kind of failures we would encounter under actual operation. The failure times, therefore, cannot be "decelerated" to use conditions. The data is irrelevant.

The high crossover temperature anticipated with Cu alloys allow much higher testing temperatures. These high temperatures will enable testing of Cu in a significantly shorter time period than is possible with Al alloys, without the problem of temperature gradients. At this time, packaged testing is limited to ~350C due to limits of the testing fixtures, but wafer level testing will not have these limitations. The maximum temperature will be limited by the oxidation of Cu, but if this could be solved, then testing temperatures as high as 450C can be envisioned. Although additional work needs to be performed to confirm some of this optimism, there is promise that, for pure Cu at least, high temperature wafer level testing can be performed in such a way that the results can be extrapolated to use condition. This is definitely not the case with Al alloys.

In any case, wafer level testing has been found to provide "Process Control" information, as long as the temptation to extrapolate the failure times from the stress to use conditions is not succumbed to. In addition, if a database of the performance under the wafer level testing is generated, any significant variation from what has been established as normal behavior, either positive or negative, can be treated as an aberration and investigated.

## Overstressing

There is great temptation to increase the stress in any accelerated test to obtain data in as short a time as possible. Time is money and management naturally is looking for a way to get data that is less expensive. However, we can easily fool ourselves. In many of the commonly accepted wafer level tests, the conditions were so severe that the wrong failure mechanisms were exposed. The trick is to have a test where we can get quick results that have meaning.

Testing that produces results that are irrelevant to actual use conditions is called overstressing and this will be explored in the following section.

#### **Temperature Acceleration**

The most common way to accelerate a failure mode that obeys an Arrhenius relation is to increase the temperature. Accelerations due to increased temperature can be expressed as;

$$\exp\frac{\Delta H}{K} \left(\frac{1}{T_{test}} - \frac{1}{T_{use}}\right)$$
(2)

where  $T_{test}$  and  $T_{use}$  are the test temperature and the operational use temperature respectively. Here it is assumed that the pre-exponential does not have a temperature dependence. The current electromigration models all include temperature in the pre-exponential in a variety of ways, but in all cases the exponential term dominates so that eqn.(2) is always at least approximately correct.

From the arguments made earlier, we see that the temperature must be limited to a regime where the same transport mechanisms are operating at the test as well as the use conditions. Assuming a fine line with a bamboo structure, we are limited to interfacial and lattice diffusion as mass transport vehicles. The cross-over temperature can be approximately calculated from the following equation;

$$T < \frac{k(\Delta H_L - \Delta H_I)}{\ln\left(\frac{wd}{10^{-7}(w+d)}\frac{A_L}{A_I}\right)}$$

where  $\Delta H_L$  is the lattice diffusion activation energy,  $\Delta H_I$  is the interfacial diffusion activation energy, w is the line width, d is the film thickness and  $A_I$  and  $A_L$  are the pre-exponential terms for electromigration coefficient for the lattice and the interface respectively. A includes terms related to the electromigration process at these locations as well as contributions from  $D_o$ , the preexponential for the diffusion coefficient.

There is no meaningful crossover temperature for thin films for Cu due to the great difference between the interfacial (0.8 eV) and the lattice diffusion energy (2.1 eV),. Even the most conservative estimates calculate a crossover temperature well over the melting temperature of Cu. Crossover from the interface to the grain boundary will not occur due to the near equivalence of their respective cross sectional areas. Therefore, unlike Al where we are limited to about 250 to 300C due to contributions from the lattice, we can stress at just about any temperature for Cu. The only limitations will be from the phase diagrams for Cu alloys. For pure Cu, this is also not an issue, as there are no phase changes before melting as the temperature of 1083C. Oxidation and the destruction of the testing apparatus will be the only limiting factor in how high a temperature we can use with Cu.

Cu alloys, on the other hand, will have limitations due to the dissolution of second phase constituents as the temperature is raised. This is also a limitation on the allowable temperature for stressing Al alloy conductors. Careful examination of the phase diagram for any prospective alloy

must precede the choice of stressing temperature to insure that the microstructure at test is similar to that at use conditions.

## **Current Acceleration**

Overstressing due to excessive current density is a much more insidious problem. The problem here is from Joule heating. When high current is passed through a thin film conductor, Joule heating produces an increase in the temperature. The temperature profile is a function of the geometry and composition of the metallization and is not uniform. Since it is not uniform, temperature gradients will be present.

Imagine a high current density being passed though a conductor with a temperature gradient along the direction of electron flow. Let the temperature be increasing from left to right.

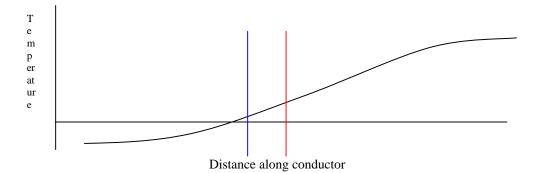


Figure 2. Schematic of the temperature profile along a conductor due to Joule heating. A region is defined between the two colored lines. Clearly the temperature is different at the two boundaries of the region. Any temperature dependent process would be affected accordingly.

If we define a finite length along the conductor as depicted by the two vertical lines in the schematic above, the mass flux at the left (blue line on the left) is less than that at the right (red line on the right). Therefore, if the current flow is from left to right, the region between the two lines will experience a loss of metal, and eventually a void will appear. If the current is flowing in the opposite direction, metal will accumulate and eventually an extrusion will develop.

The problem is that these types of flux divergences do not exist under real operational conditions. Therefore, data taken under these conditions is irrelevant to actual reliability. In order to ensure that the data obtained from accelerated tests can be extrapolated to use conditions, the current density must be limited. For a conductor line on the order of one micrometer wide deposited onto an interlevel dielectric on the order of 1  $\mu$ m thick , the current density must be limited to about 2 X 10<sup>6</sup> Amps/cm<sup>2</sup>. This figure for maximum current density is a sensitive function of the test structure geometry, the dielectric composition and thickness. Therefore, the maximum current density may differ considerably from this value and can be determined experimentally. Two million Amps/cm<sup>2</sup> must be considered a conservative value.

### **Test Structures**

Like any other electromigration program, you will require a suite of test structures for a complete characterization of your copper metallization. Although it appears that grain size to line width dependence is less important for Cu than with Al alloys, there is some indication from the

literature there may still be some effect of line width on lifetime. Therefore, just as with Al, the kinetics of wide and narrow lines need to be investigated, at least initially.

Vias also need to be studied. Cu vias connecting Cu conductors theoretically should be much better than W vias in Al alloy technologies, but recent experience (unpublished as of this writing) has been that vias significantly affect lifetime adversely. Therefore, we need to investigate what will happen with any proposed technology. The vias in the test structures should be connected to narrow lines and the maximum current density should be limited by the cross sectional area of the line, not the via. If the design calls for non-overlapped vias, it is essential that these be studied. It must also be stressed that the lot to lot variation expected for Cu metallization would be particularly true for Cu vias. Processing variations could play havoc with the local interfaces in the via structure.

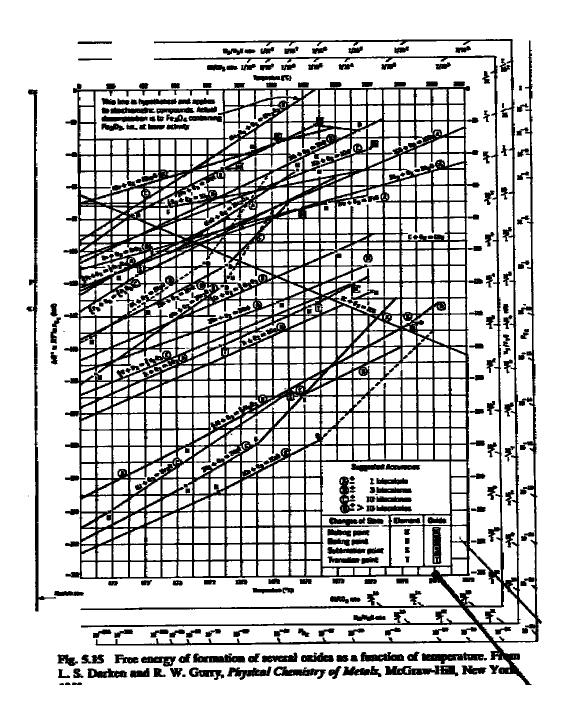
It is strongly suggested that via chains not be subjected to electromigration testing, but that single via structures be designed so that the ambiguity associated with the resistance increase of chains not be an issue in interpreting the data. (The question is, does the resistance increase represent the increase of a single via, or the gradual increase of all the many vias in the chain. The data would be treated completely differently)

# Cu Diffusion Through Dielectrics

The chemical/metallurgical nature of the Noble Metals as opposed to Al is responsible for another reliability issue that may have serious long term consequences. Al, due to its high affinity for Oxygen does not readily diffuse through oxides or other interlevel dielectrics. Being so reactive, it tends to react with whatever dielectric is present, often forming  $Al_2O_3$  which is an excellent diffusion barrier. Also, any Al that might diffuse through the Alumina layer will react with the dielectric and not make it through very quickly. Al is a gregarious metal, happily tying up with whatever is available. The snooty Noble Metals, however, act quite differently. Not being comfortable with the more prosaic elements, and being too proud to interact, they diffuse readily through the dielectrics.

The key to this behavior is illustrated in the following plot known as an Ellingham Diagram. In these diagrams, the free energy of formation for certain compounds is plotted as a function of temperature. On the following page is one for the formation of oxides. Given a line for a compound, once can see what will happen in the presence of a metal and the oxide of another. The lower a line is the more reactive. In this case we can tell much by looking at the relative positions of Al, Si, and Cu. Metal of a reaction lying below another will reduce the upper oxide forming its own oxide and liberating the metal.

Silicon lies between Cu and Al. Therefore if Cu is in contact with  $SiO_2$  nothing happens. Also, the small Cu atom will readily diffuse through Silica and not find anything it's interested in to interact with. If there were any free Si around, it would even reduce any CuO that may have formed, freeing the Cu to penetrate the oxide dielectric.



Al on the other hand will act in a completely opposite sense. Al in contact with  $SiO_2$  will reduce the Silica, forming Alumina which will block the movement of any more Al.

Because of this, Cu metallization requires a liner to keep it in its place. If Cu were to penetrate into the Si devices, it acts as a "lifetime killer" and is disastrous to device performance. Also, Cu can diffus rapidly enough trough some dielectrics, especially low-k oranics, that inter and intralevel leakage can be a problem. The problem with the liners, besides the necessity of them being essentially perfect, is that if they are too thick, the cross sectional average resistivity of the metallization becomes large enough that it no longer makes sense to use Cu. This is the reason it has taken so long to introduce Cu into IC manufacturing.

Because of this, IC liners with Cu are exceedingly thin. The IBM process, the only revenue producing Cu process in use at this time (although there are several, such as Texas Instruments, that will soon enter the marketplace), employs liners as thin as 100A and can be as thin as 50A in some critical areas. The metal used is Ta, but not pure Ta and they're not telling what the difference is.

Here is another area of great concern that must be checked to ensure reliability in critical long duration applications. Typical COTS type purchasing cannot be trusted. Although the probability of getting a bad chip may be relatively low, the consequences of getting one are disastrous. Also, inter and intralevel leakage can be checked relatively rapidly and it is anticipated that results can be obtained in a relatively short time.

# Summary

Cu metallization holds promise to allow higher performance IC's with superior reliability. However, the increase in reliability for sub-micron lines is not nearly as great as once though it would be and may not represent a significant increase over properly processed Al/Cu. It can be argued that for sub-micron lines, Cu metallization is not necessary for reliability.

Reliability is not the only reason for using Cu, and, since there are compelling reasons for its use we need to be able to test it adequately.

Due to the differences in the characteristics of the structure of Al and Cu and the attendant diffusion pathways, Cu will be much less forgiving and predictable than Al alloys. Therefore Cu must be watched more closely. If made properly Cu metallization will be superior to Al/Cu conductors, but if made improperly could be substantially worse. Electromigration testing of Cu conductors as a manufacturing line monitor is essential.

Fortunately Cu kinetics will allow higher temperature testing (400C +) with relatively short failure times and large scale testing of Cu does not present the practical difficulties that were posed with Al alloys. Oxidation of the Cu will be a major problem that needs to be addressed.

Cu electromigration testing represents a challenge that must be met to ensure reliability. It can be met if confronted with knowledge and intelligence.

Fur use in a spacecraft application where reliability is a must and where small numbers of parts are made, the traditional COTS approach may not be appropriate. However, a modified COTS approach, where samples from lots accepted can be investigated to ensure they are not "bad lots". This would mean using parts purchased from the same date code and a small number subjected to some kind of testing (to be determined on a product to product basis). Since the Cu can be tested at higher temperatures and the reliability due to electromigration related problems can be tested very quickly, this may not represent a significant increase in cost.

#### References

- 1) J.R. Lloyd and J.J. Clement, Thin Solid Films, 262, 125 (1995)
- 2) C.W. Park and R.W. Vook, Appl. Phys. Lett., 59, 175 (1991)
- 3) C.-K. Hu, M.B. Small and P.S. Ho, MRS Proceedings Volume 265, 171 (1992)
- H. Yamada, T. Hosji, T, Takewaki, T. Shibata, T. Ohmi and T. Nittam, Int. Electron Devices Meet., Tech. Dig., 269 (1993)
- 5) T. Ohmi, T. Hoshi, T. Yoshie, T. Takewaki, M. Otsuki, T. Shibata and T. Nitta, Proc. Int. Electron Devices Meet., IEEE New York, 285 (1991)
  T. Nitta, T. Ohmi, M. Otsuki, T. Takewaki and T. Shibata, J. Electrochem. Soc., 139, 922 (1992)
  T. Takewaki, T. Hosji, T. Shibata, T. Ohmi, and T. Nitta, Proc. Soc. Photo-Opt. Instrum. Eng., 1805, 3 (1992)
  T. Nitta, T. Ohmi, T. Hoshi, T. Takewaki aand T. Shibata, IEICE Trans. Electron. Dev., E76-C, 626 (1993)
  T. Nitta, T. Ohmi, T. Hoshi, S. Sakai, K. Sakaibara, S. Imai and T. Shibata, I. Electrochem. Soc., 140

T. Nitta, T. Ohmi, T. Hoshi, S. Sakai, K. Sakaibara, S, Imai and T. Shibata, J. Electrochem. Soc., 140, 1131(1993)

- 6) B. Luther, et. al., Proc. IEEE VMIC Conf., 15 (1993)
- 7) H.-K. Kang, J.S.H. Cho, I. Asano and S.S. Wong, Proc. IEEE VMIC Conf., 337 (1992)
- 8) H.-K. Kang, I. Asano, C. Ryu and S.S. Wong, Proc. IEEE VMIC Conf., 223 (1993)
- 9) J.S.H. Cho, H.-K. Kang, C. Ryu and S.S. Wong, Int. Electron. Dev. Meet., Tech. Dig., 265 (1993)
- 10) S. Shingobura and Y. Nakasaki, Appl. Phys. Lett., 58, 42 (1991)
- Y. Igarashi, T. Yamanobe, H. Jinbo and T. Ito, 1994 Symp., on VLSI Technology, Dig. Techn. Papers, 57 (1994)
- 12) L. Arnoud, R. Gonella, G. Tartavel, J, Torres, C. Gounelle, Y. Gobil and Y. Morand, Microelectron. Reliab., 38, 1029 (1998)
- 13) S. Foley, A. Scorzoni, R. Balboni, M. Impronta, I. De Munari, A. Mathewson and F. Fantini, Microlectron. Reliab., 38, 1021 (1998)
- 14) R.G. Filippi, E.N. Levine and K.P. Rodbell, J. Vac. Sci. Technol. B15, 750 (1997)
- 15) H. Onoda, T. Narita, K. Touchi and K. Hashimoto, Proc. 34th Ann. IRPS, 139 (1996)
- 16) J.R. Lloyd, Mat. Res. Soc. Symp. Proc. Vol. 265, 177 (1992)
- A.K. Stamper, W.A. Klaaasen and R.A. Wachnik Advanced Metallization Conference Orlando FL 28-30 Sep 1999
- C.-k> Hu, R. Rosenberg, W. Klaasen and A.K. Stamper Advanced Metallization Conference Orlando FL 28-30 Sep 1999
- 19) C.-K. Hu, K.L. Lee, L. Gignac, R. Carruthers, Thin Solid Films, 308, 443 (1997)
- 20) C.-K. Hu, R. Rosenberg, K.L. Lee, Appl. Phys. Lett. 74, 2945 (1999)
- V.V.S. Rana, J. Educato, S. Parikh, M. Naik, T. Pan, P. Hey and D. Yost, Advanced Metallization Conference Orlando FL 28-30 Sep 1999
- T.D. Sullivan, 5<sup>th</sup> International Workshop on Stress-Induced Phenomena in Metallization, Max-Planck-Institut fuer Metallforschung, 23-25 June 1999
- 23) C.-K. Hu, R. Rosenberg, H.S. Rathore, D.B. Nguyen and B. Agarwala 5<sup>th</sup> International Workshop on Stress-Induced Phenomena in Metallization, Max-Planck-Institut fuer Metallforschung, 23-25 June1999
- 24) T. Usui, T. Watanabe, S. Ito, M. Hasunuma, M. Kawai and H. Kaneko, Proc. 37<sup>th</sup> Ann Int'l Reliab. Physics Symp, 221 (1999)
- L. Arnaud, G. Tarteval, T. Berger, D. Mariolle, Y. Gobil and I. Touet, Proc. 37<sup>th</sup> Ann Int'l Reliab. Physics Symp, 263 (1999)
- K. Abe, S. Tokitoh, S.-C. Chen, J. Kanamori and H. Onoda, Proc. 38<sup>th</sup> Ann Int'l Reliab. Physics Symp, 333 (2000)
- 27) M. Dion, Proc. 38th Ann Int'l Reliab. Physics Symp, 324 (2000)