TECHNOLOGY READINESS OVERVIEW: **C**MOS **UL**TRA-LOW **P**OWER **R**ADIATION **T**OLERANT (**CULPRiT**) INTEGRATED CIRCUITS

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I. Technology Overview

A. Background

Two important issues that must be dealt with during spacecraft subsystem design are the power consumption and radiation tolerance of microelectronic components. Over the last decade an approach to these problems for active CMOS circuits has evolved that is distinct from traditional approaches. The low power aspect of the approach originated with Stanford's Ultra Low Power (ULP) CMOS Project [1]. This recognizes that CMOS circuits with high activity levels do not require low DC power dissipation. Thus, unlike standard CMOS circuits, which strive for low DC leakage currents, the ULP approach is based on balancing the AC (switching) and DC power dissipation so that they both account for about 50% of the power loss. This is accomplished by aggressively scaling the supply voltage (V_{dd}) and the transistor threshold voltage (V_t). The supply voltage reduction results in substantial power savings while the corresponding threshold voltage reduction tends to maintain circuit performance at a constant level, in spite of the V_{dd} reduction. Illustrative results of this effect are shown in Figure 1. This shows the power consumed in a 1 million transistor design as V_{dd} and V_t are scaled so that the circuit maintains a constant performance or speed. A fairly active circuit has been assumed (10% circuit activity), and reasonable CMOS transistor characteristics are also assumed (1 μA on current and a subthreshold slope of 80 mV/decade) for these calculations. Shown along the abscissa are the V_{dd} and V_t values. The result on the far left is typical of 3.3 V CMOS technology. Here, the transistors have V_t = 660 mV and the power dissipation is almost entirely AC. In principle, scaling these two parameters down together allows the circuit's performance to remain constant, while the power reduction is dramatic. The AC and DC power dissipation become approximately equal at V_{dd} = 0.5 V and V_t = 100 mV, which are typical of CULPRiT circuits.

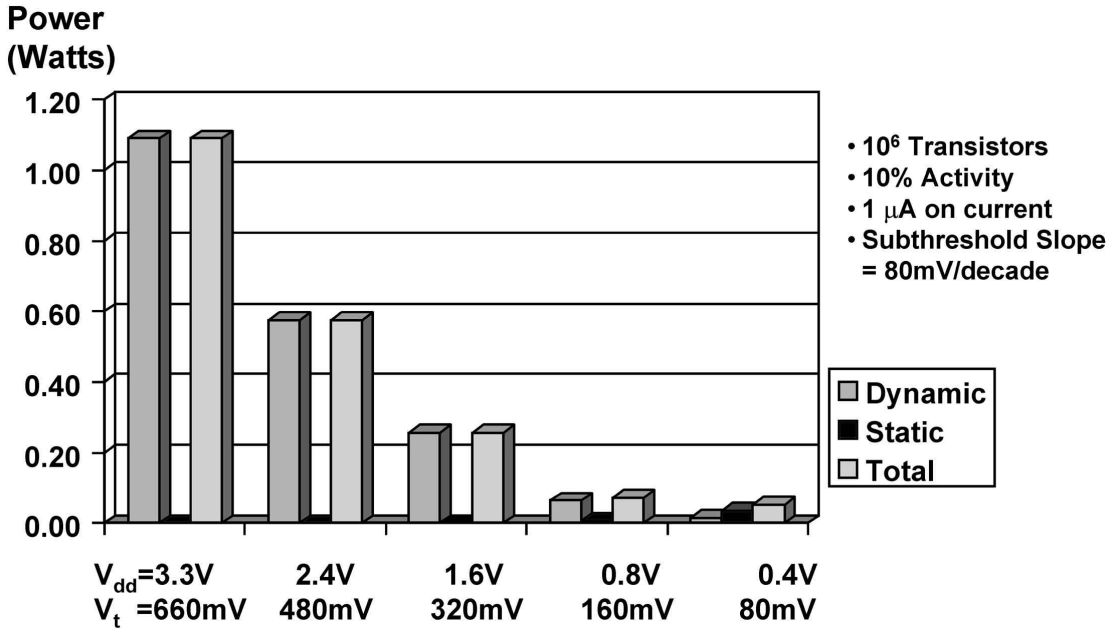

Fig. 1. Power consumption scaling at constant circuit performance.

This technology was geared more toward space applications and further developed at the University of Idaho, Center for Advanced Microelectronic and Biomolecular Research (CAMBR) [2,3], where single event upset mitigation design was introduced. It became known as **C**MOS **U**ltra-**L**ow **P**ower **R**adiation **T**olerant (**CULPR**i**T**) in a Department of Defense sponsored program, in which it was demonstrated that the technology is total dose tolerant at the transistor level [4]. This made a more realistic case in favor of using it for space applications because it then became unnecessary to modify the technology processing to achieve total dose hardened circuits.

B. Power Consumption

Several CULPRiT integrated circuits are currently under study including a version of the 8051 microcontroller and a version of the Texas Instruments C50 microprocessor. Currently, the most advanced CULPRiT integrated circuit is the Reed Solomon (RS) Encoder. In order to evaluate the reduction in power consumption, the RS Encoder design was implemented both in the AMI Semiconductor (AMIS) 3.3 V, 0.35 μm standard CMOS process as well as the 0.5 V CULPRiT process. The ULP process utilizes the same fabrication equipment and similar flows but does require additional processing steps compared to the standard CMOS. Measurements of the Encoder core power only, excluding the power required to drive the I/O pads and related board capacitance indicate a core power of 1.0 mW for the CULPRiT Encoder compared to 68

mW for the standard CMOS Encoder, while both are operating at a 10 MHz clock speed. The CULPRiT RS Encoder is functionally equivalent to another RS Encoder previously designed by CAMBR utilizing Aeroflex/UTMC radiation hardened technology and meets the requirements of the Consultative Committee for Space Data Systems (CCSDS) telemetry channel coding which has a broad space heritage [5,6]. By further comparison, the typical power consumption of the Aeroflex/UTMC radiation hard technology version RS Encoder flying in many spacecraft today is 350 mW (driving 50 pf loads at 10 MHz).

II. Potential Use

As discussed in the previous section, the most advanced CULPRiT integrated circuit is the RS Encoder. It is at a Technology Readiness Level (TRL) of 5, having been breadboard validated and tested for radiation, the latter to be subsequently discussed. The Encoders have not yet been flown in space, but are under consideration for use on NASA's ST5 mission. One of the attractions for the ST5 mission is that the power savings of CULPRiT make it a potentially enabling technology for nanosatellites. The current Encoder technology is likely to be useful on missions where the single event upset (SEU) environment is not too severe, such as low inclination LEO. For other orbits, SEU mitigation schemes may be required. Latchup and other destructive single event effects have not been observed in the CULPRiT RS Encoders. The technology is generally tolerant to total ionizing dose effects, which should not be an issue for many applications and missions.

III. Radiation Effects Overview

A. Total Ionizing Dose

CULPRiT technology is significantly more total dose tolerant than the corresponding standard commercial CMOS technology at the device level [4]. Standard CMOS technology typically fails due to radiation-induced leakage currents in the field oxide region. The reasons for the improvement of CULPRiT are two-fold. First, the reduced gate bias (V_{dd} = 0.5 V) used for CULPRiT limits the yield of radiation-induced holes in the field oxide. Second, the back-gate (substrate) bias used to control the low threshold voltages in CULPRiT technology increases the threshold voltage of the n-channel field oxide, thus suppressing radiation-induced parasitic currents. Total dose testing at the device level showed that the AMIS standard CMOS process was tolerant to about 30 krad(Si), while the corresponding AMIS CULPRiT technology was tolerant to over 200 krad(Si).

This level of total dose tolerance is expected to carry over to the circuit performance. The RS Encoders were tested at the NASA/GSFC Co-60 gamma ray facility under static bias conditions according to Mil-Standard 1019.5. The back-bias

applied during the test was chosen to optimize encoder performance at V_{dd} = 0.5 V. This turned out to be a p-channel back-bias of 2.0 V and an n-channel back-bias of –1.4 V. No degradation of performance in terms of leakage current, timing or functionality was observed at doses up to 100 krad(Si). This should be sufficient for many missions.

B. SEE Effects

Latch-up and other destructive SEE have not been observed in CULPRiT RS Encoders out to effective LET values of about 60 MeV-cm^2/mg. This is expected for latch-up because it is thought that the supply voltage is too low to sustain such a condition.

The low supply voltage, however, is generally an unfavorable condition for SEU. A formal design synthesis and analysis technique based on the theory of asynchronous sequential circuits has been developed at CAMBR and used to create a new Single Event Radiation Topology (SERT) cell design that was utilized for the CULPRiT RS Encoder design [7]. The idea is that when a particle strike causes an upset of one storage node the SERT cell feedback is designed to allow nodes to enter a high impedance or tri-state mode, thus improving SEU tolerance.

The onset SEU threshold for CULPRiT RS Encoders using the SERT cell design is about 20 MeV-cm^2/mg. This is high enough that the encoders will not experience proton-induced SEU. However, they will be susceptible to heavy ion induced SEU. The measured saturation cross section for SEU is about 17 μm^2/bit, indicating a low SEU rate. As an example, this data were used with the CREME96 suite of programs [8] to calculate SEU rates for a possible orbit for the ST5 mission. These calculations were done for an elliptical orbit with a 200 km perigee, 35,790 km apogee and 0 degree inclination. The SEU rates due to galactic cosmic rays (GCR) during solar minimum and solar maximum were calculated. In addition, the rates for a worst case solar particle event (SPE) during the peak 5 minutes, worst day and worst week of the event were also obtained. These results are shown in the table below.

SEU Rates for the 2048 bit CULPRiT RS Encoders Expected During the ST5 Mission

Condition:	#SEU/(bit-day):
GCR (solar minimum)	1.46E-9
GCR (solar maximum)	1.80E-10
Worst Case SPE (peak 5 minutes)	6.59E-6
Worst Case SPE (worst day)	1.83E-6
Worst Case SPE (worst week)	5.33E-7

IV. Potential Issues

A. Integrating 0.5 V Technology into Current Systems

Since satellite electrical subsystems operate at substantially higher voltages than the 0.5 V_{dd} used in CULPRiT technology, a major issue is how to integrate the technology. At the moment, the CULPRiT Encoder comes in two versions. One interfaces external to the Encoder chip at 0.5 V signal levels. The other includes on-chip level shifters that interface externally at 3.3 V. Currently, the only practical approach to subsystem design is to use the latter, in which case some of the core power savings are lost due to I/O power requirements. The full benefit of CULPRiT technology can not be obtained using discrete CULPRiT components in a 3.3 V electrical subsystem.

B. Noise Margins and Immunity

Initial studies have shown that the noise margins of CULPRiT technology scale at least as quickly as the supply voltage. Thus, relative to V_{dd}, the noise margins are probably no worse than current 3.3 V technology. However, effects such as electromagnetic interference on the CULPRiT low voltage outputs must be studied in the context of the system architecture.

C. SEU Mitigation

For orbits other than low inclination LEO, SEU is a potential problem. Each orbit should be considered on a case by case basis. Further SEU mitigation beyond the SERT topology discussed above may be required based on the SEU rate and the criticality of the effect.

References

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