Total Ionizing Dose Effects on Flash Memories *

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Abstract

This paper presents the results of measurements performed on two different flash memory types, NOR and NAND technologies. The data suggest that the degradation is influenced by the activation of integrated charge pump circuits. The NAND type device functionally failed at lower TID level than the NOR technology, even when the NOR device was used with the charge pump activated.

I. Introduction

Need for non-volatile, in-situ re-programmability in mass solid state storage applications in space system has increased in recent years. Due to the complex structures, limited total dose testing was done on earlier generations of non-volatile devices [1]. Flash memories with a very high density and a fast programming speed have been developed in recent years [2,3] and they are being considered for use in space.

There are two types of basic flash memory structures: NOR and NAND configurations. The NAND cell is inherently more sensitive to gate-threshold shifts due to total dose irradiation because it stacks many transistors in series. High internal voltages – 12V to 20V – are required to erase and write flash memories and charge pump circuits are provided internally to develop the high voltage from normal logic voltages.

Degradation of the charge pump can affect the radiation failure significantly. This paper compares the effects of total ionizing dose on the Intel 28F016SV and the Samsung KM29N16000 flash memories.

II. Device Descriptions

The Samsung KM29N16000 is a 2Mx8bits NAND cell structure flash memory. A diagram of the NAND structure is shown in Figure 1. Charge pump circuits are integrated in main and sub-row decoder. The Samsung device uses 16 control gates with a drain, and a source gate, for a total of 18 gates in the NAND stack. The oxide thickness between the floating gate and the body is about 25 nm. The NAND structure uses Fowler-Nordheim tunneling for both erasing and writing but with more uniform charge transfer between its floating gate and its body as shown in Figures 2(a) and 2(b).

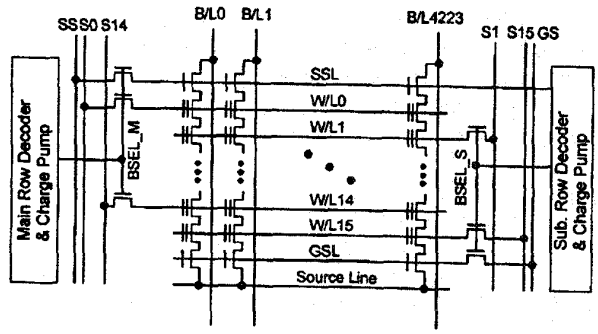

Figure 1. The NAND flash memory structure of Samsung KM29N16000 with charge pump [4]

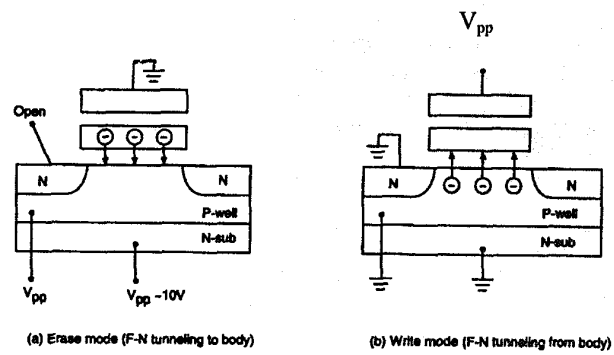

Figure 2. The NAND cell structure of Samsung KM29N16000

The Intel 28F016SV can be configured either 1Mx16bits or 2Mx8bits. The Intel device uses the NOR structure. It is fabricated with an EEPROM Tunnel Oxide (ETOX) process. Its memory cell consists of a source, a drain, and a select gate stacked over a floating gate. It is similar to the structure of an EEPROM but with a much thinner oxide, about 10 nm, between the floating gate and channel region to enhance the tunneling mechanism. By applying the high voltage V_{pp} to the source, floating the drain, and grounding the select gate, a whole block can be erased. During block-erasure, Fowler-Nordheim (F-N) tunneling pulls electrons off the floating gate by creating an electric field across the thin oxide, as shown in

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Figure 3(a). By grounding the source, and applying 12V and 6V to the select gate and the drain respectively, a cell is programmed to a different state. During programming, charge is transferred to the floating gate by hot-electron injection from the channel region, as shown in Figure 3(b). The typical NOR flash memory structure used in Intel device is shown in Figure 4.

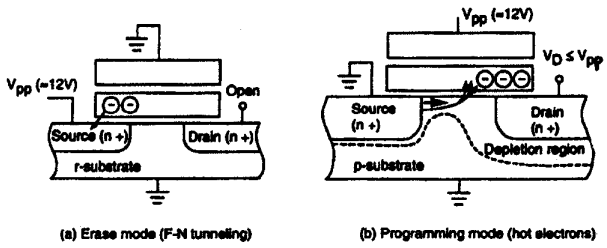

Figure 3. NOR cell Structure Used in the Intel Flash Memory

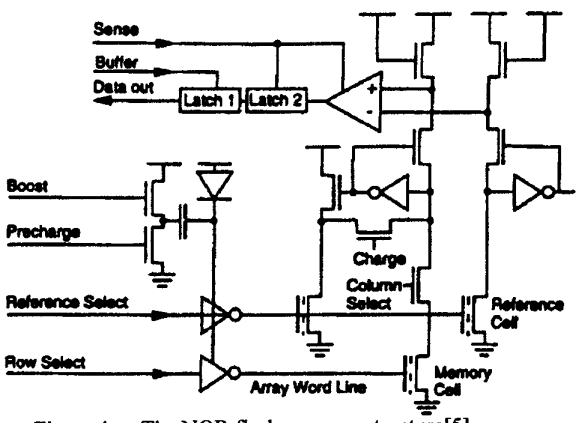

Figure 4. The NOR flash memory structure[5]

Table 1 compares important features of the Intel and Samsung devices. The Intel device can operate with a logic voltage of either 3.3V or 5V. Programming can be done at either V_{pp} of 12V or 5V. The internal charge pump is not used when V_{pp}=12V but it is automatically switched in when Vpp=5V. This feature of the Intel device was used to compare the effects of charge pump activation. The Samsung device uses only a 5V power supply; its charge pump is always activated.

Table 1. Features of the flash memories.

Device	Cell Structure	V_{dd}	V_{pp}	Charge Pump
Intel 28F016SV	NOR	5V/3.3V	12V/5V	Only with V_{pp}=5V
Samsung KM29N16000	NAND	5V	--	Always activated

III. Experimental Approach

Six devices of each manufacturer were irradiated with Co-60 at room temperature. Devices were irradiated at 25 rad(Si)/s with V_{pp}=5V and V_{dd}=5V. After irradiation, devices were taken out of radiation room and electrical measurements were made with an Advantest test system (T3342). Measurements between radiation levels were taken with three different voltage conditions; V_{dd}=3.3V, V_{pp}=5.0V; V_{dd}=3.3V, V_{pp}=12V; and V_{dd}=5.0V, V_{pp}=12V.

IV. Test Results

In the erase/write/read mode with V_{pp}=12V and V_{dd}=5V (no activation of charge pump), the Intel flash memory did not fail until 100 krad(Si) as shown in Figure 5. However, the Samsung device, which uses the charge pump to boost its internal supply Vpp to 20V during the erase/program mode, functionally failed at 10 krad(Si), an order of magnitude lower level. When the Intel devices were tested with V_{pp}=5V, activating the internal charge pump circuit, they failed at about 25 krad(Si) with V_{dd}=3.3V. These results clearly show that the charge pump plays a critical role in the total dose response.

Intel devices which use the NOR gate structure showed better total dose responses than the NAND gate structure used in the Samsung devices. The charge pump function affects device failure levels. Intel devices with V_{dd}=5V and V_{pp}=12V (no charge pump activated) operated satisfactorily at 50 krad(Si) but much lower level failure occurred when the charge pump was activated.

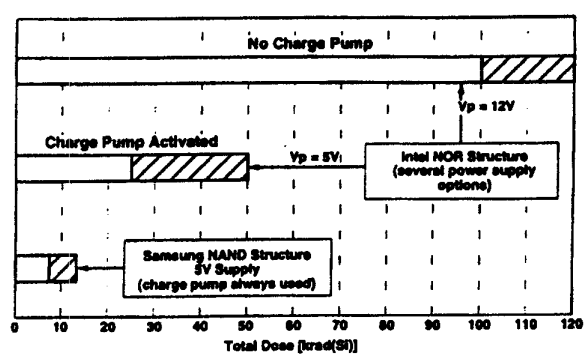

Figure 5. Total dose failure levels for flash memories in erase/write/read mode.

The charge pump also affected the time required to erase blocks of memory cells in the Intel devices. As shown in Figure 6, devices operating with V_{dd}=3.3V and V_{pp}=5V in erase/write/read mode required longer and longer time intervals to erase the whole memory. The erase time interval increased to 143 sec at 12 krad(Si), and actually exceeded 15 minutes at higher radiation levels – from 20 krad(Si) and up. There were significant variations between different units.

Devices with the charge pump inactive (V_{pp}=12V, V_{dd}=3.3V) showed no degradation in erase time up to 30 krad(Si).

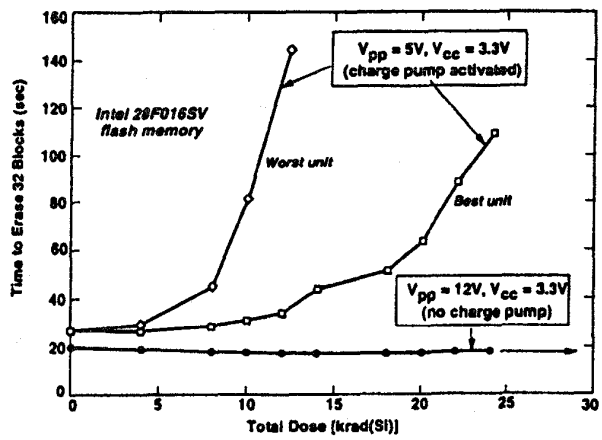

Figure 6. Time to erase with two different programming voltages for Intel devices.

Charge pump circuits share a basic design as shown in Figure 7. The following equations determine the common characteristics of charge pump:

$$V_{out} = n(V_{cc}-V_{diode})$$
$$Z_{out} = n/(CxF)$$

Where n = number of charge pump stages
C = capacitor size of each stage
F = clock rate

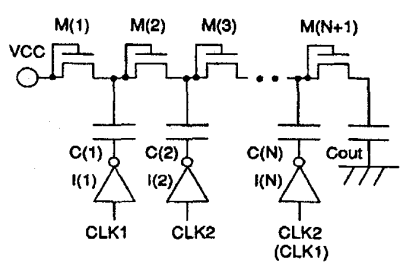

Figure 7. The Dickson charge pump circuit with MOS transfer transistor [6]

Erase time depends upon the electric field across the floating gate. Relatively small changes in the charge pump circuit will increase the time required to transfer charge to the floating gate. Table 2 summarizes the results of erase time for Intel devices (with and without charge pump activation) and Samsung devices (with charge pump activation) at various power supply voltages and total dose radiation levels. Power supply currents for both devices types were measured and the results are included in the table.

Table 2. Summary of erase time and supply current measurements at various total dose levels

Device	V_{dd}	I_{sb}	I_{sleep}	Erase Time	Total Dose Level
Intel 28F016SV w/ charge pump activated	3.3V 3.3V 5.0V	160uA	48uA	143sec 75 min	12 krad(Si) 24 krad(Si) 12 krad(Si)
Intel 28F016SV w/o charge pump activated	3.3V 5.0V	104uA	0.2uA	18sec	24 krad(Si)
Samsung KM29N1600 w/ charge pump activated	5.0V 5.0V	30uA 115uA		3.5sec	10 krad(Si) 12 krad(Si)

The stand-by current of the Intel devices showed insignificant degradation up to 24 krad(Si) and then it sharply increased in the region between 30 and 50 krad(Si) as shown in Figure 8. Functional failure was observed at 25 krad(Si) in the erase/write/read mode with V_{pp}=5V.

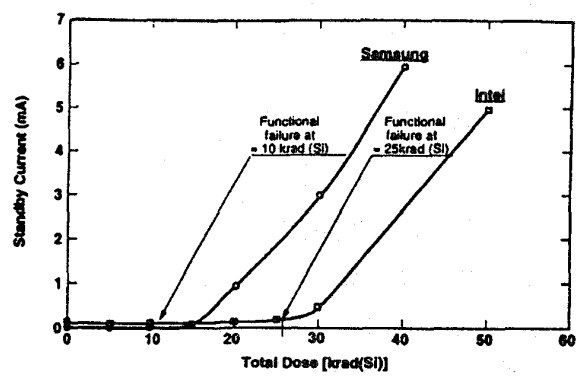

Figure 8. Stand-by current degradation for both Intel and Samsung flash memories

The Samsung devices showed a large increase in the stand-by current at 12-40 krad(Si). The devices failed functionally at about 10 krad(Si). The failure could be due to either threshold voltage changes in the NAND cell structures or charge pump degradation.

Supply current of Intel devices increased about 6 mA at 24 krad(Si) at which functional failure occurred. However, the Samsung devices showed much more degradation at lower total dose levels as shown in Figure 9. The current draw increased gradually to 17 mA at 24 krad(Si) although the most dramatic increases occur after functional failure at about 10 krad(Si). This is attributed to thickness of oxides. The oxide of the Samsung device was almost three times thicker than the Intel devices which is most likely the cause of the faster power increase of the Samsung.

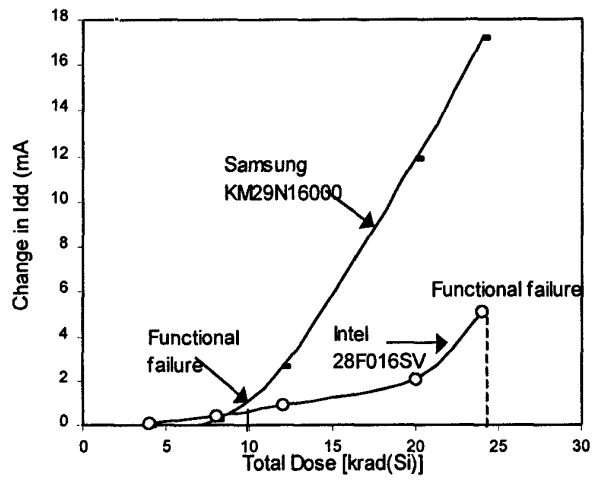

Figure 9. Supply current (I_{dd}) degradation of Intel and Samsung memories

The input leakage current of Intel devices showed larger degradation than Samsung devices. The degradation was about 2.5 time greater at 24 krad(Si) as shown in Figure 10. The Samsung devices did not showed any degradation up to the functional failure level of 10 krad(Si). The maximum specification limit is 10 μA for Samsung and 1 μA for Intel devices. Therefore, the Intel devices exceeded the specification limit at about 16 krad(Si) and functionally failed at 24 krad(Si). In contrast, the Samsung devices were well within the specification limit. However, it failed functionally at much lower level of 10 krad(Si).

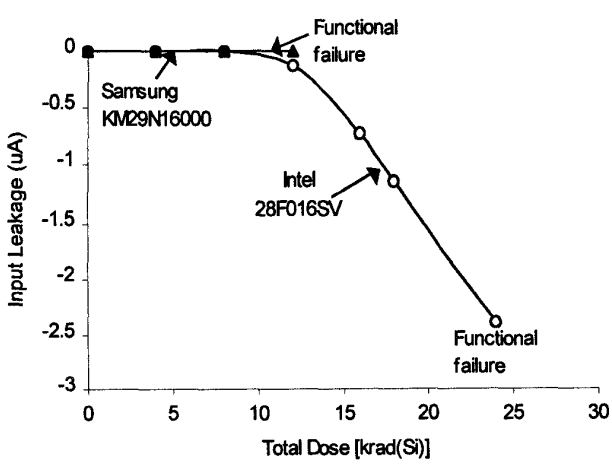

Figure 10. Input leakage degradation of Intel and Samsung devices

V. SUMMARY

This paper presents data on two flash memories with different internal cells. The results show that degradation of the charge pump, which is needed for writing and erasing, was important. One of the memory technology allowed selective operation of the charge pump, and it operated at much higher levels when the charge pump was not used. Although these results were from relatively recent technology, commercial flash memory technologies are evolving rapidly. Therefore, next-generation devices, such as multi-level flash memories, which have more complex structure and much smaller threshold voltages may have less radiation hardness.

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