IR DirectFET Performance Evaluation
Final Report

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Abstract

International Rectifier (IR) has developed DirectFET, a new method of packaging power MOSFETs. DirectFET packaging offers improved device thermal and electrical performance over conventional plastic SO-8 packaging. This study compared the static thermal and electrical performance of DirectFET packaged MOSFET devices against that of SO-8 and Toshiba High Efficiency (HE) devices.

As compared with SO-8 packaged devices, the DirectFET channeled up to 45% more drain current with up to only 20% more power dissipation. The Toshiba HE packaged devices exhibited electrical performance similar to DirectFET devices. The electrical parameter values of devices, whether packaged as DirectFETs, SO-8s or Toshiba HEs, remained stable through exposure to high temperature (up to 150C) soak and temperature cycling (-65C to +150C): the RdsON, Idss (leakage current) and Vth (threshold voltage) varied by +/- 3% or less of the initial measured values.

The DirectFET thermal test assemblies mounted with finned heat sinks exhibited junction-to-lead thermal resistance (Rj-l) 75% lower than comparable SO-8 assemblies. The DirectFET packaging significantly reduced the junction-to-ambient thermal resistance (Rj-a) by as much as 23%. Bonding a finned heat sink to the top of the DirectFETs further reduced the thermal resistances by about another 5 to 10%. On average, the devices using DirectFET packaging could dissipate about 23 percent more power while simultaneously attaining a 70 percent reduction in Rj-l and a 21 percent reduction in Rj-a. On average, the Toshiba HE device delivers a thermal performance similar to the DirectFET devices. The Toshiba HE delivers a 12 and 62 percent improvement relative to SO-8s in the thermal resistances, Rj-a and Rj-l, respectively. However, because Toshiba HE packages are plastic encapsulated, heat sink options are limited.

Increasing pad and circuitry surface area by 20% yields a nearly identical decrease in thermal resistance. However, a greater than 500 percent increase in surface area only results in a 40% decrease in thermal resistance. It is then more effective to use some form of heat sinking, such as heat pipes or cold plates, to reduce thermal resistances.

Acknowlegements

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Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

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1.0 Introduction

In 2003, International Rectifier (IR) introduced a new form of packaging for its MOSFET devices known as DirectFET packaging (Figure 1). By routing the drain through the bottom of the die and connecting this to a metal lid, this package design greatly enhances the device's ability to dissipate heat: the lid can be readily heat sinked in a variety of ways. The enhanced thermal performance translates into more efficient electrical performance, lower power consumption and longer working life of DirectFET packaged devices.

Figure 1 . International Rectifier DirectFET MOSFET Packaging

The design also presents additional advantages. The complete elimination of wire bonds and package leads thanks to the "flip chip" nature of this assembly eliminates most of the parasitic inductances which are common with SO-8 packaged devices. The minimal package inductance allows one to use these devices in high frequency, high power switching applications. The improved efficiency, performance and small form factor of DirectFET devices then enables higher density designs for DC/DC converters and other applications.

Given the advantages described above, the devices show great potential in space applications where power efficiency, device performance and payload weight directly affect mission life. Specifically, the incorporation of these devices into spacecraft electronics could extend the battery life and the duration of deep space missions and missions to Mars. Consequently, the DirectFET technology has aroused considerable interest at the Jet Propulsion Laboratory (JPL) and the NEPP community. Partnering with IR and Stellar Microelectronics (SMI), JPL has initiated a multi-phase study to evaluate the DirectFET technology.

In this initial phase of the study, SMI has compared the electrical and thermal performance of the DirectFET packaged MOSFETs versus those packaged in standard molded SO-8 packages or those packaged using Toshiba's own higher efficiency packaging method. The results and conclusions of electrical and thermal measurements on all three types of packaging are detailed herein.

2.0 Electrical & Environmental Test Evaluation

2.1 Experimental

2.1.1 Devices and Test Assemblies

2.1.1.1 Test Devices

A set of DirectFET and SO-8 packaged device types were obtained from IR and two Toshiba High Efficiency Packaged device types were from Toshiba. Table I lists the devices and their electrical specifications. Additionally, IR provided "dummy" DirectFET MX outline packages. In these dummy devices, the die is replaced with a copper slug. This device can be used to baseline the contribution of the circuit board and device packaging to the measured electrical resistance of the circuit board assemblies.

The original intent of this study was to compare the thermal and electrical performance of a set of DirectFET and SO-8 devices. In order to do this comparison, the die mounted in the two different styles of package must be of the same generation, size and device characteristics. Unfortunately, perhaps due to an oversight by IR, most of the device types supplied by IR are not strictly comparable at least from the perspective of electrical performance. The Toshiba devices likewise are not strictly comparable to the IR devices.

There are only two device pairings that can be properly compared: the IRF6611 / IRF7832 pair and the IRF6635 / IRF7852. For all the other devices, an approximate comparison will be attempted.

2.1.1.2 Test PWB Assemblies

The devices were mounted onto two different circuit board designs, one for DirectFET and the other for SO-8 and Toshiba packaging, as shown in Figure 2. The board designs were obtained from IR and fabricated using standard epoxy FR-4 laminate materials, 0.5 oz. copper with ENIG surface finish.

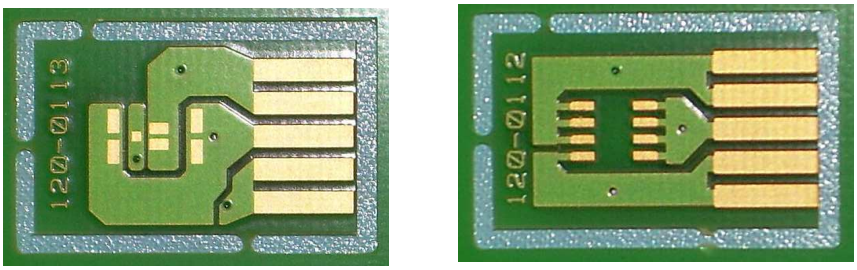

Figure 2 . Electronic Test Circuit Boards

The test assemblies were fabricated using automated assembly equipment and lead-tin eutectic solder paste. The finished assemblies are depicted in Figure 3. X-ray inspection of the DirectFET assemblies revealed significant voiding in the source and gate solder joints and evidence of solder balls entrapped under the devices (see Figure 4). This suggests that the solder reflow profile requires fur-

ther optimization. However, with the exception of the electrical resistance, the voiding should have minimal effect on the measured device electrical parameters. The effect of voiding on the measured resistance can be subtracted using the averaged data obtained from dummy DirectFET assemblies.

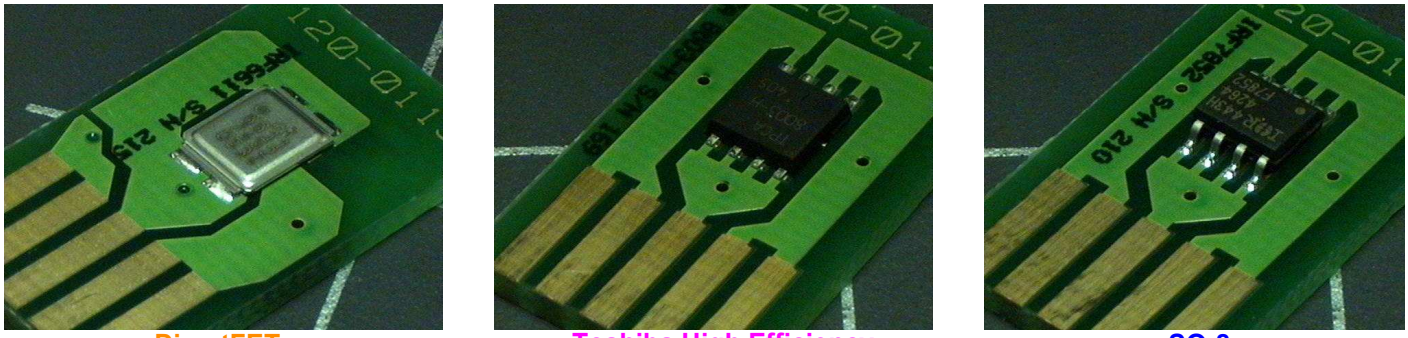

Figure 3 . Electronic Test Assemblies and Three Package Types

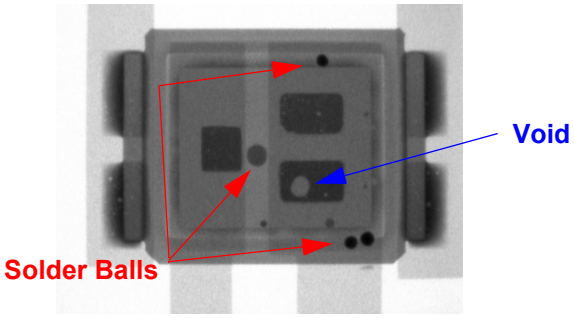

Figure 4 . X-Ray Inspection of DirectFET Assembly: Defects

2.1.2 Electrical and Environmental Testing

A sequence of electrical and environmental tests were performed on the electrical test assemblies as outlined in Table II. An automatic FET Test system Model 9400 was programmed to measure Rds On, Ids (leakage current) and Vth (threshold voltage) of each device in accordance with the test conditions outlined in the device specifications. A Blue M nitrogen purged batch oven was used for all temperature soak conditioning. A Ransco Temperature Cycle Chamber Model 7102 was used for temperature cycle conditioning.

For each device type for IR, a set of 5 assemblies were set aside as references. Because of limited numbers of test parts, only two toshiba assemblies of each device type were set aside as references. The reference samples were tested alongside the test samples at each test point in the sequence.

Table I: Devices Used in Study

Device Model Number		Package Type	Max. RdsOn 1 Specification (mOhm)	Max. RdsOn 2 Specification (mOhm)	Max. RdsOn 3 Specification (mOhm)	Max. Ids 1 Specification (nA)	Max. Ids 2 Specification (nA)	Max. Vth Specification (Volt)
Directly Comparable Devices								
Identical Die	IRF7832	SO8	**4.0** *(Vgs= 10V; Id= 20A)*	**4.8** *(Vgs= 4.5V; Id= 20A)*		**1,000** *(Vds= 24V; Vgs= 0V)*		**2.32** *(Vds=Vgs; Id=250µA)*
	IRF6611	DirectFET	**2.6** *(Vgs= 10V; Id= 27A)*	**3.4** *(Vgs= 4.5V; Id= 16A)*		**1,000** *(Vds= 24V; Vgs= 0V)*		**2.25** *(Vds=Vgs; Id=250µA)*
Identical Die	IRF7852	SO8	**3.4** *(Vgs= 10V; Id= 22A)*	**4.1** *(Vgs= 4.5V; Id= 18A)*		**1,000** *(Vds= 24V; Vgs= 0V)*		**2.35** *(Vds=Vgs; Id=250µA)*
	IRF6635	DirectFET	**1.8** *(Vgs= 10V; Id= 32A)*	**2.4** *(Vgs= 4.5V; Id= 25A)*		**5,000** *(Vds= 24V; Vgs= 0V)*		**2.35** *(Vds=Vgs; Id=250µA)*
Other Devices								
IRF6604		DirectFET	**11.5** *(Vgs= 7V; Id= 12A)*	**13** *(Vgs= 4.5V; Id= 9.6A)*		**30,000** *(Vds= 24V; Vgs= 0V)*	**50,000** *(Vds= 30V; Vgs= 0V)*	**2.1** *(Vds=Vgs; Id=250µA)*
IRF6644		DirectFET	**13** *(Vgs= 10V; Id= 10.3A)*			**20,000** *(Vds= 100V; Vgs= 0V)*		**4.8** *(Vds=Vgs; Id=150µA)*
IRF7455		SO8	**7.5** *(Vgs= 10V; Id= 15A)*	**9** *(Vgs= 4.5V; Id= 12A)*	**20** *(Vgs= 2.8V; Id= 3.5A)*	**20,000** *(Vds= 24V; Vgs= 0V)*		**2.0** *(Vds=Vgs; Id=250µA)*
IRF7490		SO8	**39** *(Vgs= 10V; Id= 3.2A)*			**20,000** *(Vds= 100V; Vgs= 0V)*		**4.0** *(Vds=Vgs; Id=250µA)*
8003-H		Toshiba HE	**6.6** *(Vgs= 10V; Id= 18A)*	**9.5** *(Vgs= 4.5V; Id= 18A)*		**10,000** *(Vds= 30V; Vgs= 0V)*		**2.3** *(Vds= 10V; Id=1mA)*
8004-H		Toshiba HE	**4.6** *(Vgs= 10V; Id= 20A)*	**6.2** *(Vgs= 4.5V; Id= 20A)*		**10,000** *(Vds= 30V; Vgs= 0V)*		**2.3** *(Vds= 10V; Id=1mA)*

Note: Test Parameter settings are noted in italics beneath each specification value.

Table II: Sequence of Electrical and Environmental Tests

Test Step	Test Description	Test Conditions
1	Initial Electrical	25C Electrical: Measure RdsOn, Ids, and Vth
2	Heat Soak	24 hour @ 125C
3	Temperature Cycle	MIL-STD-883, Method 1019, Condition B, 10 Cycles, -55C to +125C
4	Interim Electrical 1	25C Electrical: Measure RdsOn, Ids, and Vth
5	Heat Soak	24 hour @ 150C
6	Temperature Cycle	MIL-STD-883, Method 1019, Condition B, 10 Cycles, -65C to +150C
7	Interim Electrical 2	25C Electrical: Measure RdsOn, Ids, and Vth
8	Heat Soak	24 hour @ 150C
9	Temperature Cycle	MIL-STD-883, Method 1019, Condition B, 10 Cycles, -65C to +150C
10	Interim Electrical 3	25C Electrical: Measure RdsOn, Ids, and Vth
11	Temperature Cycle	MIL-STD-883, Method 1019, Condition B, 100 Cycles, -65C to +150C
12	Final Electrical	25C Electrical: Measure RdsOn, Ids, and Vth

2.2 Results and Discussion

2.2.1 Initial Electrical

2.2.1.1 General

The initial electrical test results for each device are presented in Table III. The specification maximum values for each device type are listed. A Cpk value was computed using the specification values and the measured Rds On and Vth values. No Cpk was calculated for Ids, since in all cases the measured values were orders of magnitude below the specification maximum. The Cpk gives a measure of how well within specification the measured values are as well as the variance in the measured values from part to part. A Cpk value of 1 represents a 3 sigma part (i.e., there are 3 standard deviations between the specification maximum and the mean measured value) and a Cpk of 2 represents a 6 sigma part. In general, the larger the Cpk, the more within specification and the more consistent the part measured values are.

With the exception of RdsOn, all measured Ids and Vth values were well within specification and were very consistent part to part. The RdsOn values, however, measured mostly on the high end, many of which exceeded the maximum specification limits. This was especially apparent with the SO-8 devices and with RdsOn specification limits that were on the order of 5 mOhms or less.

2.2.1.2 Rds On Measurement Issues

The apparent failure to meet RdsOn specification requirements is caused by the resistance contribution of the package itself plus those from the solder joints and

the circuit boards. This resistance contribution was found to be substantial. The RdsOn values of a series of 10 DirectFET MX dummy assemblies were measured using the test conditions for IRF6611 and IRF6635 and were found to be about 0.8 to 0.9 mOhms. If this additional resistance is subtracted from the measured values for the IRF6611 and IRF6635, these parts then easily pass the test: Cpk values rise from zero or near zero to between 7 and 11.

Only the RdsOn values for the IRF6611 and IRF6635 were corrected, since equivalent dummy DirectFET packages were obtained only for these parts. The IRF6604 and IRF6644 are MN and MQ outline DirectFET packages, respectively. Consequently, the resistance measurement would be different for these packages though it is likely to be of the same order of magnitude. Likewise, no dummy packages were available for the SO-8 and Toshiba style assemblies and no correction factor could be determined. However, it is likely that they too would have resistances on the order of 1 mOhm or greater. Consequently, the corrected RdsOn values would then be well within specification.

2.2.1.3 Device Performance: IRF6611/6635 (DirectFET) versus IRF7832/7852 (SO-8)

The power dissipation of the devices was calculated based on the average RdsOn measurements and the applied drain current. The power dissipation is plotted versus applied drain current in Figure 5. These results overstate the amount of power dissipation that is due to just device packaging: the calculations do not factor in the resistance contribution from the solder joints and the board itself, since no correction factor could be measured for the SO-8 packaged devices.

The power performance advantage, nevertheless, of the DirectFET is clearly shown in the figure: one obtains between 35 percent and 45 percent more current flow in the DirectFET devices with only a nominal (between 0 percent and 24 percent) increase in power dissipation. The larger interconnect areas, the shorter current pathways, and the better thermal dissipation of the DirectFET package no doubt serve to reduce device power dissipation relative to the SO-8 package.

2.2.1.4 General Device Performance: SO-8 versus Toshiba HE and DirectFET

It is not possible to make a fair and accurate comparison between the electrical performance of the other devices with respect to each other. Nonetheless, an attempt was made to compare the power dissipation of the various devices based upon their measured RdsOn values. In Figure 6, the power dissipation of all the tested devices is plotted versus the drain current.

The IRF6611 and IRF6635 outperform all the other devices in terms of current output versus power dissipated. All other devices dissipated more power while channeling a smaller drain current.The Toshiba devices exhibited a performance comparable to that of the IRF 7832 and IRF 7852 SO-8 devices. This type of comparison, however, does not separate the effects of the device packaging from those of the device (die) characteristics. Rather these are lumped together and it is difficult to conclude from this that one type of packaging scheme is better than another.

Table III: Initial Electrical Test: Measurement Results

Device Type (Package Type)	Sample Qty[B]	RdsOn 1		RdsOn 2		RdsOn 3		Ids 1		Ids 2		Vth	
		Res. (mOhm)	Spec. (mOhm) / Cpk	Res. (mOhm)	Spec. (mOhm) / Cpk	Res. (mOhm)	Spec. (mOhm) / Cpk	Current (nA)	Spec. (nA)	Current (nA)	Spec. (nA)	Voltage (Volt)	Spec. (Volt) / Cpk
IRF6604 (DF)	20	8.909 ± 0.287	11.5 / 3.00	10.379 ± 0.290	13 / 4.76			4.758 ± 1.265	30,000	19.367 ± 6.940	50,000	1.657 ± 0.016	2.1 / 9.18
IRF6611 (DF)	20	1.719 ± 0.041[A]	2.6[A] / 7.24	2.404 ± 0.052[A]	3.4[A] / 6.33			6.293 ± 0.568	1,000			1.885 ± 0.011	2.25 / 11.94
IRF6635 (DF)	20	1.233 ± 0.017[A]	1.8[A] / 10.86	1.692 ± 0.021[A]	2.4[A] / 11.36			4.531 ± 0.376	5,000			1.778 ± 0.011	2.35 / 18.15
IRF6644 (DF)	20	12.152 ± 0.148	13 / 1.90					7.123 ± 1.812	20,000			3.767 ± 0.138	4.8 / 2.49
IRF7455 (SO8)	20	**8.687 ± 0.112**	**7.5 / 0**	**9.653 ± 0.109**	**9 / 0**	11.477 ± 0.103	20 / 27.65	0.744 ± 1.16	20,000			1.280 ± 0.007	2 / 33.44
IRF7490 (SO8)	20	33.705 ± 0.397	39 / 4.45					2.125 ± 0.219	20,000			3.078 ± 0.102	4 / 3.012
IRF7832 (SO8)	20	**4.410 ± 0.137**	**4 / 0**	**5.011 ± 0.130**	**4.8 / 0**			59.62 ± 12.37	1,000			1.654 ± 0.017	2.32 / 12.82
IRF7852 (SO8)	20	**4.300 ± 0.060**	**3.4 / 0**	**5.000 ± 0.062**	**4.1 / 0**			15.46 ± 3.473	1,000			1.824 ± 0.0135	2.35 / 12.99
8003-H (THE)	10	8.898 ± 0.120	9.5 / 1.66	**6.570 ± 0.070**	**6.6 / 0**			4.476 ± 1.100	10,000			2.020 ± 0.044	2.35 / 2.51
8004-H (THE)	10	**6.267 ± 0.212**	**6.2 / 0**	**4.679 ± 0.093**	**4.6 / 0**			6.925 ± 1.899	10,000			1.886 ± 0.078	2.3 / 1.77

[A] These values for RdsOn have be corrected to account for the approximately 0.9 mOhm contribution from the package and assembly resistances.

[B] In addition to the test samples, a set of 5 units of each device type were set aside as reference samples; the reference samples were not subjected to heat soak or temperature cycling.

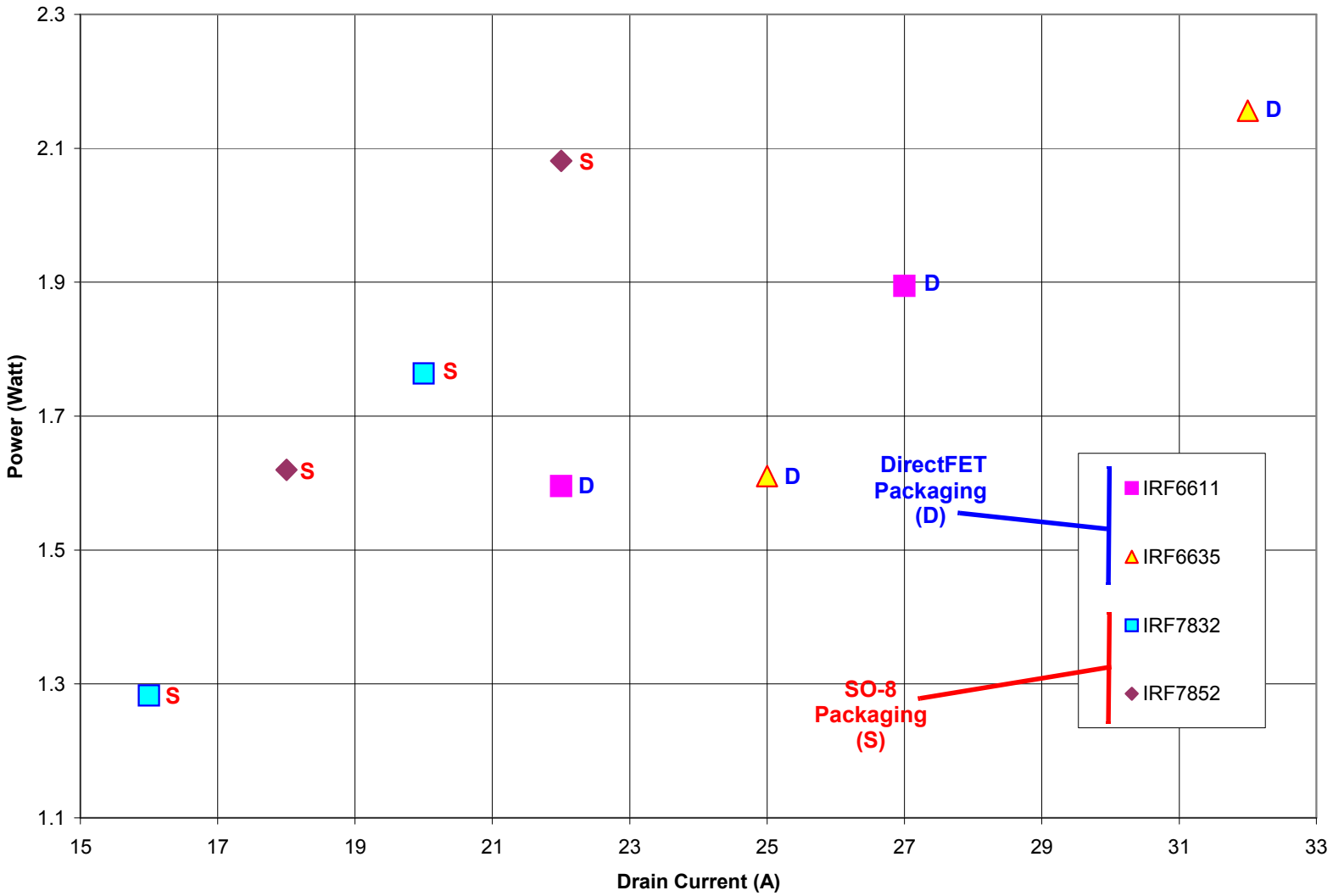

Figure 5 . Device Power Dissipation versus Drain Current (RdsOn Tests): IRF6611, IRF6635 versus IRF7832, IRF7852

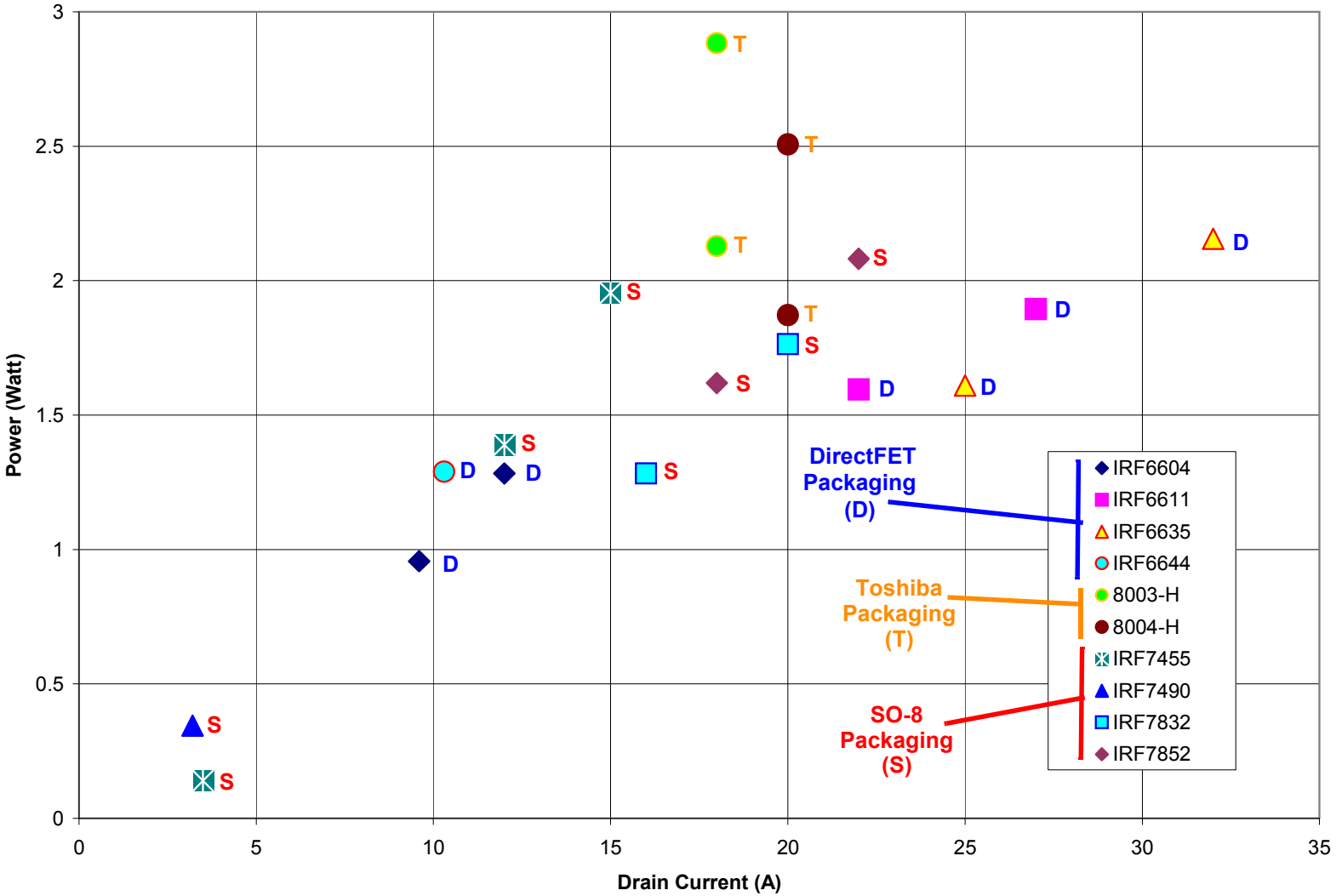

Figure 6 . Device Power Dissipation versus Drain Current (RdsOn Tests): All Devices

2.2.2 Environmental Testing

All assemblies listed in Table I were subjected to the series of environmental tests described in Table II and the values of the electrical parameters were measured. The percent variation of the measured RdsOn and Vth relative to the mean value measured at initial electrical are plotted in Figures 7 and 8. The Ids values were not plotted since these were so far below (on the order of 0.01 percent) of the maximum specifications and they did not appreciably change over the course of testing.

The mean values of the RdsON and Vth did not vary by more than +/- 3 percent over the duration of the tests. The values remained very stable and well within specification limits. Additionally, part to part variance did not appreciably increase either over the duration of the tests. All devices, DirectFET, SO-8 and Toshiba packaged parts, displayed consistent performance largely unaffected by extended heat exposure and temperature cycling.

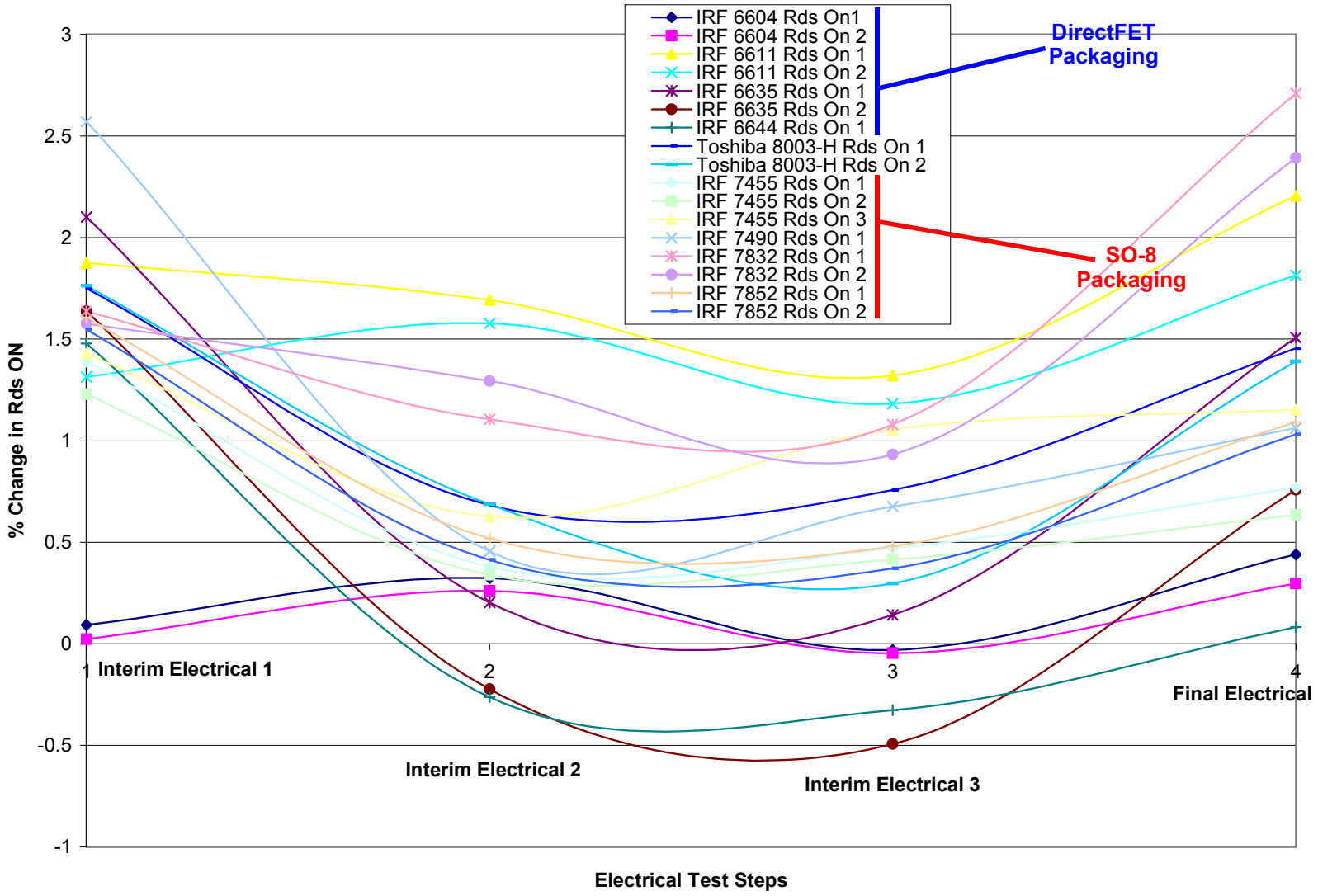

Figure 7 . Percent Shift in RdsOn Values Relative to Initial Electrical Measurement

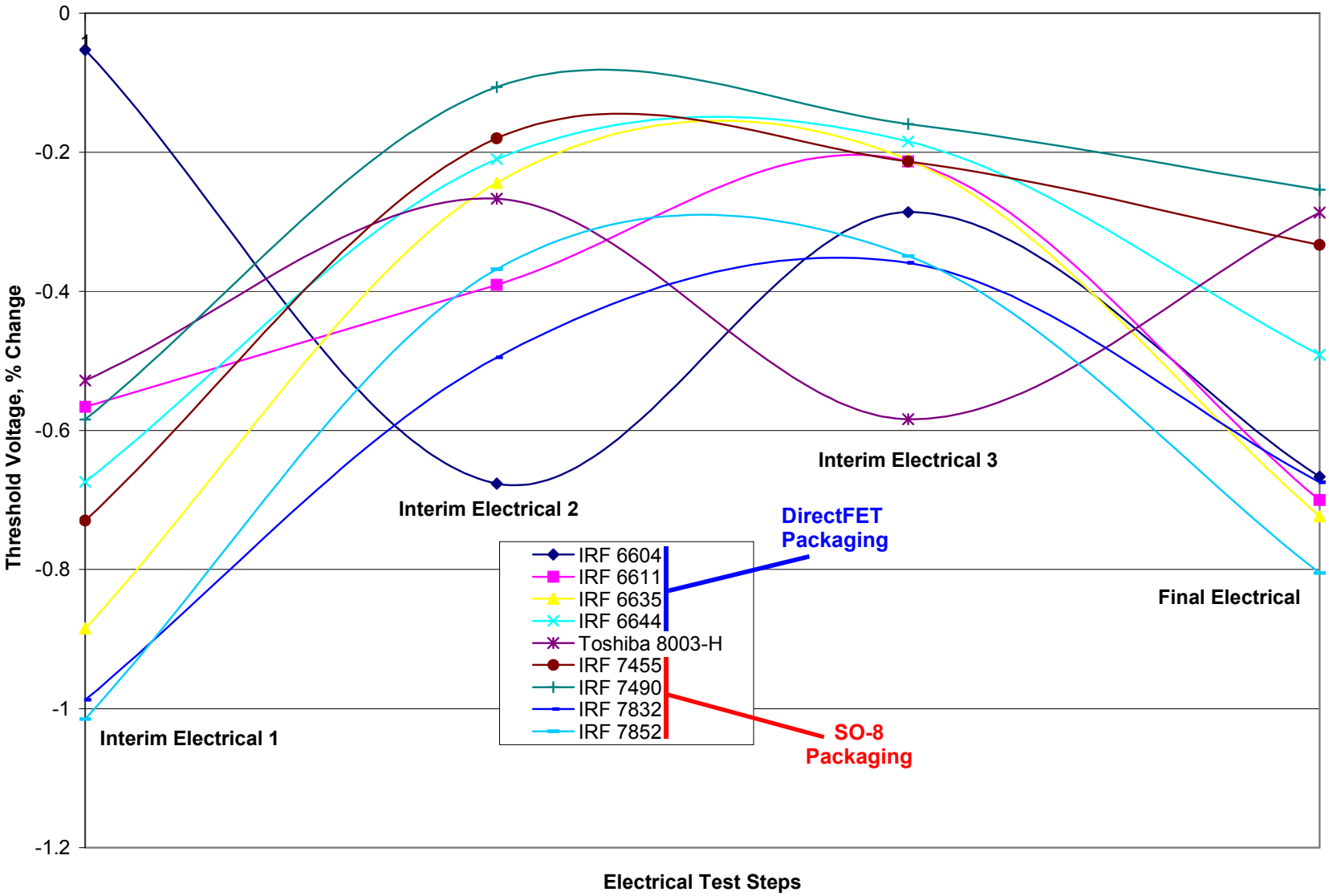

Figure 8 . Percent Shift in Voltage Threshold (Vth) Values Relative to Initial Electrical Measurement

3.0 Thermal Resistance Test Evaluation

3.1 Experimental

3.1.1 Devices and Test Assemblies

The thermal test board design was obtained from IR as shown in Figure 9. The boards were designed with three different sets of DirectFET and SO-8 pad configurations (see Figure 10): “Heavy” copper, “Medium” copper, and “Minimum” copper. The amount of copper (i.e., the surface area of the traces) connected to gate, source and especially the drain pads was varied from one configuration to the next. The boards then allow one to evaluate the effect of heat dissipation through circuit board leads on device thermal performance. The boards were fabricated using standard epoxy FR-4 laminate materials, 0.5 oz. copper with ENIG surface finish.

The same set of test devices (three of each type) from IR and Toshiba (see Table I) were surface mounted onto thermal test boards (see Figure 9). In the interest of minimizing the number of test samples, devices were only mounted on the medium copper pad configuration location. The medium copper configuration represents a realistic compromise, maximizing pad surface area for heat dissipation while minimizing package outline on the circuit board.

Two additional board assemblies (Figure 11) were fabricated with IRF 6611 and IRF 6635 DirectFET devices mounted on the heavy and minimum copper locations in addition to the medium copper location. Heat sinks (16 pin DIP finned heat sinks) were bonded on top of all the devices as shown in Figure 11 using B-tech TM-40 thermoplastic film adhesive (0.004 inch thick, Thermal Conductivity > 700 W/mK). The purpose of these assemblies was to measure the effect of the heat sink on the thermal performance of the DirectFET device. The two boards were also used for measuring the effect of the quantity of copper on the devices’ thermal performance.

No heat sinks were added to the SO-8 devices as there was no advantage in doing so. Heat in SO-8 devices is principally dissipated through the lead frame and not through the package body as this is an insulative plastic. This is one of the key advantages of the DirectFET design over the conventional SO-8: heat dissipation can be greatly enhanced by heat sinking the body of the DirectFET package, a strategy that is ineffectual with the SO-8.

3.1.2 Thermal Resistance Testing

The thermal resistance testing was performed by Analysis Tech (Wakefield, MA). Analysis Tech (AT) measured two thermal resistances for each device type: Junction-to-Ambient and Junction-to-Lead. The latter resistance used a thermocouple soldered to one of the device leads in order to obtain the junction to lead resistance. All measurements were carried out in still air at ambient (~ 25C) temperatures.

An Analysis Tech Phase 11 Thermal Analyzer was used for all measurements. Measurements were performed according to the guidelines established in the JEDEC JESD24-3 standard. The MOSFET diode junction was used as the reference. Three devices for each device type were used for calibrating each device (K-Factor and intercept). The calibrations were carried out in a constant temperature bath.

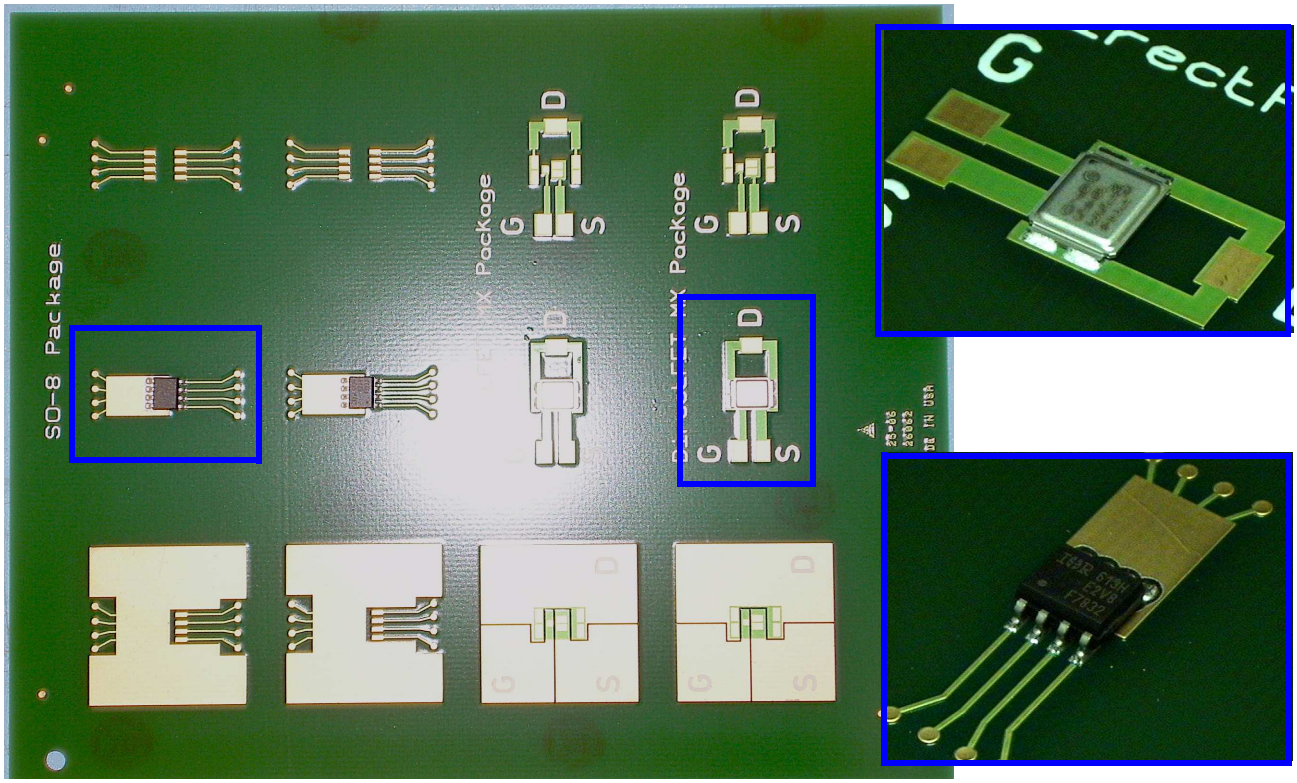

Figure 9 . Thermal Resistance Board Assembly

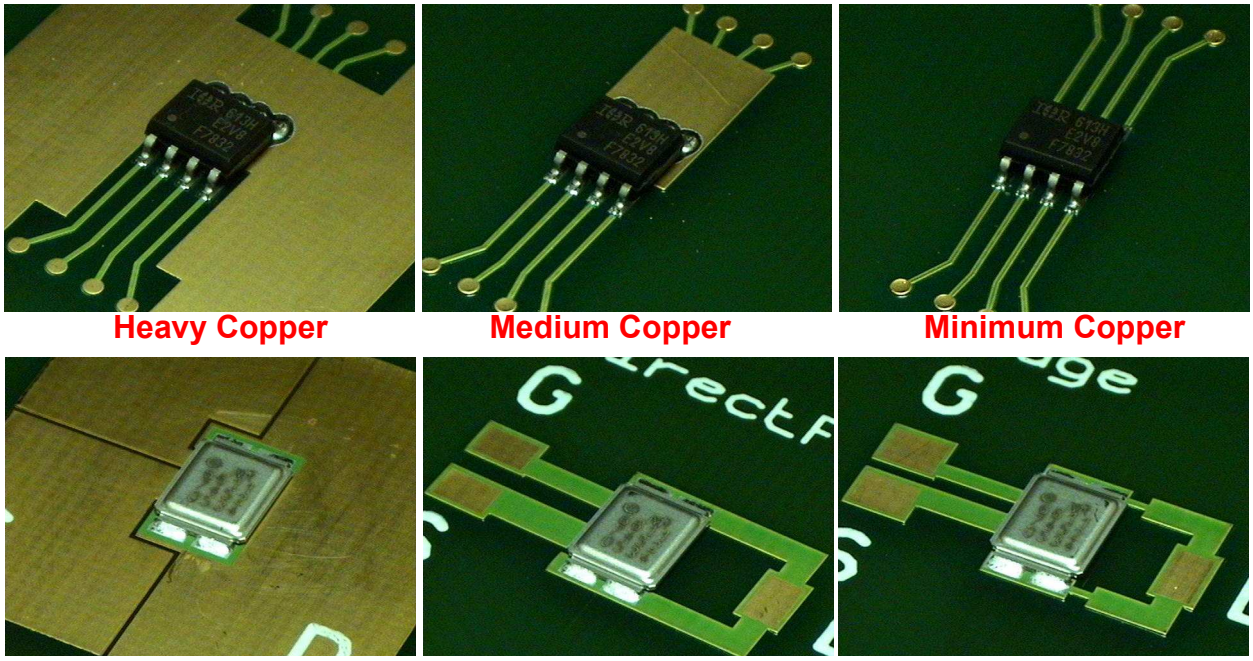

Figure 10 . Thermal Resistance Board: Three Pad Configurations

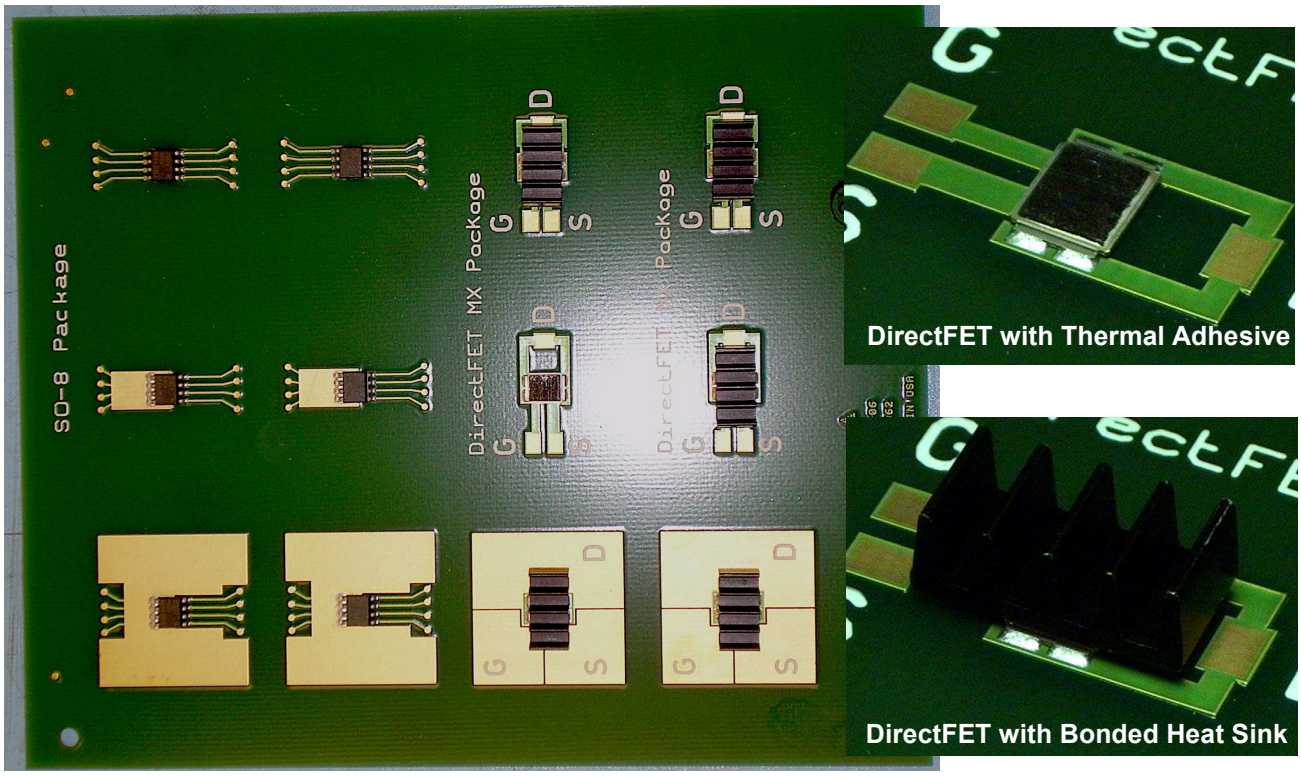

Figure 11 . Thermal Resistance Board Assembly with Heat Sinks

Thermal resistance measurements were made on three of each device type. The IRF 6644 devices, unfortunately, yielded no data because they would not power up. There was an open circuit condition with these assemblies, most likely at the solder joint.

3.2 Results and Discussion

3.2.1 Effect of Packaging Type

3.2.1.1 DirectFET versus SO-8: IRF6611/IRF6635 vs. IRF7832/IRF7852

The majority of the heat generated by the MOSFET devices is dissipated through the Drain lead. In the SO-8 package, the drain lead is connected to the package lead frame. In the DirectFET package, the Drain lead is connected to a large lid, that increases by about 120% the surface area (relative to SO-8 lead frame) over which heat may be dissipated. Consequently, package thermal resistance is significantly reduced.

The fact that the majority of the MOSFET heat is dissipated through a thermally conductive top (lid) in the DirectFET package, allows one to easily heat sink the devices to further enhance the heat dissipation. In contrast adding a heat sink to the body of an SO-8 yields no such advantage since the body is thermally insulative.

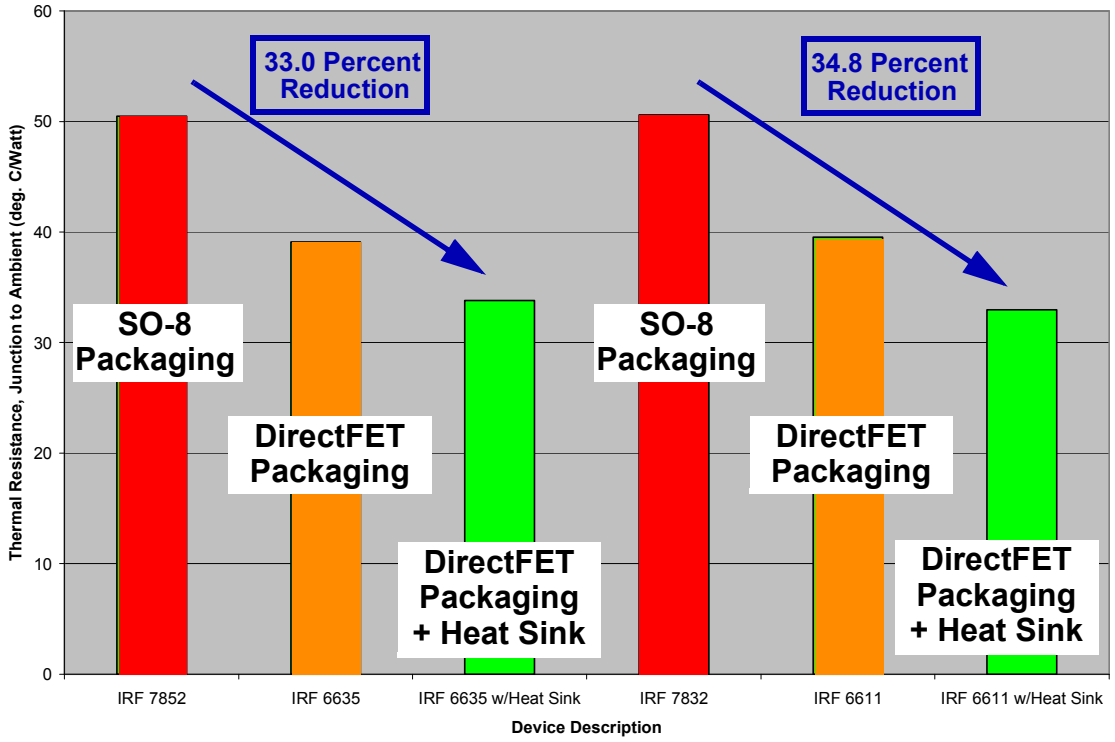

Figure 12 . Effect of Package Type on Thermal Resistance, Junction to Ambient: DirectFET versus SO-8

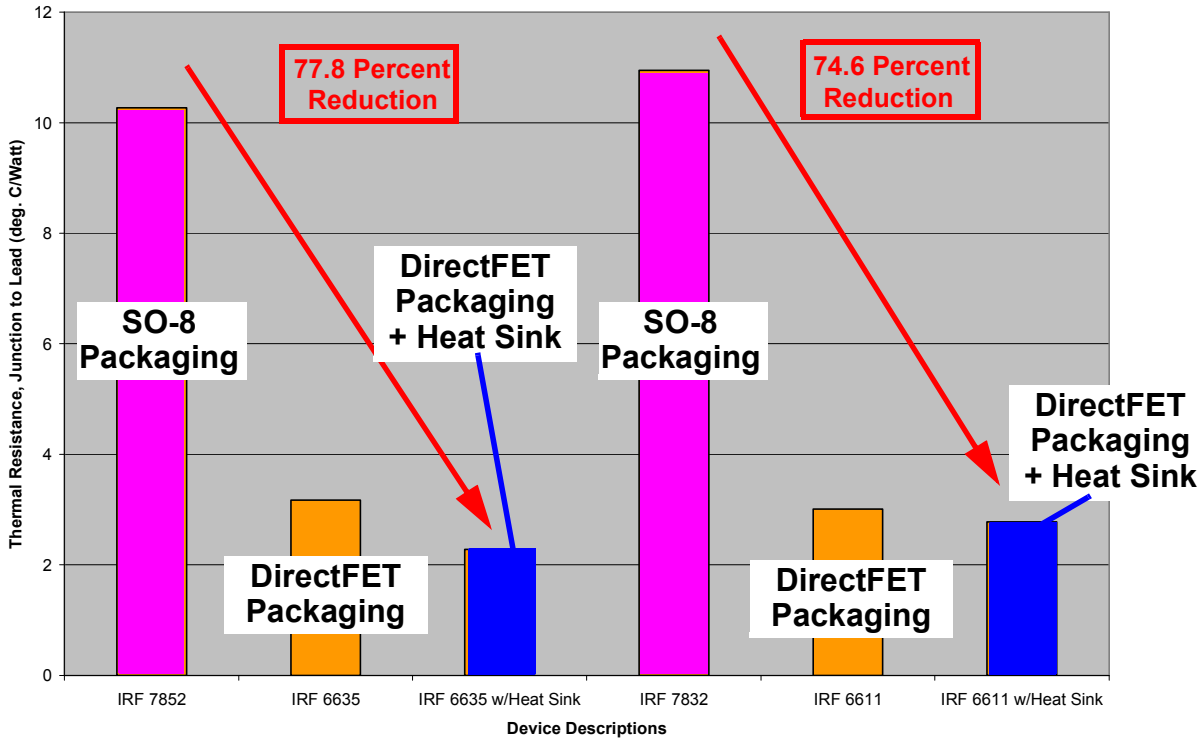

Figure 13 . Effect of Package Type on Thermal Resistance, Junction to Lead: DirectFET versus SO-8

Finned heat sinks in this evaluation were used only for a relative comparison of the thermal drop between the two types of packaging. Conductive cooling, such as with heat pipes or cold plates, could also be employed in the actual applications, especially in space applications where convective cooling cannot be used.

Figure 12 graphs the average Thermal Resistance, Junction to Ambient (Rj-a) of the heat sinked and un-heat sinked IRF 6611, IRF 6635 DirectFETs versus the IRF 7832, IRF 7852 SO-8 devices. The DirectFET packaging significantly reduced the thermal resistance of the devices, by as much as 23%. Adding a heat sink to the top of the DirectFETs further reduced the thermal resistance by about another 10%. Examining the thermal resistance of Junction to Lead (Rj-l), the effect of enhanced thermal dissipation was even more dramatic Figure 13 shows the thermal resistance drops by about 70% relative to the SO-8 packages. The addition of a heat sink on these devices results in a 75% drop in thermal resistance relativer to the comparable SO-8 device. The effect of the heat sink would likely be even greater had there been a constant airflow across the parts rather than simply still air.

The thermal resistance of junction to lead is substantially less than that of Junction to air. This reflects the fact that the resistance pathway is much shorter when measuring junction to lead versus junction to ambient: there is less distance for heat to travel from junction to the edge of the device lead versus the ambient air surrounding the board.

3.2.1.2 DirectFET versus SO-8 Devices: General Discussion

Table IV summarizes power dissipation versus thermal resistance and junction temperature data for each device type.

On average, the devices using DirectFET packaging could dissipate about 23 percent more power while simultaneously attaining a 70 percent reduction in Rj-l and a 21 percent reduction in Rj-a. The substantial reduction in Rj-l can be attributed to the nearly 120 percent increase in the lead frame area from DirectFET relative to SO-8: the larger surface area conducts heat more rapidly and effectively away from the MOSFET. The reduction in Rj-a is attributed to the increased surface area of drain and source leads and corresponding circuit board pads. The SO-8 devices must dissipate heat through the relatively small lead frame, through a series (a quantity between 14 and 21) of 0.001 inch wires connecting to the die source pads, and then through the narrow package leads to the board. In contrast, the DirectFET heat dissipation pathway is more direct and offers a greater surface area for more effective heat transfer.

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Table IV: Device Dimensions and Thermal Performance

Device	Package Type	Drain Lead Area ($inch^2$)	Drain+Source Lead Area ($inch^2$)	Lead Frame Area ($inch^2$)	Power Dissipated (Watt)	Thermal Resistance Junction to Air (deg. C/Watt)	Thermal Resistance Junction to Lead (deg. C/Watt)
8003-H	Toshiba HE	0.01216	Unknown	0.02571	1.850	44.98	4.13
8004-H	Toshiba HE	0.01851	Unknown		2.032	42.94	3.05
7455	SO-8	0.01508	0.01509	0.02141	1.806	52.23	11.98
7490	SO-8	0.01496	0.01497		1.794	52.48	11.35
7832	SO-8	0.01762	.0.01764		1.797	50.59	10.95
7852	SO-8	0.01827	0.01829		1.798	50.48	10.27
6604	Direct-FET	0.00905	0.01034	0.04683	2.180	42.97	3.54
6611	Direct-FET	0.01920	0.02447		2.331	39.53	3.01
6635	Direct-FET	0.02354	0.02882		2.154	39.11	3.17

3.2.1.3 DirectFET and SO-8 versus Toshiba HE Devices: General Discussion

Table IV also summarizes the data for the Toshiba High Efficiency packaged devices. On average, the high efficiency device delivers a thermal performance similar to the DirectFET devices. If one compares the thermal resistance of the Toshiba 8003-H to the average of the SO-8 devices, one sees that the Toshiba package delivers a 12 and 62 percent improvement in the thermal resistances, Rj-a and Rj-l, respectively. The high efficiency package achieves this by enlarging the lead frame (drain lead) area and by allowing one to solder and to directly heat sink this to the PWB.

The 8004-H device delivers thermal performance that is within +/- 6 percent of that obtained on average from the three DirectFET type devices. The Toshiba package design offers a shorter pathway for heat dissipation than does the DirectFET, which may explain its low thermal resistance in spite of having a 45 percent smaller lead frame (drain lead) surface area. Additionally, the use of a metal ribbon to connect the source pads to the lead frame may also enhance its performanceThe Toshiba high efficiency package, however, cannot be as efficiently heat sinked as can the DirectFETs. As with the SO-8, the Toshiba package is a molded plastic package design and it acts as a thermal barrier. Consequently, heat sinking, other than adding thermal vias under the drain and source pads, is ineffective. In contrast, the DirectFET package can both be heat sinked from the top of the package body and also by adding thermal vias into the PWB design.

3.2.1.4 Effect of the Amount of Copper Circuitry

Figure 14 shows the effect of the amount of copper circuitry on the thermal impedance, junction to ambient. The PWB circuitry provides additional pathways via heat conduction for heat dissipation. Consequently, a 20 percent increase in pad and circuitry surface area (medium copper configuration relative to minimum configuration) yields a nearly identical decrease in thermal resistance. Yet, this approach has its limitations as can be seen by comparing the heat resistance for the heavy copper versus the minimum copper: a greater than 500 percent increase in surface area only results in a 40 percent decrease in thermal resistance. The extra copper surface area then does not substantially decrease the thermal resistance but consumes more valuable real estate on the circuit board.

In designing a circuit board for the DirectFET, one would then look for the optimum balance between minimizing surface area and minimizing the heat resistance. One strategy to enhance the heat conduction and keeping board real estate to a minimum, would be to add large thermal vias into the pads adjacent or under the DirectFET leads.

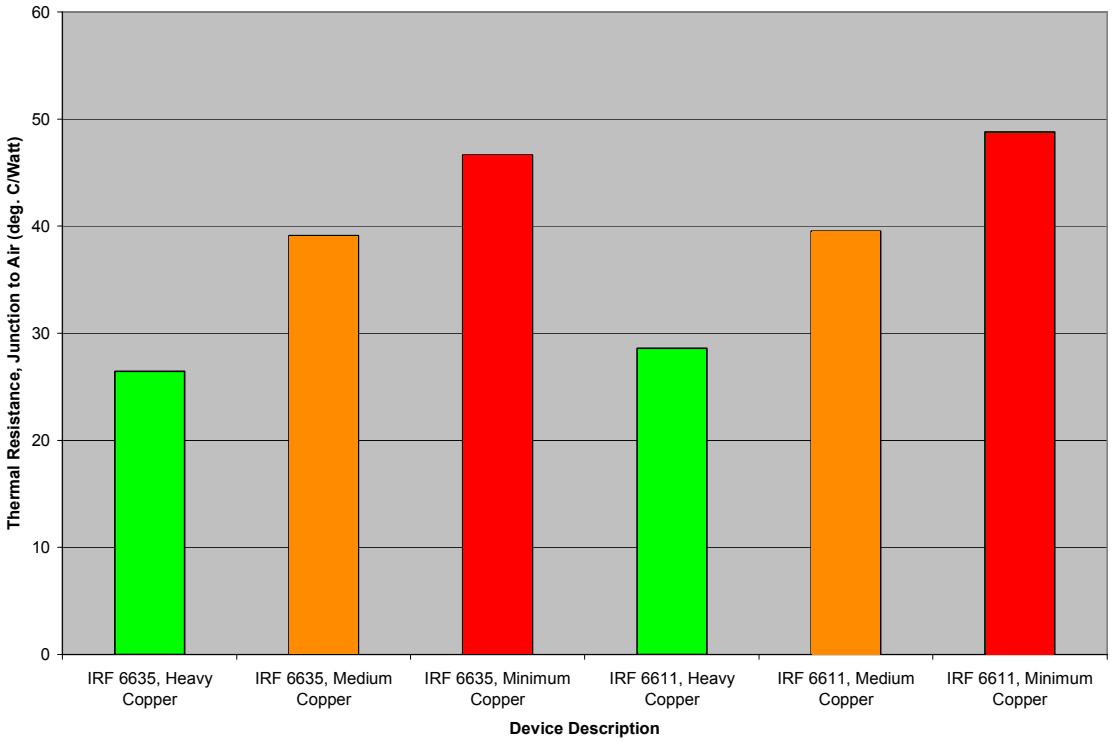

Figure 14 . Effect of Copper Quantity on Thermal Resistance

4.0 Summary

4.1 General

- JPL, NEPP and SMI performed a study of the DirectFET packaged power MOSFET devices.
- JPL, NEPP and SMI compared and contrasted the electrical and thermal performance of four DirectFET devices, four SO-8 devices and two Toshiba High Efficiency devices listed in Table I.
- IR selected the devices (except the Toshiba devices which were selected by JPL) for this study and provided sample units to JPL.
- Only two sets of device types are strictly comparable from both an electrical and thermal standpoint: (1) the IRF 6611 and IRF 7832 and (2) the IRF 6635 and IRF 7852.
- All other devices were then subject to only a more limited analysis from which broad conclusions about the effects of the packaging type were not always possible.

4.2 Electrical Performance

- SMI measured the following electrical characteristics of the MOSFET devices: RdsOn, Ids and Vth.

Initial Electrical: IRF6611/IRF6635 (DirectFET) vs. IRF7832/IRF7852 (SO-8)

- The DirectFET packaged devices channeled larger currents, up to 45% more, while dissipating the same or up to only 20% more power than the comparable SO-8 devices.

Initial Electrical: DirectFET vs. SO-8 and Toshiba HE Devices

- Only a basic comparison between packaged device power performance was possible.
- In terms of dissipated power versus drain current, the IRF6611 and IRF6635 devices outperformed all others that were tested.

Effect of Environmental Testing

- Devices were all subjected to a series of environmental tests with periodic electrical measurements as described in Table II.
- The temperature cycling and heat soak tests had a negligible effect on the mean value measured device parameters.

- The temperature cycling and heat soak tests had no visible effect on the distribution of measured device parameter values within a group of parts.

- For all the devices, the RdsOn values varied relative to the initial electrical measurements by at most +/- 3 percent.

- For all the devices, the Vth values varied relative to the initial electrical measurements by at most +/- 1 percent.

4.3 Thermal Performance

DirectFET vs. SO-8 Devices: IRF6611/IRF6635 vs. IRF7832/IRF7852

- In the DirectFET package, the Drain lead is connected to a large lid, which increases by about 120% the surface area (relative to SO-8 lead frame) over which heat may be dissipated

- Heat sinking, as demonstrated using finned heat sinks, reduces thermal resistance, Rj-l, by about 75% relative to the SO-8 packages.

- The DirectFET packaging significantly reduced the thermal resistance relative to ambient, Rj-a, of the devices, by as much as 23%.

- The addition of a heat sink, as demonstrated using a finned heat sink, to the top of the DirectFETs further reduced the thermal resistance by about another 5 to 10%.

- Using finned heat sinks combined with forced convection or using conductive cooling techniques, such as heat pipes or cold plates, could further reduce thermal resistances.

DirectFET vs. SO-8 and Toshiba HE: General

- On average, the devices using DirectFET packaging could dissipate about 23 percent more power while simultaneously attaining a 70 percent reduction in Rj-l and a 21 percent reduction in Rj-a.

- On average, the high efficiency device delivers a thermal performance similar to the DirectFET devices.

- Relative to SO-8 packaged devices, the Toshiba HE package delivers a 12 and 62 percent improvement in the thermal resistances, Rj-a and Rj-l, respectively.

- The 8004-H device delivers thermal performance that is within +/- 6 percent of that obtained on average from the three DirectFET type devices.

- The Toshiba HE package, however, cannot be as efficiently heat sinked as the DirectFETs.

- As with SO-8, the Toshiba package is a molded plastic package design and acts as a thermal barrier. Consequently, heat sinking, other than adding thermal vias under the drain and source pads, is not effective.

Effect of Pad and Circuit Trace Surface Area on DirectFET Thermal Resistance

- Large copper pads and wide traces help dissipate heat from DirectFET devices but at the cost of increasing PWB area.
- A 20 percent increase in pad and circuitry surface area (medium copper configuration relative to minimum configuration) yields a nearly identical decrease in thermal resistance.
- This approach has its limitations: a greater than 500 percent increase in surface area only results in a 40 percent decrease in thermal resistance.
- Heat sinking the top of the package and adding thermal vias in the pads may be more efficient methods than increasing circuit surface area to minimize thermal resistances.

5.0 Conclusions

- ***Of all devices tested, the DirectFET IRF 6635 displayed the best combined electrical and thermal performance while the DirectFET IRF 6611 displayed the second best performance.***
- ***The values of all measured electrical parameters for all devices irrespective of packaging type were not affected by temperature cycling or heat soaking to temperature extremes as low as -65ºC or as high as 150ºC.***
- ***DirectFET devices exhibit thermal resistances up to 75% lower than that of comparable SO-8 packaged MOSFETs.***

6.0 Recommendations

- Use of DirectFet over the SO-8 packaging is highly recommended for better electrical and thermal performance in the temperature ranges of -66ºC to 150ºC
- Continue evaluation of some new generation DirectFet Packaging, by International Rectifier, intended for extreme temperatures required for space application.
- Evaluate the thermal performance of DirectFET devices with conductive cooling
- Also include in a future evaluation, the new generation DirectFet packaging chosen for radiation requirements by a parts engineer.