

Reference No.: 33
Project Title: Robust Manufacturing Processes for CSPs
NEEP Project: Electronic Packaging Project
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Center: Jet Propulsion Laboratory
Status: New: On going: Third year of three year program
Performance Period: FY 98 – FY00
Benefits: Robust CSP manufacturing process will assure ready integration for microelectronic application to space flight hardware. These miniature packages reduce weight due to their small sizes and cost due to being commercial-off-the-shelf.

Partnerships and Endorsements CISM, X-2000, DSN, Mars Exploration, NASA-Wide programs for use of miniaturized commercial of the shelf (COTS) electronic packages such as Space Station; data exchange with GSFC to perform analytical modeling, Information exchange and training course for other centers.

Industry wide consortium with nearly 30 team members has been established and has designed its first test vehicle with 15 packages. In addition, three industry consortia with very large memberships also support our activities. An in-kind contribution of about eight times is estimated.

The current team members include: Boeing, Raytheon, TRW, ITT, Litton, USAF, Harris, Sandia National Labs., Micron, Sun Microsystems, StorageTek, Siemens, Hughes Network Systems, Amkor, Kyocera, Abpac, AMD, Sony, GE, Mitsubishi, EPIC, Irvine Sensors, LG Semicon, Flip Chip Technologies. And three industry consortia are: ITRI, Sematech, NCMS

Objectives of Proposal Activity: Develop board level manufacturing parameters related to interconnect quality and reliability for the rapidly growing miniaturized chip scale packages. Select a large number of packages from low to high I/O and assemble on printed wiring board (PWB). Determine robustness of the new technology by ease of manufacturing using leaded conventional package as control. Include packages with high pitch to low pitch to understand manufacturing limitation of this technology. Use different surface finish such as HASL, OSP, and Ni/Au to see adaptability of this new technology with conventional surface finish (HASL) to newer cost-effective version (OSP). Assemble grids CSPs with a known placement offset to determine self-alignment limitation for package type, weight, and I/O. Use conventional and other cleaning techniques to see the effectiveness of cleaning for low profile CSP assemblies. Develop and validate inspection and evaluation (e.g. NDE) criteria and processes. This task directly relates to the evaluation of the readiness of emerging commercial-off-the-shelf (COTS) CSP microelectronics manufacturing processes. Guidelines on CSP assessment, test methods/tools evaluation, advanced interconnect technology process characterization, inspection and interconnect reliability will be provided to NASA projects as well as industry.

Technical Approach: Implement the agreed task plan with consortia to create quantifiable board level assembly data correlation between manufacturing variables to interconnection reliability. Inspection criteria and processes will be developed and validated by testing to failure under various environments (thermal and dynamic). Failure modes will be identified and crack initiation and propagation as a function of

