Modeling of Single Event Effects in Circuit-Hardened High-Speed SiGe HBT Logic

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Abstract— **This paper presents SEE modeling results of circuit-hardened SiGe HBT logic circuits. A simple equivalent circuit is proposed to model the ion-induced currents at all of the terminals, including the p-type substrate. The SEE sensitivity of a D flip-flop was simulated using the proposed equivalent circuit. The simulation results are qualitatively consistent with earlier SEE testing results. The circuit upset is shown to be independent of the number of active paths. Considerable charge collection occurs through the reverse biased n-collector/p-substrate junction, regardless of the status of the emitter steering current, resulting in circuit upset through the commonly connected load resistor. A heavily doped substrate is shown to be beneficial for SEE.**

Index Terms: Single Event Effects, SiGe, HBT, charge collection, circuit modeling, current-mode logic.

I. Introduction

SiGe HBT technology, because it has higher intrinsic performance than Si technology at similar process complexity, and delivers better cost-performance than GaAs technology, has recently emerged as a contender for high-speed digital, RF, and microwave applications. Previously, as-fabricated first generation SiGe HBTs were shown to be robust to various types of ionizing radiation, in terms of both dc and ac electrical characteristics. Recently SiGe HBT logic circuits were found vulnerable to single-event effects (SEE) [1], and many surprising and unexplained phenomena were observed. Circuit level hardening using the current-sharing hardening (CSH) technique [2] was not effective for the SiGe HBT logic circuits investigated. To understand these SEE testing results, device and circuit simulations are needed. A logical approach is to use sophisticated mixed-mode circuit simulation, in which the electrical characteristics of the transistor being hit by an ion strike are solved using a device simulator. In addition to complexity, commercial mixed-mode simulators often do not support advanced transistor models used by circuit designers, making mixed-mode simulation difficult in practice.

An alternative and popular methodology is to simulate the SEE-induced transient terminal currents using a device simulator [3], and then use these transient currents as excitations in the circuit simulator used by designers. Advanced transistor models can be used as is. In this work, we present for the first time a simple equivalent circuit to model the SEE-induced transient currents in SiGe HBTs for circuit simulation. The heavy ion-induced terminal currents are examined as a function of linear energy transfer (LET), substrate doping, and circuit configuration using quasi-3D simulation [4] [5]. This model is used to simulate the SEE in a master-slave D flip-flop circuit that employs CSH hardening [1]. The SiGe HBT design kit from IBM was used in conjunction with Cadence's Spectre circuit simulator for circuit simulation. Inside the design kit, the SiGe HBTs were described using the Vertical Bipolar Inter Company (VBIC) transistor model.

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II. Device Technology

Fig. 1 shows a schematic device cross-section of the SiGe HBT used in these simulations. The SiGe HBT has a planar, self-aligned structure with a conventional poly emitter contact, silicided extrinsic base, and deep- and shallow-trench isolation. The SiGe base was grown using UHV/CVD. Details of the fabrication process can be found in [6]. The n-p-n layers of the intrinsic transistor and the p-type substrate form a n-p-n-p multi-layer structure, making the charge collection more complicated than in a conventional bipolar process [7]. The substrate is usually biased at the lowest potential in order to reverse bias the collector-substrate junction. Key performance metrics of the SiGe HBT's include: 1) 50GHz cut-off frequency (f_T); 2) 70GHz maximum oscillation frequency (f_{max}); 3) less than 0.5dB minimum noise figure (NF_{min}) at 2GHz; 4) an excellent power added efficiency of 65% at 900MHz; and 5) an excellent linearity efficiency of 10 at 2GHz.

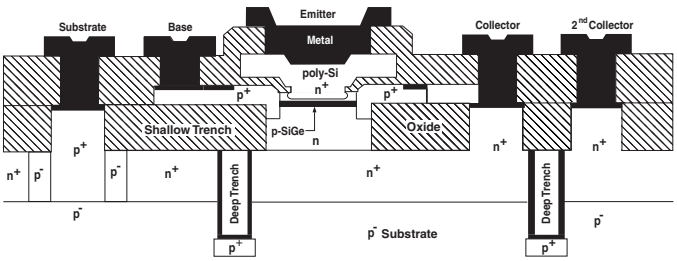

Fig. 1. The schematic cross section of the SiGe HBT used in simulation.

III. Equivalent Circuit Model

Upon an ion strike, a column of high density electrons and holes is deposited. Electrons are collected by the emitter (E) and collector (C), and holes are collected by the base (B) and sub-

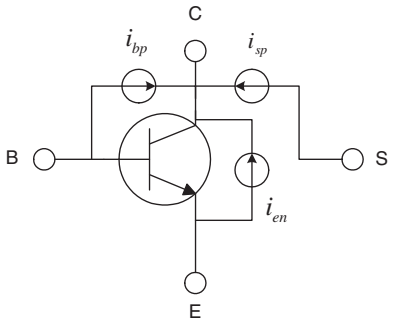

Fig. 2. An equivalent circuit model for including the ion-induced terminal currents in circuit simulation.

strate (S). For convenience, the ion-induced currents at the emitter and collector are denoted as i_{en} and i_{cn}, where the subscript n indicates "electron collection." Similarly, the ion-induced currents at the base and substrate are denoted as i_{bp}, and i_{sp}, where p indicates "hole collection." i_{en}, i_{cn}, i_{bp} and i_{sp} can be simulated using a device simulator as a function of time for a given ion strike. The sum of all of the terminal currents is always zero, which is verified by summing the simulated terminal currents. As a result, we only need to describe any three of the four currents, and the other current is automatically accounted for. The equivalent circuit shown in Fig. 2 explicitly describes i_{bp}, i_{sp}, and i_{en}:

- i_{bp} represents the hole current through the base. Even though i_{bp} appears between B and C, it contains all of the holes collected by the base through interactions with electrons collected by both the emitter and collector.
- i_{sp} represents the hole current through the substrate. Even though i_{sp} appears between the collector and substrate, it contains all of the holes collected by the substrate through interactions with electrons collected by both the emitter and collector.
- i_{en} represents the electron current through the emitter. i_{en} appears between the collector and emitter, and connects with both i_{sp} and i_{bp}. Such a connection is necessary to ensure that all the terminal currents are properly described.

The ion-induced electron current through the collector, i_{cn}, is given by:

$$i_{cn} = -(i_{bp} + i_{sp} + i_{en}) \quad (1)$$

IV. Circuit Description

A rising edge-triggered master-slave D flip-flop SiGe HBT circuit is used in this work. The D flip-flop is a basic building block of the 32 stage shift-register tested in [1]. Fig. 3 shows the circuit schematic of the unhardened D flip-flop. The master stage consists of a pass cell (Q1 and Q2), a storage cell (Q3 and Q4), a clocking stage (Q5 and Q6), and a control switch (Q7). The slave stage has a similar circuit configuration. In the hardened version, each transistor element is implemented with a five path CSH architecture. Fig. 4 depicts the CSH concept using a single level basic current-mode logic gate. Three of the five paths are controlled by Vcs1, and the remaining two paths are controlled by Vcs2 and Vcs3, respectively. In the CSH hardened version of Fig. 3, these paths were maintained separately through the clocking stage and through the pass and storage cells. In essence, the

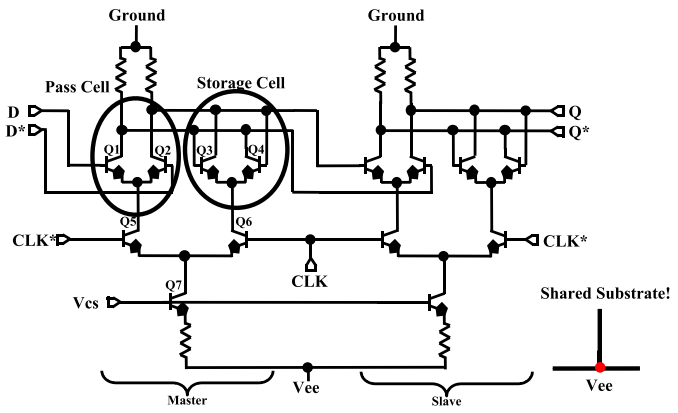

Fig. 3. Schematic of the rising edge-triggered master-slave D flip-flop used in simulation. Each transistor element consists of five subtransistors arranged according to the CSH concept. The current source transistor Q7 was divided into 5 paths, with Vcs1 controlling 3 paths and Vcs2 and Vcs3 controlling 1 path each. These paths were maintained separately through the clocking stage and through the pass and storage cells.

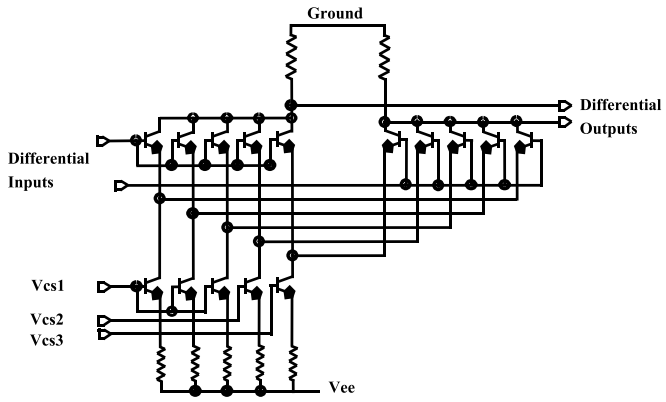

Fig. 4. Current-sharing hardening (CSH) implementation of a basic CML gate. 5 parallel (sub)transistor elements are used to maintain separate current paths.

input and output nodes of five copies of the switching circuits, including the controlling switch, clock, master and storage cells, are connected in parallel. The load resistance is shared by all the current paths. The full schematic of the hardened version is not shown here because of the large number of transistors and interconnects.

V. Device Simulation Approach

At the device level, the SEU-induced transient terminal currents are obtained using quasi-3D device simulation, which was reported in [3] for the same SiGe HBTs used in this work. MEDICI, a commercial device simulator, was used. In [3], we examined SEE-induced charge collection at the device level as a function of device bias, load condition, substrate doping, and ion strike depth. In this work, we examine how the device level SEU-induced charge collection translates into circuit level upset.

A brief summary of the device simulation is as follows. The SiGe HBT doping profile and Ge profile were constructed using measured SIMS data and calibration of dc and ac electrical characteristics. A set of advanced physical models (as opposed to the default simplest models) were selected, and the coefficients were tuned to match the measured dc and ac electrical character-

istics [8]. All of the lateral structures shown in Fig. 1, including the deep- and shallow-trench isolation, were present in the simulation. Because of the large SEU-induced transient current in the substrate, we use a top substrate contact as shown in Fig. 1, which better mimics reality, as opposed to a bottom contact that is typically used in conventional device simulation [3].

To account for the charge collection deep in the substrate, the geometries of the simulation region must be sufficient such that the boundary conditions implemented in the device simulator are consistent with the physical boundary conditions. In practice, only a finite depth substrate can be simulated due to memory, speed, and complexity limitations. The minimum depth required to provide a reasonable approximation is problem specific, and depends on LET, the depth of ion strike, doping, and bias. Our approach to determining the minimum depth is to gradually increase the simulation depth until the simulated charge collection results no longer change. For most of the simulations used in this work, the minimum simulation depth is between 50–100μm.

The center of the emitter was used as the cylindrical z-axis as an approximation of a worst case ion strike. A fine mesh was used along the path of the ion strike, and at the pn junction interfaces. The average number of nodes is 10^4 for each simulation. The validity of the griding scheme was checked by repeating the simulation on finer grids. The charge track was generated over a period of 10 picoseconds using a Gaussian waveform. The Gaussian has a 1/e characteristic time scale of 2 picoseconds, a 1/e characteristic radius of 0.2μm, and the peak of the Gaussian occurs at 4 picoseconds. By default, the depth of the charge track is 10μm, and the LET value is uniform along the charge track. Two substrate doping values of $5 \times 10^{15}/cm^3$ and $1 \times 10^{18}/cm^3$ and five LET values from 0.1-0.5pC/μm are simulated. Currents going into the terminals (E,B,C,S) are defined to be positive.

VI. Simulation Results and Discussion

Transient currents for different SEU conditions are then simulated using quasi-3D device simulation, and included in circuit simulation using the equivalent circuit model described in Section III. In principle, any transistor in the circuit can be hit. Here we focus on the sensitive storage cell transistors (Q2 and Q3) in the master stage. In the following, circuit upset is examined as a function of the current paths configuration, LET, and substrate doping level respectively, followed by discussions of hardening implications.

A. Impact of Current Paths

One of the most surprising heavy ion testing results reported in [1] was that upset occurs even when the transistor being hit is in the inactive current path. To mimic this testing condition, **we turned on only Vcs1, and turned off both Vcs2 and Vcs3**. At 2ns, the SEE-induced transient currents were activated on one of the **Vcs3 controlled** sub-transistors in the storage cell of the master stage (Q3). Fig. 5 shows the simulated SEE response of the D flip-flop for a LET of 0.5pC/μm and a substrate doping of $10^{18}/cm^3$. The data rate is 2 Gigabit/second. The input data is an alternating "0" and "1" series. In total, the SEE-induced transient currents disrupt 6 bits of data at the output. This is qualitatively consistent with the testing results.

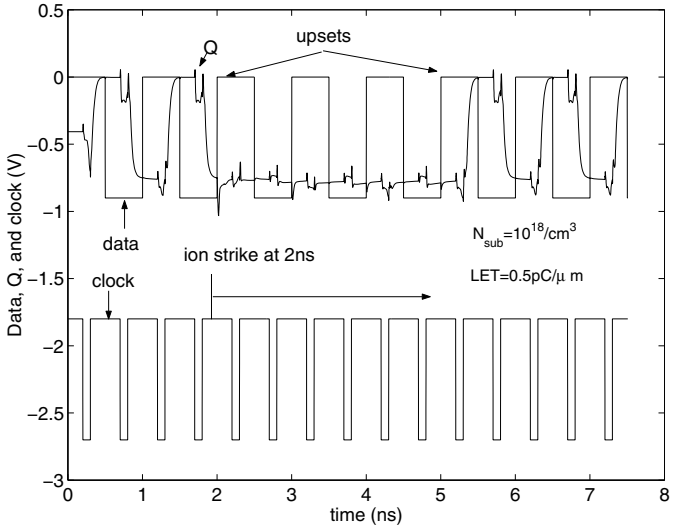

Fig. 5. Simulated SEE response of the D flip-flop for $N_{sub} = 10^{18}/cm^3$ and LET=0.5pC/μm.

The above circuit simulations were performed for two sets of transient currents simulated for a grounded emitter (as was done in [3]), and an emitter connected to the ground through a large resistor. In principle, a large emitter resistor allows us to better mimic the impedance seen by the emitter of a switching transistor in an inactive path. The resulting circuit level upsets, however, are virtually identical for the two emitter connections. The status of the steering current source ("on" or "off") does not have much impact on the collector current transients in the switching transistor being hit, and thus the circuit level upset.

Another observation in [1] was that the upset rate was independent of the number of active current paths. The simulated SEE responses from using different numbers of active current paths are indeed identical. The total switching current is kept the same for different combinations of active path configurations, as was in the experiment [3], in order to maintain the correct logic swing. Fig. 6 compares the SEE responses for: 1) Vcs1 is on, Vcs2 and Vcs3 are off, and 2) Vcs1, Vcs2 and Vcs3 are all on. In both cases, the levels of the control voltages are adjusted such that the total switching current flowing through the load resistor is fixed.

The above simulation results are consistent with the testing results, and indicate that the CSH technique is not effective for hardening this technology. One of the reasons, we believe, is that the collector current (i_{nc}) of the transistor being hit is not controlled by the emitter when the strike occurs. A considerable portion of charge collection occurs in the n^+ collector to p-substrate junction. i_{cn} can thus be dominated by i_{sp}. Even if the controlling transistor is off before the associated memory transistor is hit, a significant amount of i_{cn} is generated in the memory transistor, and flows through the same load resistor, thus causing an upset. As a result, the SEE response is insensitive to the number of active current paths.

B. Impact of LET

Fig. 7 shows the SEE responses for LET=0.1, 0.2 and 0.3pC/μm ($N_{sub} = 10^{18}/cm^3$). The other simulation conditions

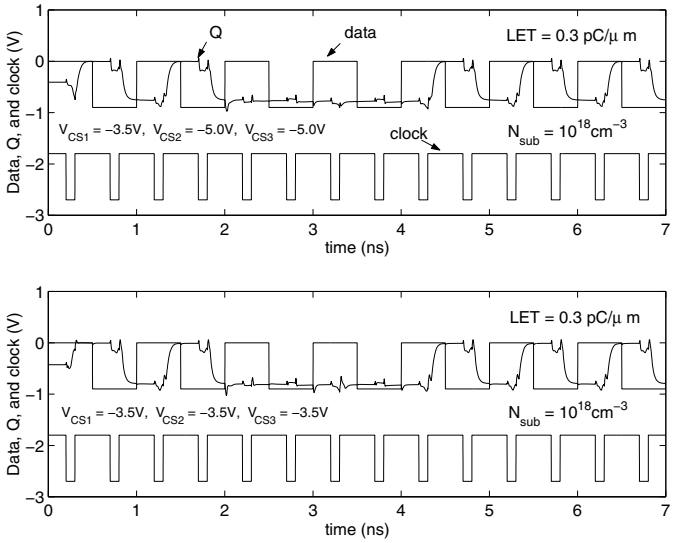

Fig. 6. Comparison of the simulated SEE responses using different active current paths: 1)Vcs1 on, Vcs2 and Vcs3 off, 2) Vcs1, Vcs2 and Vcs3 all on. $N_{sub} = 10^{18}/cm^3$ and LET=0.5pC/μm.

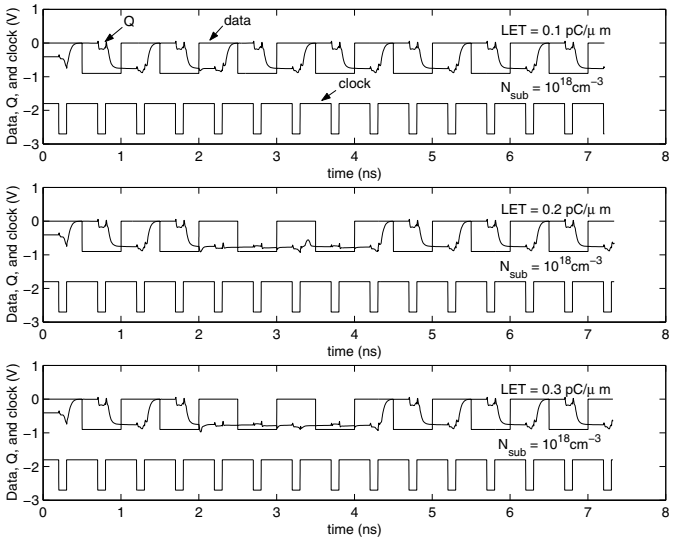

Fig. 7. Simulated SEE response of the D flip-flop for LET=0.1, 0.2 and 0.3pC/μm. $N_{sub} = 10^{18}/cm^3$.

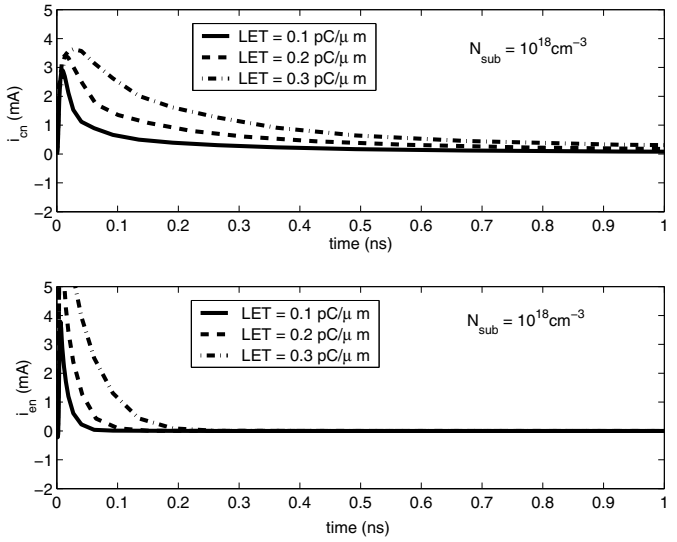

Fig. 8. SEE-induced collector and emitter currents for LET=0.1, 0.2 and 0.3pC/μm. $N_{sub} = 10^{18}/cm^3$.

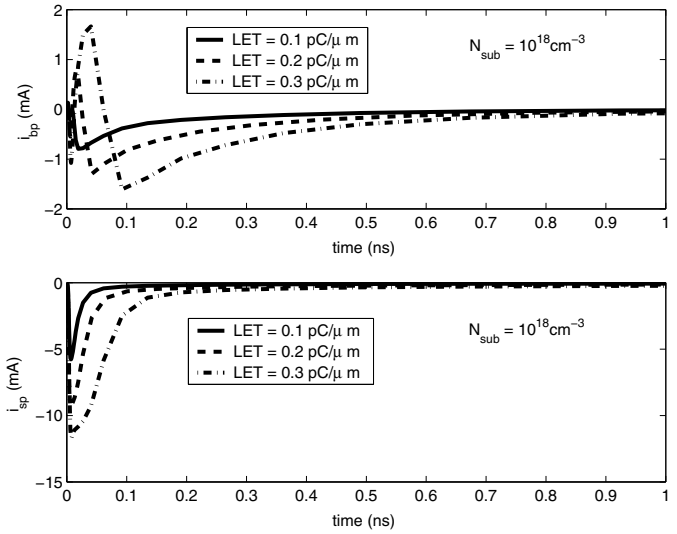

Fig. 9. SEE-induced base and substrate currents for LET=0.1, 0.2 and 0.3pC/μm. $N_{sub} = 10^{18}/cm^3$.

are the same as for Fig. 5. No upset occurs for LET=0.1pC/μm, and 4 bits of upset occur for LET=0.2 and 0.3pC/μm. The number of upset bits is 4 and 6 for LET=0.4 and 0.5pC/μm.

Fig. 8 and 9 show the SEE-induced transient currents as a function of the time from the strike used in simulating Fig. 7. The transient currents were obtained from MEDICI simulation for an off-state transistor biased at $V_B = 0$, $V_E = 0$, and $V_{sub} = -5.2V$. It is worth noting that at only 1ns after the ion strike, i_{cn} becomes well below the switching current (approximately 5mA) of the circuit. However, the circuit upset continues, and lasts for 3ns in the cases of LET=0.2 and 0.3pC/μm (Fig. 7). This indicates a considerable circuit level memory effect of the upset triggered by the transient SEU currents.

C. Impact of Substrate Doping

Our earlier device simulation results showed that the maximum magnitude of SEE-induced transient currents is much larger for SiGe HBTs with a heavily-doped substrate, while the duration time of the transient currents is much longer for SiGe HBTs with a lightly-doped substrate [3]. It was not clear, however, how the substrate doping level affects the circuit-level SEE response. Fig. 10 shows a typical comparison between the circuit SEE responses from using a $5 \times 10^{15}/cm^3$ substrate and from using a $1 \times 10^{18}/cm^3$ substrate. Surprisingly, more data bits are corrupted for a lightly-doped substrate than for a heavily-doped substrate, despite the fact that the peak collector transient current is significantly lower for a lightly-doped substrate than for a heavily-doped substrate, as shown by the device simulation results in Fig. 11. The transient base and substrate currents are

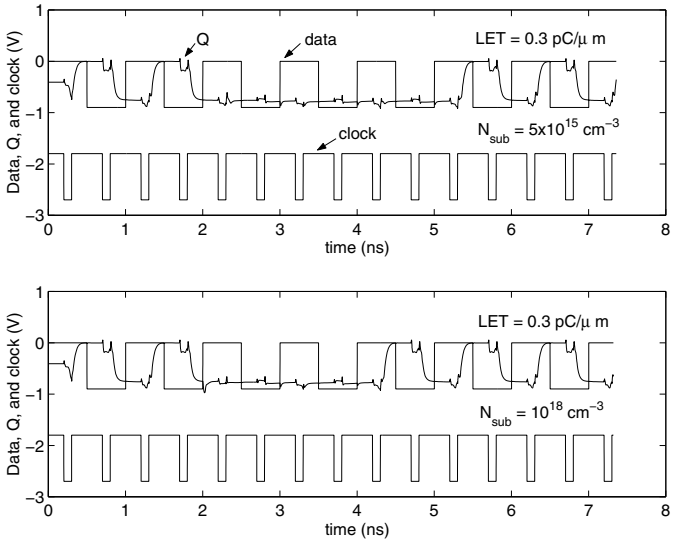

Fig. 10. Simulated SEE response of the D flip-flop for $N_{sub} = 5 \times 10^{15}/cm^3$ and $N_{sub} = 10^{18}/cm^3$. LET=0.3pC/μm.

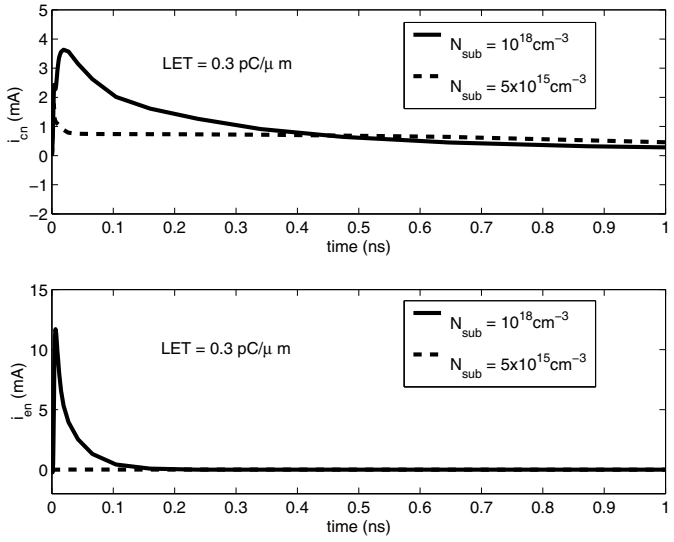

Fig. 11. SEE-induced transient collector and emitter currents for $N_{sub} = 5 \times 10^{15}$ and $10^{18}/cm^3$. LET=0.3pC/μm.

shown in Fig. 12 for the two substrate doping levels used.

For the heavily-doped substrate, the circuit upset continues after the SEE-induced collector current reduces to well below the switching current (5mA), indicating a memory effect. These are likely related to charge storage effects and the circuit topologies of the pass cell and the storage cell shown in Fig. 3. For the lightly-doped substrate, the transient collector current is always much smaller than the switching current, even though the circuit level upset is worse than for the heavily-doped substrate. On the other hand, the charge collection time has a stronger correlation to the circuit level upset duration than the magnitude of the transient currents. Fig. 13 shows the charge collected by the collector as a function of time, obtained by integrating the transient collector current with respect to time, for the two substrate doping levels. Charge collection occurs over a longer period of time for the lightly-doped substrate. We are investigating the details of the circuit upset to gain intuitive understanding of the substrate doping dependence and upset mechanism.

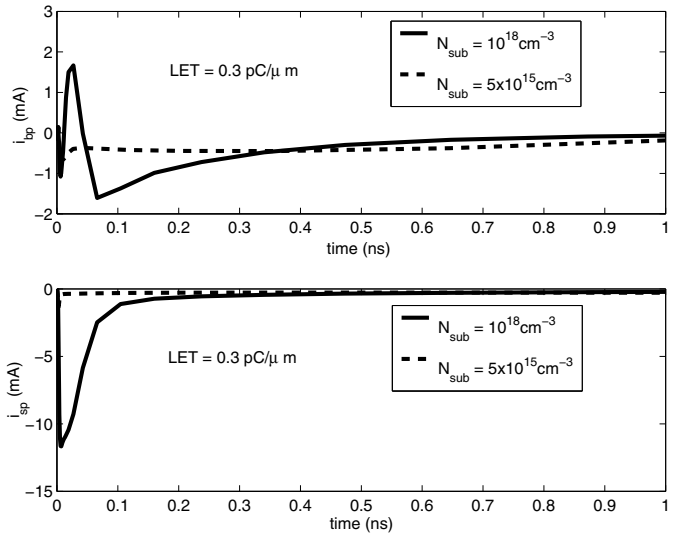

Fig. 12. SEE-induced transient base and substrate currents for $N_{sub} = 5 \times 10^{15}$ and $10^{18}/cm^3$. LET=0.3pC/μm.

D. Hardening Implications

SiGe HBT current mode logic circuits operate by switching a current between two emitter coupled transistors. A logical approach to hardening is to increase the switching current. Another approach is to decrease the total amount of charge deposition. The use of a larger switching current necessarily increases power consumption, and chip area as well if transistors are to be operated at the same high current density to minimize gate delay. Caution must be exercised when comparing the SEE responses of a hardened circuit and its unhardened version: comparisons can be made at either the same current or the same current density. To confirm the effectiveness of this hardening approach, we repeated the simulation by increasing the switching current. For each LET used, upsets disappear when the switching current is above certain threshold, as expected. Circuit-level or logic-level hardening techniques that do not have significant power and chip area penalties are certainly preferred over a simple increase of switching current.

The total charge deposition can only be effectively reduced by reducing the thickness of the p-type substrate, or simply removing the p-type substrate through the use of an insulating substrate, such as an SOI substrate. We performed simulations for different p-type substrate thicknesses, which confirm that the upset rate decreases monotonically with decreasing p-type substrate thickness. An insulating layer was assumed to be below the p-type substrate. Any post-processing that can thin the substrate, and transfer the active device layers to an insulating substrate can therefore improve the SEU immunity of SiGe HBT logic circuits.

VII. Conclusions

A simple equivalent circuit model for including SEE-induced transient currents in SiGe HBTs was proposed, and applied to the simulation of the SEE response of a circuit hardened SiGe HBT

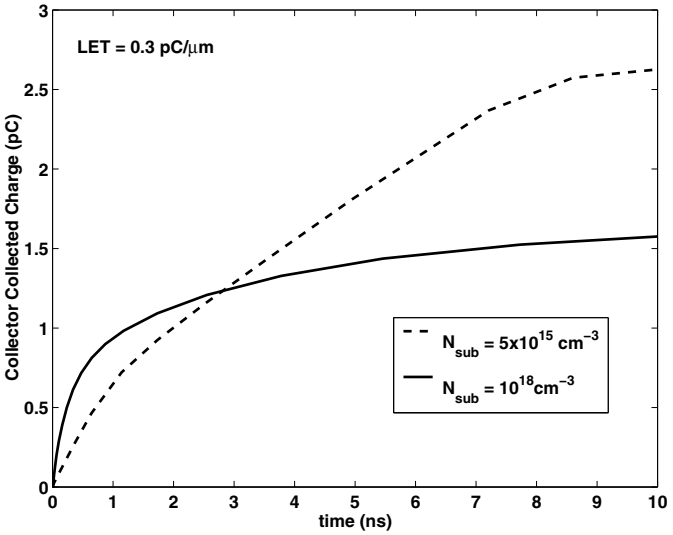

Fig. 13. Collector collected charge as a function of time for $N_{sub} = 5 \times 10^{15}$ and $10^{18}/cm^3$. LET=0.3pC/μm. Charge column length is 10μm.

master-slave D flip-flop. Various LET values were simulated for a lightly-doped substrate and a heavily-doped substrate. Data upset continues after the SEE-induced transient collector current reduces to well below the switching current. The upset is insensitive to the number of active current paths as long as the total switching current is kept the same. Upset occurs even when the transistor being hit is in an inactive path. These results are consistent with reported SEE testing results. The upset was found to be worse for a lightly-doped substrate than for a heavily-doped substrate. In future work, quantitative simulation to data comparison will be made using more realistic 3-D device simulation.

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