REVISIONS			
SYMBOL	DESCRIPTION	DATE	APPROVAL
---	Released	1/5/93	

SHEET REVISION STATUS

SH	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
REV	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SH	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
REV	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SH	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
REV	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SH	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
REV	-																			

ORIGINATOR A. F. Moor/Paramax	DATE 12/4/92	FSC: 5962
APPROVED /Paramax	12/4/92	Procurement Specification for Real Time Express DSP/ Microcontroller, RTX2010RH Type Microcircuit, Radiation Hardened, (100 Kilorad (Si) minimum)
CODE 311 APPROVAL /GSFC	12/4/92	
CODE 311 SUPERVISORY APVL /GSFC	12/4/92	
ADDITIONAL APPROVAL		S-311-P-721

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND 20771

CAGE CODE: 25306

1. SCOPE

1.1 Scope. This drawing describes device and Quality Conformance Inspection (QCI) requirements for Class S SOS (silicon on sapphire) CMOS radiation hardened Real Time Express core microcontroller microcircuit in accordance with 1.2.2 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with non-compliant non-JAN devices".

1.1.1 Description. The RTX 2010RH is a radiation hardened 16-bit core microcontroller with on-chip timers, an interrupt controller, a multiply-accumulator, and a barrel-shifter.

The RTX 2010RH is Pin compatible to the RTX 2000 and RTX 2001A and incorporates two 256-word stacks with multitasking capabilities, including configurable stack partitioning and over/underflow interrupt control.

Instruction execution times of one or two machine cycles are achieved by utilizing a stack oriented, multiple bus architecture. The high performance ASIC BusT, which is unique to the RTXT family of products, provides for extension of the microcontroller architecture using off-chip hardware and application specific I/O devices.

The RTX 2010RH microcontroller supports the C and Forth programming languages.

The RTX 2010RH has been designed and fabricated utilizing the Harris Advanced Standard Cell and Compiler Library.

1.2 Part number. Parts procured in complete compliance with the requirements of this specification shall be identified by a Goddard part number of the following form:

1.2.1 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as specified below (See Figure 2A and 2B herein):

001: 84 Pin Grid Array (PGA)
002: 84 Pin Quad Flatpack

1.2.2 Device type(s). The device type(s) shall be identified as specified in attached specification sheets (See Figure 1 herein).

1.3 Absolute maximum ratings.

Supply voltage (referenced to ground) ...	+7.0 Vdc maximum
Input, output, or I/O voltage applied) ..	GND -0.5 Vdc to V_{CC} +0.5 Vdc
Storage temperature range	-65°C to +150°C
Maximum package power dissipation (P_D)	2 W
Lead temperature (soldering, ten seconds)	+300°C
Junction temperature (T_J)	+175°C
Gate count	30,000
Thermal characteristics:	
Junction-to-ambient (rO_{ja})	TBD °C/W
Junction-to-case (rO_{jc})	TBD °C/W

1.4 Recommended operating conditions.

Operating voltage range (V_{CC})	+4.5 Vdc to +5.5 Vdc
Frequency of operation (f_{MAX})	8 MHz
Case operating temperature range (T_C) ...	-55°C to +125°C
Maximum rise and fall times for E15-E13 (t_r, t_f)	20 ns

1.5 Radiation characteristic/properties.

Gamma total dose	>100 kilorads(Si)
Transient upset	$>10^{10}$RAD(Si)/sec
Single Event:	
Upset	$<1 \times 10^{-10}$Upsets/bit-day
L.E.T.	>80 MeV/mg-cm^2
Latch-up	Not possible
Snap-back	Not possible

2. APPLICABLE DOCUMENTS

2.1 Government specification and standards. Unless otherwise specified, the following specification and standards of the latest issue in effect at time of device manufacture, form a part of this drawing to the extent specified herein.

SPECIFICATIONS
MILITARY

MIL-I-45208 - Inspection System Requirements.

MIL-M-38510 - Microcircuits, General Specification for,

STANDARDS
MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations, and Waivers

MIL-STD-883 - Test Methods and Procedures for Microcircuits

MIL-STD-976 - Certification Requirements for Microcircuits

MIL-STD-1835 - Microcircuit Case Outlines

OTHER DOCUMENTS
GODDARD SPACE FLIGHT CENTER (25306)

S-311-M-70 - Destructive Physical Analysis of Electronic Parts, Specification for

(Copies of the specification and standards required by the manufacturer in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

2.2 Order of precedence. The order of precedence shall be as follows: Purchase order, this specification, the applicable military documents. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

2.3 Copies of documents. Unless otherwise specified, copies of federal and military specifications, standards and handbooks, are available from the Standardization Documentation Order Desk, 700 Robbins, Section D, Bldg. 4., Philadelphia, PA 19111-5094.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.2 of MIL-STD-883. "Provisions for the use of MIL-STD-883 in conjunction with non-compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, Class S requirements, except as otherwise stated herein. The use of silver glass die attach, "metal glass die mounting", is acceptable (as allowed by 3.5.7 of MIL-M-38510, with Procuring Activity approval). As devices supplied to the requirements of this drawing are not compliant non-JAN device types, the manufacturer need not validate device design against the requirements of MIL-STD-883. However, the Procuring activity reserves the option to review all nonproprietary design documentation (see 3.9 herein).

3.2.1 Case outlines. The case outline shall be in accordance with 1.2.1 and as specified in Figures 2A and 2B herein. Lead material shall conform to MIL-M-38510 and lead finish shall be Type C (gold plate) as defined by MIL-M-38510.

3.2.2 Functional diagram. The functional diagram shall be as specified in Figure 3 herein.

3.2.3 Terminal connections and signal assignments. The terminal connections and signal assignments shall be as specified in Figures 4A and 4B herein. A description of each signal assignment is specified in Figures 5A through 5E herein.

3.2.4 Instruction codes. The instruction codes shall be as specified in Tables 1A through 1Q.

3.3 Materials. External parts, elements or coatings, including markings, shall be nonnutrient to fungus and shall not blister, crack, outgas, soften, flow, or exhibit defects that adversely affect storage, operation or environmental capabilities of microcircuits delivered to this specification under the specified test conditions. **NOTE:** The use of silver glass die mount is permitted (reference paragraph 4.2b herein).

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are specified in Table 2A herein and shall apply over the full case operating temperature range.

3.4.1 Fault coverage. The manufacturer shall provide written certification that the parts manufactured and built to this specification shall meet a minimum fault coverage of ninety-six percent (96%) or higher, excluding unconnected nodes (i.e., Q and Q) and 100% on all I/O's (per MIL-M-38510/605, Microcircuits, Digital, CMOS, Semicustom (Gate Array) Devices, Monolithic Silicon, fault grading shall be 90%, as a minimum). Silos fault simulations or equivalent, using the methods described in MIL-STD-883, Method 5012, shall be performed using the simulation vectors used for design verification and subsequently for package test of the RTX2010RH device.

The simulator used shall have an enhanced concurrent fault simulation algorithm that accurately models input-stuck and output-stuck faults. The concurrent fault simulation shall simultaneously compare the resultant state values at test node outputs, for many "faulted" networks with the corresponding "fault-free" network. For the circuit being tested, each of the faulted networks shall have a node in either a Low (0) or a High (1) state.

An actual (or hard) detect for a faulted node shall be reported when the level of the test node outputs differs between the faulted and fault free networks and neither of the levels is an Unknown. A possible (or soft) detect shall be recorded whenever the level of at least on test node changes from the previous strobe time.

Oscillations caused by a circuit with feedback shall be excluded from being counted as a faulted node. The program used shall check for oscillations be comparing the iteration count of the circuit affected by the stuck fault with the iteration count of the identical fault-free circuit. If the iteration count exceeds a set value before the next iteration for the fault-free circuit occurs, the faulted circuit is considered to be oscillating.

3.4.2 Functional testing. Devices supplied to this specification shall perform functionally and are to be guaranteed to execute the instruction codes described in Tables 1A through 1Q, herein, when tested at eight megahertz (8MHz). Testing shall be performed, 100%, on all opcodes and the devices shall meet the fault coverage as specified in paragraph 3.4.1 herein. In addition, the manufacturer shall supply test tapes, to the Procuring Activity, to perform independent electrical verification at a National Aeronautics and Space Administration (NASA) approved facility. Test tapes shall be maintained under manufacturer's configuration control and shall adhere to the requirements of paragraph 3.9 herein.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in Table 2B herein. The electrical tests for each subgroup are described in Table 2A herein.

3.6 Screening requirements. Devices furnished to this specification shall be 100% screened to the requirements of MIL-STD-883, Method 5004, for Class-S device types, except as modified herein. The percent defective allowable (PDA) shall be as specified in MIL-STD-883, Method 5004 (see paragraph 4.2h herein).

3.7 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part number listed in 1.2 herein is for reference only. Microcircuits that comply with the requirements of this drawing shall be marked with the following (specified paragraph numbers refer to MIL-M-38510 unless otherwise specified):

a. Index point in accordance with 3.6.1.

b. Part number: (see paragraph 1.2 herein).

c. Inspection lot identification code in accordance with 3.6.3.2 except the unique suffix letter may be omitted when an alternate lot identifier is used which maintains the unique traceability required in 3.6.3.2.

d. Manufacturers identification in accordance with 3.6.4.

e. Electrostatic discharge sensitivity (ESD) identifier in accordance with 3.6.9.2. This may be used as the index point as defined by 3.7.a herein.

f. Marking location and sequence in accordance with 3.6.9.

g. Container marking in accordance with 3.6.10.

h. Serialization in accordance with 3.6.8. Serial numbers shall not be duplicated within a single lot of date code supplied.

3.7.1 Country of origin. County of origin marking is not required as only devices manufactured, assembled, and tested within the United States and its territories shall be supplied against the requirements of this drawing.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing. This certificate of conformance shall affirm that the manufacturer's product meets all requirements as set forth by this drawing and shall be signed by an authorized Quality Control representative within the manufacturer's organization.

3.9 Notification of change. Notification of change to the acquiring activity shall be required in accordance with MIL-STD-480 for all Class I changes.

3.10 Verification and review. The acquiring activity shall retain the option to review the manufacturer's facility and all applicable nonproprietary documentation and/or areas. Appropriate and mutually acceptable notification will be given to the manufacturer.

3.11 Traceability. Each device shall be traceable to a wafer lot. A wafer lot shall consist only of microcircuit wafers subjected to each and every process step of masking, etching, deposition, diffusion, metallization, etc., as a group. Each wafer lot shall be assigned a unique identifier which provides traceability to all wafer processing steps.

3.12 Rework. Rework of any operation from wafer manufacturing through final package seal shall not be permitted, except as allowed by MIL-M-38510 and MIL-STD-883, for product assurance level S. If rework is desired, the Procuring Activity must be contacted and written permission obtained. Rework documentation shall be submitted with the data package requirements of paragraph 5.2 herein.

3.13 Production facility. The manufacturer of microcircuits in compliance with this specification shall have and use production and test facilities, wafer fabrication facility excluded, certified by DESC in accordance with requirements of MIL-STD-976. Quality and reliability assurance program should be adequate to assure successful compliance with the provisions of this specification and the associated specifications sheets.

3.14 Automated test equipment programs. When automatic testing is used, this device's test program must be under manufacturer's configuration control, including date and revision level. The Procuring Activity shall be notified of any changes to these programs that affect the ability of devices to meet the requirements of this specification. Notification of changes are required during production of devices to an existing order or prior to acceptance of a

new purchase order to this drawing. The Procuring Activity reserves the right to review and/or request a copy of any test tape used in the production of devices built to this specification (see paragraphs 3.4.2, 3.10 and 4.3.1c herein).

3.15 Source inspection. The Procuring Activity shall perform pre-seal source inspection and final source inspection and reserves the right to perform other source inspections, when required by the purchase order, at the manufacturer's facility to assure device conformance to this specification. At least seventy-two hours notification shall be given by the manufacturer prior to pre-seal and final source inspection. Souce inspection shall include, but not be limited to, manufacturer's Statistical Process Controls (SPC), review of standard cell and compiler libraries, design methodology and tools, and review of the TSOS4 process.

3.16 Packaging. Packaging shall be in accordance with MIL-M-38510 and section 5 herein. Provision for ESD protection shall be provided. Preparation for delivery shall meet specified requirements for identification, certification, and data package requirements.

3.17 Destructive physical analysis. Sample devices delivered against this specification may, at the discretion of the Procuring Activity, be subjected to Destructive physical Analysis (DPA). When DPA is performed, testing shall be conducted in accordance with GSFC specification, S-311-M-70, for Class-S compliant material. Lot acceptance or rejection shall be based on successful completion of this testing.

3.18 Radiation hardness. These devices must meet or exceed the requirements for a Radiation Hardness Assurance (RHA) level of 100 kilorads (Si), minimum, when tested in accordance with the Group E, Subgroup 2, requirements of MIL-STD-883, Method 5005. There shall be no degradation of device performance at the 100 kilorad level. Radiation testing need not be performed by the manufacturer if the above limits are guaranteed in writing (see paragraph 1.5 herein).

3.18.1 Single Event Upset (SEU). Devices furnished to this specification shall **not** be susceptible to latch-up. The Linear Energy Transfer (LET) threshold shall be greater than or equal to 80Mev/mg-cm^2 for SEU. Radiation testing, for single event upset, need not be performed by the manufacturer if the above limits are guaranteed in writing (see paragraph 1.5 herein).

3.19 Data requirements. The deliverable data package is described in section 4.4 and 5.2 herein.

3.20 AC measurement points and timing diagrams. Devices furnished to this specification shall be capable of meeting the timing requirements specified in Figure 7 and Figures 8A through 8G herein.

3.21 Quality assurance provisions. Quality assurance requirements shall be as specified in MIL-STD-883, MIL-M-38510 and section 4 herein. The product assurance program shall be subject to review and approval by the Procuring Activity.

3.22 Qualification Requirements. Device qualification shall depend upon acceptability of manufacturer's reliability data on TSOS-4 process requalification by using 64K SRAM as Technology Characterization Vehicle (TCV).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510, product assurance level S, and to the extent specified in MIL-STD-883 (see 3.1 herein) except as modified by Tables 3 and 4, herein, for small lot Groups B and D inspection sampling.

4.2 Screening. Screening shall be in accordance with Method 5004 of MIL-STD-883, product assurance level S, except as modified herein, and shall be conducted on all devices (100%) prior to quality conformance inspection. The following additional criteria shall apply:

a. Internal visual inspection. Internal visual inspection shall be performed in accordance with MIL-STD-883, Method 2010, Test Condition A, except as follows (references shown to Method 2010 of MIL-STD-883):

(1) Paragraph 3.f(21). Add new definition as follows. SOS - Silicon on sapphire. It will be considered as a nonconductive material for all inspection criteria.

(2) Paragraph 3.1.3.c. A crack that exceeds 3.0 mils in length and points toward the active area, or comes closer than 0.25 mils to any operating metallization or other functional circuit element.

(3) Paragraph 3.1.3.d. Semicircular crack(s) or multiple adjacent cracks, not in the active area, starting and terminating at the edge of the die are acceptable.

(4) Paragraph 3.2.1.4. Add item "1." as follows. Bonds over contacts where at least 50% of the contact perimeter is undisturbed and visible is acceptable.

b. Manufacturer in-process controls.

(1) Wire bond pull monitor. Wire bond pull monitor shall be sampled in accordance to MIL-STD-883, Method 2011, Test Condition D, to a LTPD of 10 applying to the number of wire bonds pulled from two devices minimum at the start and end of each shift, at the end of each lot, after approximately two (2) hours of production, after changing spools, package or die size, and after performing equipment maintenance. The end of production for each operator each shift shall be satisfied if performed

anytime during the last hour of production. This criteria meets the requirements of MIL-STD-976 for in-line die shear monitor.

(2) Substrate attach strength. Substrate attach strength monitor shall be sampled in accordance to MIL-STD-883, Method 2027. Samples shall be pulled from each lot or sublot die attached on a single machine and processed as a single group through final adhesive cure, with the sample randomly selected according to the following table:

Lot Size	Sample Size	Failure Allowed
1 to 400	2	0
401 to 600	3	0
601 to 800	4	0
801 to 1000	5	0

For lot sizes larger than 1000 devices, the sample shall be .005 times the lot size. Lot size X .005 = randomly selected sample size with no failure allowed.

c. Burn-in tests. The manufacturer shall perform two burn-in tests on each device supplied. The burn-in tests shall be performed as follows:

(1) Static burn-in test. Test Condition A or B of MIL-STD-883, Method 1015 for 72 hours, minimum, with T_A = +125°C using the circuit as specified in Figure 6A herein. Accelerated testing shall **not** be permitted.

(2) Dynamic burn-in test. Test Condition D of MIL-STD-883, Method 1015 for 240 hours with T_A = +125°C using the circuit as specified in Figure 6B herein. Accelerated testing shall **not** be permitted.

The order of these burn-in tests may be reversed.

d. Nondestructive bond pull. Nondestructive bond pull test shall not be required. Elimination of this test is due to the manufacturer being physically unable to get the test fixture (jig) into place for devices packaged in configurations having greater than 40 internal bond wires. The spacing of the bond wires in conjunction with the physical size of the test fixture (jig) necessary to perform the pull test prohibit the performance of the test without damaging adjacent internal bond wire(s) (reference para. 4.2b(1) herein).

e. Radiographic inspection (X-ray). In accordance with MIL-STD-883, Method 5004, radiographic footnote; due to pin configuration, only one view (Y_1 or Y_2) shall be required for devices supplied (reference note 14/ of Table I, Method 5004, of MIL-STD-883).

f. Steady-state total dose irradiation. For lot supplied against this drawing, the manufacturer shall perform steady-state total dose irradiation using a Cobalt 60 (gamma) source to a level of 100 kilorads (Si), minimum, in accordance with the requirements of MIL-STD-883, Method 1019 and Method 5005, Group E, subgroup 2. The bias circuit shall be as specified in Figure 6C herein.

g. Read and record requirements. The manufacturer shall read and record and perform delta calculations for those parameters as specified in Table 5 herein.

h. Percent defective allowable (PDA). Percent defective allowable (PDA) shall be 5% or one device, whichever is greater, calculated through each burn-in test separately. This PDA shall be based on failures from Group A, subgroup 1 plus deltas combined. In addition, there shall be a separate PDA of 3% based on failures from Group A, subgroup 7. Lots and sublots may be resubmitted for burn-in one time only and may be resubmitted only when the PDA does not exceed 20%. Resubmitted inspection lots, lot splits, and sublots shall be kept separate from new lots and sublots and shall be inspected for all specified characteristics using a tightened inspection PDA equal to the next lower number in the LTPD series of Appendix B of MIL-STD-38510, or one device, whichever is greater.

i. Customer source inspection. Customer source inspection shall be required at either the pre-cap and/or final inspection points and only when specifically required by the individual purchase order (reference 3.15 and 4.5 herein).

j. Electrical test parameters. Interim and final electrical test parameters shall be specified in Table 2B herein.

k. AC measurements and timing diagrams. AC measurements and timing waveforms shall be specified in Figure 7 and Figures 8A through 8G herein.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883, product assurance level S, including Groups A, B, and D inspections except as shown in Tables 3 and 4 herein for small lot Groups B and D inspections. Devices used for Groups B and D inspections are to be over and above flight quantities specified on the purchase order and are considered as deliverable items against the purchase order (reference 5.3 herein).

4.3.1 Group A inspection.

a. Tests shall be as specified in Table 2B herein.

b. Subgroups 4, 5, and 6 in Table I, Method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7, 8A, and 8B shall consist of verifying the functionality of the device. These tests form a part of the manufacturer's test tape and shall be maintained by the manufacturer and available for review by the acquiring activity (see 3.4.2, 3.10 and 3.14 herein).

4.3.2 Groups B and D inspections.

a. Small lot sampling plan as specified in Table 3 and 4 herein.

b. End-point electrical parameters shall be as specified in Table 2B herein.

c. Steady-state life test, Method 1005 of MIL-STD-883 conditions.

(1) Test Condition D using the circuit as specified in Figure 6B herein.

(2) T_A = +125°C. Accelerated life test shall **not** be permitted.

(3) Test duration: 1,000 hours, minimum. Accelerated life test shall **not** be permitted.

4.4 Test data. All data requirements as defined in section 5.2 herein.

4.4.1 Delivery of data. All data and parts shall be sent to the addressee listed on the purchase order (reference 3.19 and 5.2 herein).

4.4.2 Technical requests. Any technical questions pertaining an existing order should be directed to the addressee listed on the purchase order.

4.5 Responsibility for inspection.

4.5.1 Manufacturer. The manufacturer is responsible for controlling the quality of his product and offering to the Procuring Activity only those parts that conform to all specified requirements.

4.5.2 Liability of source inspection. Source inspection at the manufacturer's facility, or at the manufacturer's source (and any other facility) does not relieve the manufacturer of responsibility to furnish to the Procuring Activity an acceptable end-product, as stipulated by contract or purchase order; nor does it indicate that parts supplied the manufacturer will be accepted at the Procuring Activity's facility. Final acceptance of the end-product shall be at the Procuring Activity's facility.

4.6 Alternate test methods. Other test methods or circuits may be substituted for those specified herein provided it is demonstrated to the Procuring Activity that such a substitution meets or exceeds the requirements of this drawing and written approval is obtained prior to use.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

5.2 Data package requirements. All lots of devices shipped shall include a data package containing the following items:

a. Cover sheet. As a minimum, the cover sheet is to include:

(1) Purchase order number and revision

(2) Customer part number as found in paragraph 1.2 herein.

(3) Lot date code

(4) Harris part number

(5) Lot number

(6) Quantity

b. Certificate of conformance. May be included as part of the shipper.

c. Lot serial number sheet. Good device serial numbers and lot number.

d. Screening attributes data. The attributes data supplied shall be from post-encapsulation screening through end of 100% screening operations. As a minimum, this data shall include:

(1) Identification the test operation(s).

(2) Quantity of devices subjected to each test operation.

(3) Quantity of devices accepted at the conclusion of each test operation.

(4) Date on which each test operation was performed.

e. Variables data for all read and record and delta operations performed. Each value shall be identified to the specific serial number of the device for which the data represents.

f. Group A attributes data summary.

g. Groups B and D inspection data summary, when required to be performed (see paragraphs 4.3.2 and 5.3 herein).

h. Wafer lot acceptance report (MIL-STD-883, Method 5007) to include SEM photographs (not photocopies). The SEM photographs shall include the percentage of step coverage.

i. Radiographic (X-Ray) inspection report and film(s). The film(s) shall include penetrameter measurements.

j. Gamma total dose radiation report with the initial shipment of devices from the same wafer lot.

k. Fault coverage certification and methodology used.

l. Rework documentation (if applicable).

5.3 Group B and D devices. Groups B and D devices shall be packaged separately from deliverable devices and marked as such. Groups B and D devices are over and above flight quantities and are considered to be deliverables against the purchase order (see paragraph 4.3 herein). NOTE: Subgroup B5 Life Test Units are to handled in a manner consistent to that of nondestructive flight units.

5.4 Shipping container. The shipping container shall be legibly marked with the following information:

(a) Purchase order number.

(b) Device Part number (see paragraph 1.2).

(c) The actual manufacturer's name, registered trademark or H4 code identification number.

5.5 Delivery of data. Delivery of data and parts or any technical questions regarding an existing purchase order shall be directed to the addressee on the purchase order (see paragraph 4.4 herein).

6. NOTES

6.1 Ordering data. Procurement documents shall specify the following:

(a) Title, number and date of this and the applicable detail specification.

(b) Device part number (see 1.2).

6.2 Qualification provisions. With respect to products requiring qualification, awards will be made only for products which have been tested and approved by GSFC before the time for opening of bids. The attention of the suppliers is called to this requirement: manufacturers should arrange to have qualification tests made on products which they propose to offer to GSFC to become eligible for awards of contracts or order for products covered by this specification. The manufacturer shall bear the cost of qualification inspection to this specification. Information pertaining to qualification of product may be obtained from the activity whose address is listed in 6.4.

6.2.1 NOTICE. When GSFC drawings, specifications, or other data are sent for any purpose other than in connection with a definitely related GSFC procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever. The fact that GSFC may have formulated, furnished or in any way supplied said drawings, specifications, or other data, is not to be regarded by implication or otherwise as in any manner licensing the holder or any persons or corporations, or conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

6.3 Preparing activity. The identification and contact address of the preparing activity shall be as follows:

Custodian:
Goddard Space Flight Center
Greenbelt, MD. 20771

ATTN: QPL Administrator
Code 311.2

Attachments Specification Sheets

FIGURES

Attachments Specification Sheets

TABLES

Manufacturer Part Number	S-311-721 Dash Number
RTX2010RH2101	Device Type 001 (ref. para. 1.2.1)
RTX2010RH2102	Device Type 002 (ref. para. 1.2.1)

FIGURE 1. PART NUMBER TYPE

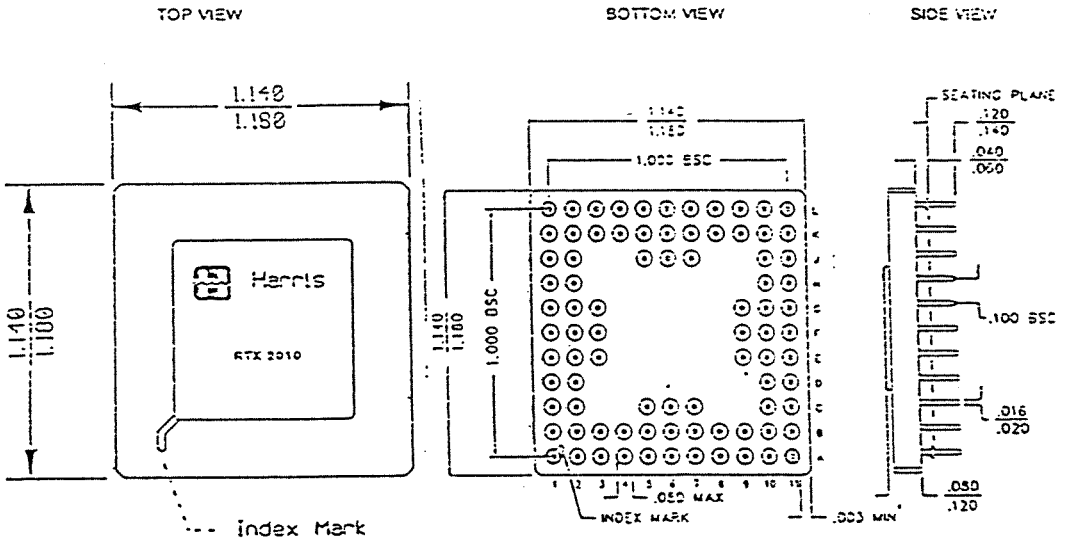


FIGURE 2A. CASE OUTLINE (84 Pin Grid Array)

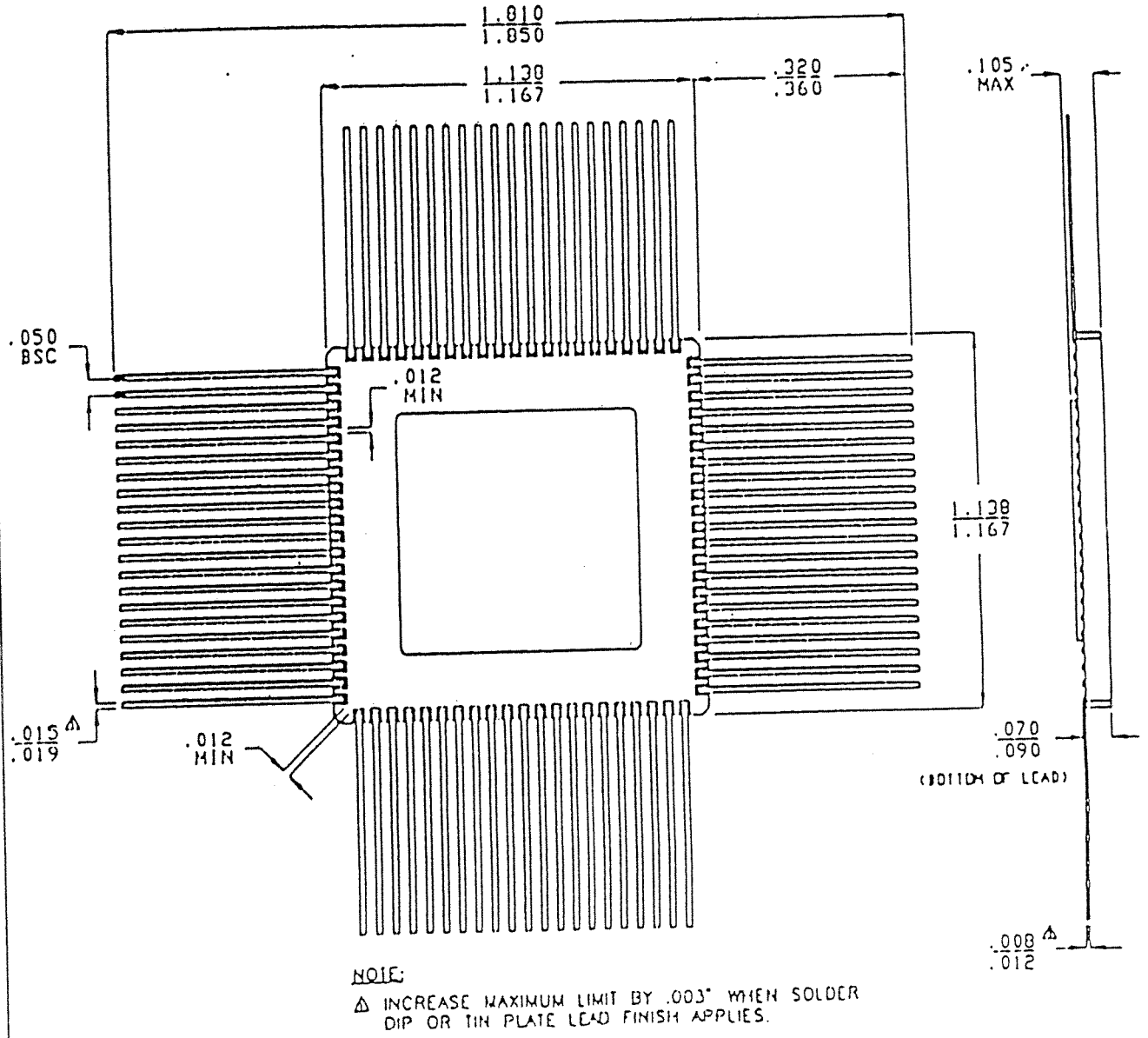


FIGURE 2B. CASE OUTLINE (84 Pin Quad Flatpack)

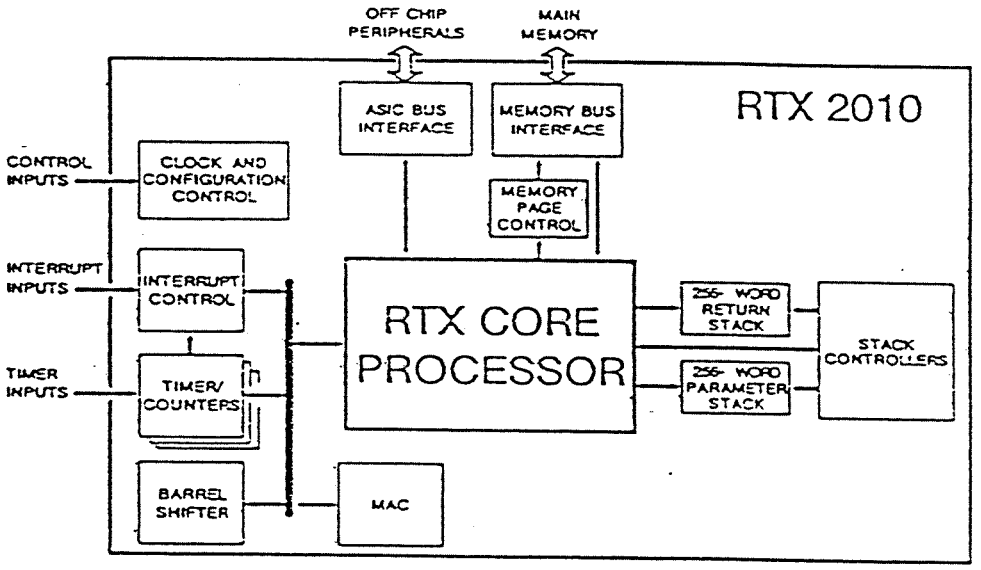


FIGURE 3. FUNCTIONAL DIAGRAM

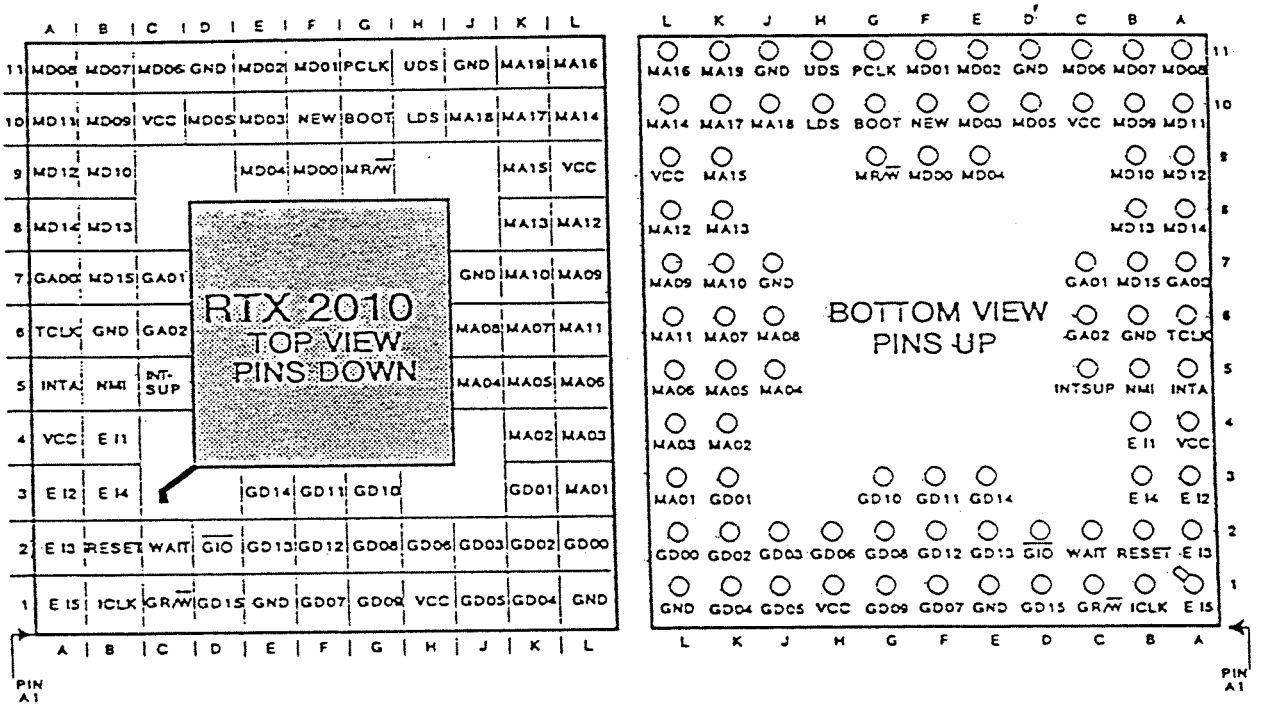


FIGURE 4A. TERMINAL CONNECTIONS/SIGNAL ASSIGNMENTS
(84 Pin Grid Array)

PLCC LEAD	PGA PIN	SIGNAL NAME	TYPE
1	C6	GA02	Output; Address Bus
2	A6	TCLK	Output
3	A5	INTA	Output
4	B5	NMI	Input
5	C5	INTSUP	Input
6	A4	VCC	Power
7	B4	EI1	Input
8	A3	EI2	Input
9	A2	EI3	Input
10	B3	EI4	Input
11	A1	EI5	Input
12	B2	RESET	Input
13	C2	WAIT	Input
14	B1	ICLK	Input
15	C1	GR/$\overline{W}$	Output
16	D2	$\overline{GIO}$	Output
17	D1	GD15	I/O; Data Bus
18	E3	GD14	I/O; Data Bus
19	E2	GD13	I/O; Data Bus
20	E1	GND	Ground
21	F2	GD12	I/O; Data Bus
22	F3	GD11	I/O; Data Bus
23	G3	GD10	I/O; Data Bus
24	G1	GD09	I/O; Data Bus
25	G2	GD08	I/O; Data Bus
26	F1	GD07	I/O; Data Bus
27	H1	VCC	Power
28	H2	GD06	I/O; Data Bus
29	J1	GD05	I/O; Data Bus
30	K1	GD04	I/O; Data Bus
31	J2	GD03	I/O; Data Bus
32	L1	GND	Ground
33	K2	GD02	I/O; Data Bus
34	K3	GD01	I/O; Data Bus
35	L2	GD00	I/O; Data Bus
36	L3	MA01	Output; Address Bus
37	K4	MA02	Output; Address Bus
38	L4	MA03	Output; Address Bus
39	J5	MA04	Output; Address Bus
40	K5	MA05	Output; Address Bus
41	L5	MA06	Output; Address Bus
42	K6	MA07	Output; Address Bus
43	J6	MA08	Output; Address Bus
44	J7	GND	Ground
45	L7	MA09	Output; Address Bus
46	K7	MA10	Output; Address Bus
47	L6	MA11	Output; Address Bus
48	L8	MA12	Output; Address Bus
49	K8	MA13	Output; Address Bus
50	L9	VCC	Power
51	L10	MA14	Output; Address Bus
52	K9	MA15	Output; Address Bus
53	L11	MA16	Output; Address Bus
54	K10	MA17	Output; Address Bus
55	J10	MA18	Output; Address Bus
56	K11	MA19	Output; Address Bus
57	J11	GND	Ground
58	H10	LDS	Output
59	H11	UDS	Output
60	F10	NEW	Output
61	G10	BOOT	Output
62	G11	PCLK	Output
63	G9	MR/$\overline{W}$	Output
64	F9	MD00	I/O; Data Bus
65	F11	MD01	I/O; Data Bus
66	E11	MD02	I/O; Data Bus
67	E10	MD03	I/O; Data Bus
68	E9	MD04	I/O; Data Bus
69	D11	GND	Ground
70	D10	MD05	I/O; Data Bus
71	C11	MD06	I/O; Data Bus
72	B11	MD07	I/O; Data Bus
73	C10	VCC	Power
74	A11	MD08	I/O; Data Bus
75	B10	MD09	I/O; Data Bus
76	B9	MD10	I/O; Data Bus
77	A10	MD11	I/O; Data Bus
78	A9	MD12	I/O; Data Bus
79	B8	MD13	I/O; Data Bus
80	A8	MD14	I/O; Data Bus
81	B6	GND	Ground
82	B7	MD15	I/O; Data Bus
83	A7	GA00	Output; Address Bus
84	C7	GA01	Output; Address Bus

FIGURE 4A. TERMINAL CONNECTIONS/SIGNAL ASSIGNMENTS
(84 Pin Grid Array)
(continued)

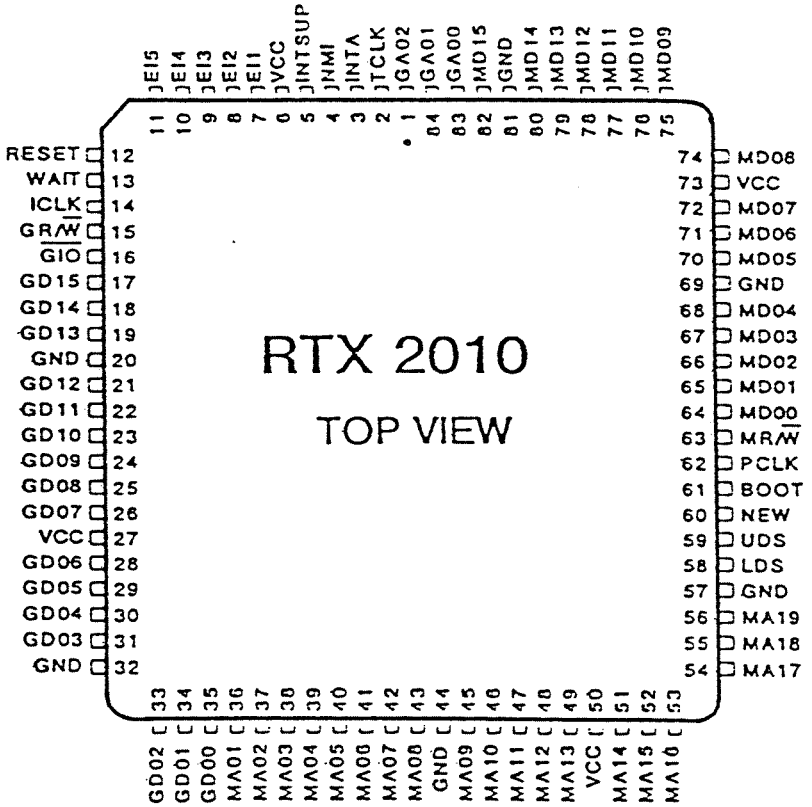


FIGURE 4B. TERMINAL CONNECTIONS/SIGNAL ASSIGNMENTS
(84 Pin Quad Flatpack)

LEAD	SIGNAL NAME	TYPE
1	GA02	Output, Address Bus
2	TCLK	Output
3	INTA	Output
4	NMI	Input
5	INTSUP	Input
6	VCC	Power
7	EI1	Input
8	EI2	Input
9	EI3	Input
10	EI4	Input
11	EI5	Input
12	RESET	Input
13	WAIT	Input
14	ICLK	Input
15	GR/W	Output
16	GIO	Output
17	GD15	I/O, Data Bus
18	GD14	I/O, Data Bus
19	GD13	I/O, Data Bus
20	GND	Ground
21	GD12	I/O, Data Bus
22	GD11	I/O, Data Bus
23	GD10	I/O, Data Bus
24	GD09	I/O, Data Bus
25	GD08	I/O, Data Bus
26	GD07	I/O, Data Bus
27	VCC	Power
28	GD06	I/O, Data Bus
29	GD05	I/O, Data Bus
30	GD04	I/O, Data Bus
31	GD03	I/O, Data Bus
32	GND	Ground
33	GD02	I/O, Data Bus
34	GD01	I/O, Data Bus
35	GD00	I/O, Data Bus
36	MA01	Output, Address Bus
37	MA02	Output, Address Bus
38	MA03	Output, Address Bus
39	MA04	Output, Address Bus
40	MA05	Output, Address Bus
41	MA06	Output, Address Bus
42	MA07	Output, Address Bus

LEAD	SIGNAL NAME	TYPE
43	MA08	Output, Address Bus
44	GND	Ground
45	MA09	Output, Address Bus
46	MA10	Output, Address Bus
47	MA11	Output, Address Bus
48	MA12	Output, Address Bus
49	MA13	Output, Address Bus
50	VCC	Power
51	MA14	Output, Address Bus
52	MA15	Output, Address Bus
53	MA16	Output, Address Bus
54	MA17	Output, Address Bus
55	MA18	Output, Address Bus
56	MA19	Output, Address Bus
57	GND	Ground
58	LDS	Output
59	UDS	Output
60	NEW	Output
61	BOOT	Output
62	PCLK	Output
63	MR/W	Output
64	MD00	I/O, Data Bus
65	MD01	I/O, Data Bus
66	MD02	I/O, Data Bus
67	MD03	I/O, Data Bus
68	MD04	I/O, Data Bus
69	GND	Ground
70	MD05	I/O, Data Bus
71	MD06	I/O, Data Bus
72	MD07	I/O, Data Bus
73	VCC	Power
74	MD08	I/O, Data Bus
75	MD09	I/O, Data Bus
76	MD10	I/O, Data Bus
77	MD11	I/O, Data Bus
78	MD12	I/O, Data Bus
79	MD13	I/O, Data Bus
80	MD14	I/O, Data Bus
81	GND	Ground
82	MD15	I/O, Data Bus
83	GA00	Output, Address Bus
84	GA01	Output, Address Bus

FIGURE 4B. TERMINAL CONNECTIONS/SIGNAL ASSIGNMENTS
(84 Pin Quad Flatpack)
(continued)

SIGNAL	LEAD	RESET LEVEL	DESCRIPTION
NEW	60	1	NEW: A HIGH on this pin indicates that an instruction Fetch is in progress.
BOOT	61	1	BOOT: A HIGH on this pin indicates that Boot Memory is being accessed. This pin can be set or reset by accessing bit 3 of the Configuration Register.
MR/$\overline{W}$	63	1	MEMORY READ/WRITE: A LOW on this pin indicates that a Memory Write operation is in progress.
UDS	59	1	UPPER DATA SELECT: A HIGH on this pin indicates that the high byte of memory (MD15-MD08) is being accessed.
LDS	58	1	LOWER DATA SELECT: A HIGH on this pin indicates that the low byte of memory (MD07 - MD00) is being accessed.
$\overline{GIO}$	16	1	ASIC I/O: A LOW on this pin indicates that an ASIC Bus operation is in progress.
GR/$\overline{W}$	15	1	ASIC READ/WRITE: A LOW on this pin indicates that an ASIC Bus Write operation is in progress.
PCLK	62	0	PROCESSOR CLOCK: Runs at half the frequency of ICLK. All processor cycles begin in the rising edge of PCLK. Held low extra cycles when WAIT is asserted.
TCLK	2	0	TIMING CLOCK: Same frequency and phase as PCLK but continues running WAIT cycles.
INTA	3	0	INTERRUPT ACKNOWLEDGE: A HIGH on this pin indicates that an Interrupt Acknowledge cycle is in progress.

FIGURE 5A. OUTPUT SIGNAL DESCRIPTIONS

SIGNAL	LEAD	DESCRIPTION
WAIT	13	WAIT: A HIGH on this pin causes PCLK to be held LOW and the current cycle to be extended.
ICLK	14	INPUT CLOCK: Internally divided by 2 to generate all on-chip timing (CMOS input levels).
RESET	12	A HIGH level on this pin resets the RTX. Must be held high for at least 4 rising edges of ICLK plus 1/2 ICLK cycle setup and hold times. (Schmitt trigger CMOS input levels.)
EI2,EI1	8, 7	EXTERNAL INTERRUPTS 2, 1: Active HIGH level-sensitive inputs to the Interrupt Controller. Sampled on the rising edge of PCLK. See Timing Diagrams for detail.
EI5-EI3	11 - 9	EXTERNAL INTERRUPTS 5, 4, 3: Dual purpose inputs; active HIGH level-sensitive Interrupt Controller inputs; active HIGH edge-sensitive Timer/Counter inputs. As interrupt inputs, they are sampled on the rising edge of PCLK. See Timing Diagrams for detail.
NMI	4	NON-MASKABLE INTERRUPT: Active HIGH edge-sensitive Interrupt Controller input capable of interrupting any processor cycle when NMI is set to Mode 0. See Interrupt Suppression and Interrupt Controller Sections. (Schmitt trigger CMOS input levels.)
INTSUP	5	INTERRUPT SUPPRESS: A HIGH in this pin inhibits all maskable interrupts, internal and external.

FIGURE 5B. INPUT SIGNAL DESCRIPTIONS

SIGNAL	LEAD	DESCRIPTION
GA02	1	ASIC ADDRESSES: 3-bit ASIC Address Bus which carries address information for Main Memory.
GA01	84	
GA00	83	
MA19 - MA14	56 - 51	MEMORY ADDRESSES: 19-bit Memory Address Bus which carries address information for Main Memory.
MA13 - MA09	49 - 45	
MA08 - MA01	43 - 36	

FIGURE 5C. ADDRESS BUS (OUTPUTS) DESCRIPTIONS

SIGNAL	LEAD	DESCRIPTION
GD15 - GD13	17 -	ASIC DATA: 16-bit bidirectional external ASIC Data Bus which carries data to and from off-chip I/O devices.
GD12 - GD07	21 - 26	
GD06 - GD03	28 - 31	
GD02 - GD00	33 - 35	
MD15	82	MEMORY DATA: 16-bit bidirectional Memory Data Bus which carries data to and from Main Memory.
MD14 - MD08	80 - 74	
MD07 - MD05	72 - 70	
MD04 - MD00	68 - 64	

FIGURE 5D. DATA BUS (I/O) DESCRIPTIONS

SIGNAL	LEAD	DESCRIPTION
VCC	6, 27, 50, 73	Power supply +5 Volt connection. A 0.1 uF, low impedance decoupling capacitor should be placed between VCC and GND. This should be located as close as to the RTX package as possible.
GND	20, 32, 44, 57, 69, 81	Power supply ground return connections.

FIGURE 5E. POWER CONNECTION DESCRIPTIONS

QFP PIN #	PGA PIN #	PIN NAME	PIN FUNCT	RESIST.	LEVEL/ SIGNAL
1	C6	GA02	O	--	NC
2	A6	TCLK	O	--	NC
3	A5	INTA	O	--	NC
4	B5	NMI	I	47K	GND
5	C5	INTSUP	I	47K	VDD
6	A4	VDD	PWR	--	VDD
7	B4	EI1	I	47K	GND
8	A3	EI2	I	47K	GND
9	A2	EI3	I	47K	GND
10	B3	EI4	I	47K	GND
11	A1	EI5	I	47K	GND
12	B2	RST	I	47K	VDD
13	C2	WAIT	I	47K	GND
14	B1	ICLK	I	47K	SEENOTE 2
15	C1	GRW*	O	--	NC
16	D2	GIO*	O	--	NC
17	D1	GD15	I/O	47K	VDD
18	E3	GD14	I/O	47K	GND
19	E2	GD13	I/O	47K	VDD
20	B6	VSS	PWR	--	GND
21	F2	GD12	I/O	47K	GND
22	F3	GD11	I/O	47K	VDD
23	G3	GD10	I/O	47K	GND
24	G1	GD09	I/O	47K	VDD
25	G2	GD08	I/O	47K	GND
26	F1	GD07	I/O	47K	VDD
27	C10	VDD	PWR	--	VDD
28	H2	GD06	I/O	47K	GND
29	J1	GD05	I/O	47K	VDD
30	K1	GD04	I/O	47K	GND
31	J2	GD03	I/O	47K	VDD
32	D11	VSS	PWR	--	GND
33	K2	GD02	I/O	47K	GND
34	K3	GD01	I/O	47K	VDD
35	L2	GD00	I/O	47K	GND
36	L3	MA01	O	--	NC
37	K4	MA02	O	--	NC
38	L4	MA03	O	--	NC
39	J5	MA04	O	--	NC
40	K5	MA05	O	--	NC
41	L5	MA06	O	--	NC
42	K6	MA07	O	--	NC

FIGURE 6A. STATIC BURN-IN TEST CIRCUIT

43	J6	MA08	O	--	NC
44	E1	VSS	PWR	--	GND
45	L7	MA09	O	--	NC
46	K7	MA10	O	--	NC
47	L6	MA11	O	--	NC
48	L8	MA12	O	--	NC
49	K8	MA13	O	--	NC
50	H1	VDD	PWR	--	VDD
51	L10	MA14	O	--	NC
52	K9	MA15	O	--	NC
53	L11	MA16	O	--	NC
54	K10	MA17	O	--	NC
55	J10	MA18	O	--	NC
56	K11	MA19	O	--	NC
57	J11	VSS	PWR	--	GND
58	H10	LDS	O	--	NC
59	H11	UDS	O	--	NC
60	F10	NEW	O	--	NC
61	G10	BOOT	O	--	NC
62	G11	PCLK	O	--	NC
63	G9	MRW*	O	--	NC
64	F9	MD00	I/O	47K	VDD
65	F11	MD01	I/O	47K	GND
66	E11	MD02	I/O	47K	VDD
67	E10	MD03	I/O	47K	GND
68	E9	MD04	I/O	47K	VDD
69	J7	VSS	PWR	--	GND
70	D10	MD05	I/O	47K	GND
71	C11	MD06	I/O	47K	VDD
72	B11	MD07	I/O	47K	GND
73	L9	VDD	PWR	--	VDD
74	A11	MD08	I/O	47K	VDD
75	B10	MD09	I/O	47K	GND
76	B9	MD10	I/O	47K	VDD
77	A10	MD11	I/O	47K	GND
78	A9	MD12	I/O	47K	VDD
79	B8	MD13	I/O	47K	GND
80	A8	MD14	I/O	47K	VDD
81	L1	VSS	PWR	--	GND
82	B7	MD15	I/O	47K	GND
83	A7	GA00	O	--	NC
84	C7	GA01	O	--	NC

NOTES: 1. VDD = 6.0 ± 0.5 VOLTS
2. APPLY A MINIMUM OF 10 ICLK PULSES AFTER POWER-UP PULSES ARE 50% DUTY CYCLE SQUARE WAVE, PERIOD > 5US AFTER INITIAL PULSES, ICLK IS LEFT HIGH

FIGURE 6A. STATIC BURN-IN TEST CIRCUIT (continued)

QFP PIN #	PGA PIN #	PIN NAME	PIN FUNCT	RESIST.	LEVEL/ SIGNAL
1	C6	GA02	O	47K	VDD/2
2	A6	TCLK	O	47K	VDD/2
3	A5	INTA	O	47K	VDD/2
4	B5	NMI	I	47K	F12
5	C5	INTSUP	I	47K	F13
6	A4	VDD	PWR	N/A	VDD
7	B4	EI1	I	47K	F11
8	A3	EI2	I	47K	F10
9	A2	EI3	I	47K	F9
10	B3	EI4	I	47K	F9
11	A1	EI5	I	47K	F9
12	B2	RST	I	47K	SEE NOTE 6
13	C2	WAIT	I	47K	GND
14	B1	ICLK	I	47K	F0
15	C1	GRW*	O	47K	VDD/2
16	D2	GIO*	O	47K	VDD/2
17	D1	GD15	I/O	47K	F1
18	E3	GD14	I/O	47K	F2
19	E2	GD13	I/O	47K	F3
20	B6	VSS	PWR	N/A	GND
21	F2	GD12	I/O	47K	F4
22	F3	GD11	I/O	47K	F5
23	G3	GD10	I/O	47K	F6
24	G1	GD09	I/O	47K	F7
25	G2	GD08	I/O	47K	F8
26	F1	GD07	I/O	47K	F1
27	C10	VDD	PWR	N/A	VDD
28	H2	GD06	I/O	47K	F2
29	J1	GD05	I/O	47K	F3
30	K1	GD04	I/O	47K	F4
31	J2	GD03	I/O	47K	F5
32	D11	VSS	PWR	N/A	GND
33	K2	GD02	I/O	47K	F6
34	K3	GD01	I/O	47K	F7
35	L2	GD00	I/O	47K	F8
36	L3	MA01	O	47K	VDD/2
37	K4	MA02	O	47K	VDD/2
38	L4	MA03	O	47K	VDD/2
39	J5	MA04	O	47K	VDD/2
40	K5	MA05	O	47K	VDD/2
41	L5	MA06	O	47K	VDD/2
42	K6	MA07	O	47K	VDD/2
43	J6	MA08	O	47K	VDD/2

FIGURE 6B. DYNAMIC BURN-IN AND LIFE TEST CIRCUIT

44	E1	VSS	PWR	N/A	GND
45	L7	MA09	O	47K	VDD/2
46	K7	MA10	O	47K	VDD/2
47	L6	MA11	O	47K	VDD/2
48	L8	MA12	O	47K	VDD/2
49	K8	MA13	O	47K	VDD/2
50	H1	VDD	PWR	N/A	VDD
51	L10	MA14	O	47K	VDD/2
52	K9	MA15	O	47K	VDD/2
53	L11	MA16	O	47K	VDD/2
54	K10	MA17	O	47K	VDD/2
55	J10	MA18	O	47K	VDD/2
56	K11	MA19	O	47K	VDD/2
57	J11	VSS	PWR	N/A	GND
58	H10	LDS	O	47K	VDD/2
59	H11	UDS	O	47K	VDD/2
60	F10	NEW	O	47K	VDD/2
61	G10	BOOT	O	47K	VDD/2
62	G11	PCLK	O	47K	VDD/2
63	G9	MRW*	O	47K	VDD/2
64	F9	MD00	I/O	47K	F1
65	F11	MD01	I/O	47K	F2
66	E11	MD02	I/O	47K	F3
67	E10	MD03	I/O	47K	F4
68	E9	MD04	I/O	47K	F5
69	J7	VSS	PWR	N/A	GND
70	D10	MD05	I/O	47K	F6
71	C11	MD06	I/O	47K	F7
72	B11	MD07	I/O	47K	F8
73	L9	VDD	PWR	N/A	VDD
74	A11	MD08	I/O	47K	F1
75	B10	MD09	I/O	47K	F2
76	B9	MD10	I/O	47K	F3
77	A10	MD11	I/O	47K	F4
78	A9	MD12	I/O	47K	F5
79	B8	MD13	I/O	47K	F6
80	A8	MD14	I/O	47K	F7
81	L1	VSS	PWR	N/A	GND
82	B7	MD15	I/O	47K	F8
83	A7	GA00	O	47K	VDD/2
84	C7	GA01	O	47K	VDD/2

NOTES:
1. VDD = 6.0 ± 0.5 VOLTS
2. F0 = 100KHZ, 50% DUTY CYCLE SQUARE WAVE
3. F1 = F0/2, F2 = F1/2,.....
4. INPUT VOLTAGE LOW: VIL = -0.2V TO +0.4V
5. INPUT VOLTAGE HIGH: VIH = 4.5V +/- 10%
6. PULSE RST HIGH FOR 100US AFTER EVERY 2ND CYCLE OF F13
7. FOR DYNAMIC LIFE TEST, VDD $\geq$ 6.0 VOLTS

FIGURE 6B. DYNAMIC BURN-IN AND LIFE TEST CIRCUIT (continued)

QFP PIN#	PGA PIN #	PIN NAME	PIN FUNCT	RESIST.	LEVEL/ SIGNAL
1	C6	GA02	O	47K	VDD
2	A6	TCLK	O	47K	VDD
3	A5	INTA	O	47K	VDD
4	B5	NMI	I	47K	GND
5	C5	INTSUP	I	47K	VDD
6	A4	VDD	PWR	--	VDD
7	B4	EI1	I	47K	GND
8	A3	EI2	I	47K	GND
9	A2	EI3	I	47K	GND
10	B3	EI4	I	47K	GND
11	A1	EI5	I	47K	GND
12	B2	RST	I	47K	VDD
13	C2	WAIT	I	47K	GND
14	B1	ICLK	I	47K	VDD (SEE NOTE 2)
15	C1	GRW*	O	47K	GND
16	D2	GIO*	O	47K	GND
17	D1	GD15	I/O	47K	VDD
18	E3	GD14	I/O	47K	VDD
19	E2	GD13	I/O	47K	VDD
20	B6	VSS	PWR	--	GND
21	F2	GD12	I/O	47K	VDD
22	F3	GD11	I/O	47K	VDD
23	G3	GD10	I/O	47K	VDD
24	G1	GD09	I/O	47K	VDD
25	G2	GD08	I/O	47K	VDD
26	F1	GD07	I/O	47K	VDD
27	C10	VDD	PWR	--	VDD
28	H2	GD06	I/O	47K	VDD
29	J1	GD05	I/O	47K	VDD
30	K1	GD04	I/O	47K	VDD
31	J2	GD03	I/O	47K	VDD
32	D11	VSS	PWR	--	GND
33	K2	GD02	I/O	47K	VDD
34	K3	GD01	I/O	47K	VDD
35	L2	GD00	I/O	47K	VDD
36	L3	MA01	O	47K	VDD
37	K4	MA02	O	47K	VDD
38	L4	MA03	O	47K	VDD
39	J5	MA04	O	47K	VDD
40	K5	MA05	O	47K	VDD
41	L5	MA06	O	47K	VDD
42	K6	MA07	O	47K	VDD

FIGURE 6C. STEADY STATE TOTAL DOSE IRRADIATION BIAS TEST CIRCUIT

43	J6	MA08	O	47K	VDD
44	E1	VSS	PWR	--	GND
45	L7	MA09	O	47K	VDD
46	K7	MA10	O	47K	VDD
47	L6	MA11	O	47K	VDD
48	L8	MA12	O	47K	VDD
49	K8	MA13	O	47K	VDD
50	H1	VDD	PWR	--	VDD
51	L10	MA14	O	47K	VDD
52	K9	MA15	O	47K	VDD
53	L11	MA16	O	47K	VDD
54	K10	MA17	O	47K	VDD
55	J10	MA18	O	47K	VDD
56	K11	MA19	O	47K	VDD
57	J11	VSS	PWR	--	GND
58	H10	LDS	O	47K	GND
59	H11	UDS	O	47K	GND
60	F10	NEW	O	47K	GND
61	G10	BOOT	O	47K	GND
62	G11	PCLK	O	47K	VDD
63	G9	MRW*	O	47K	GND
64	F9	MD00	I/O	47K	VDD
65	F11	MD01	I/O	47K	VDD
66	E11	MD02	I/O	47K	VDD
67	E10	MD03	I/O	47K	VDD
68	E9	MD04	I/O	47K	VDD
69	J7	VSS	PWR	--	GND
70	D10	MD05	I/O	47K	VDD
71	C11	MD06	I/O	47K	VDD
72	B11	MD07	I/O	47K	VDD
73	L9	VDD	PWR	--	VDD
74	A11	MD08	I/O	47K	VDD
75	B10	MD09	I/O	47K	VDD
76	B9	MD10	I/O	47K	VDD
77	A10	MD11	I/O	47K	VDD
78	A9	MD12	I/O	47K	VDD
79	B8	MD13	I/O	47K	VDD
80	A8	MD14	I/O	47K	VDD
81	L1	VSS	PWR	--	GND
82	B7	MD15	I/O	47K	VDD
83	A7	GA00	O	47K	VDD
84	C7	GA01	O	47K	VDD

NOTES: 1. VDD = 5.5 +/- 0.5
2. APPLY A MINIMUM OF 10 ICLK PULSES AFTER POWER-UP PULSES ARE 50% DUTY CYCLE SQUARE WAVE, PERIOD > 5US AFTER INITIAL PULSES, ICLK IS LEFT HIGH

FIGURE 6C. STEADY STATE TOTAL DOSE IRRADIATION BIAS TEST CIRCUIT (continued)

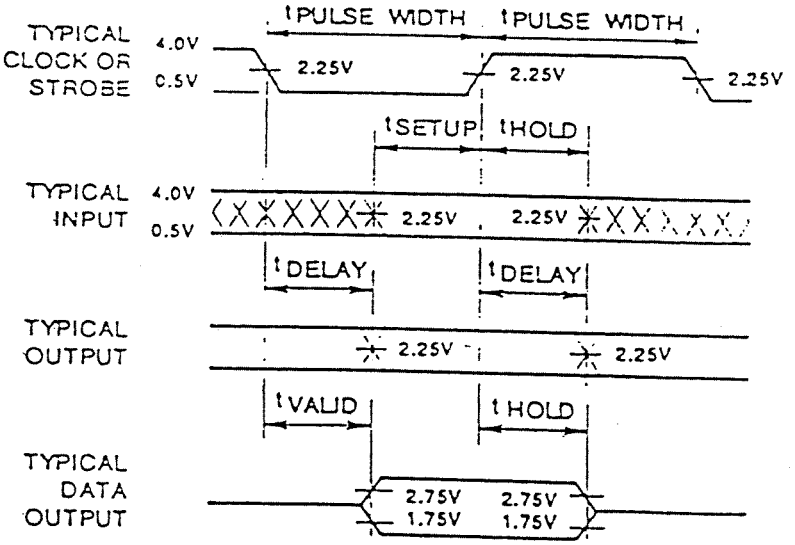
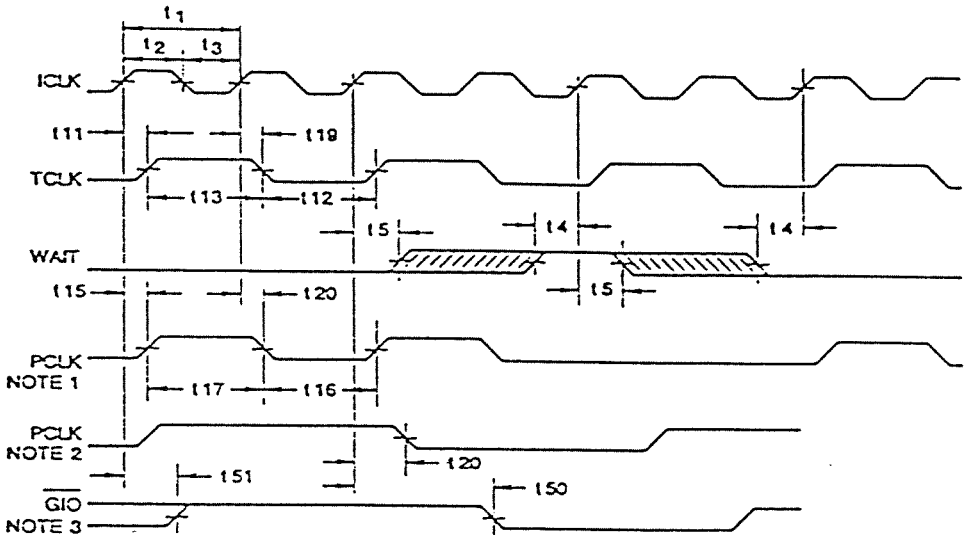


FIGURE 7. AC DRIVE AND MEASUREMENT POINTS - CLK INPUT



NOTES:

1. NORMAL CYCLE: This waveform describes a normal PCLK cycle and a PCLK cycle with a Wait state.
2. EXTENDED CYCLE: This waveform describes a PCLK cycle for a USER memory access or an external ASIC Bus read cycle when the CYCEXT bit or ARCE bit is set.
3. EXTENDED CYCLE: This waveform describes a $\overline{GIO}$ cycle for an external ASIC Bus read when the ARCE bit is set.
4. An active HIGH signal on the RESET input is guaranteed to reset the processor if its duration is greater than or equal to 4 rising edges of ICLK plus ½ ICLK cycle setup and hold times. If the RESET input is active for less than four rising edges of ICLK, the processor will not reset.

FIGURE 8A. TIMING DIAGRAMS-CLOCK AND WAIT TIMING

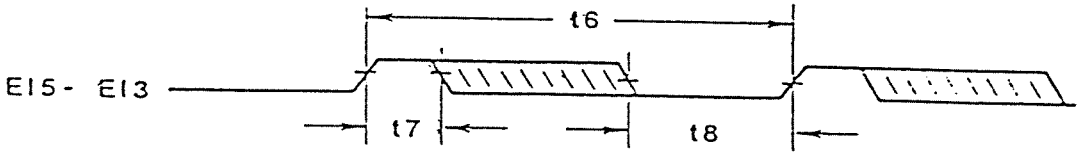
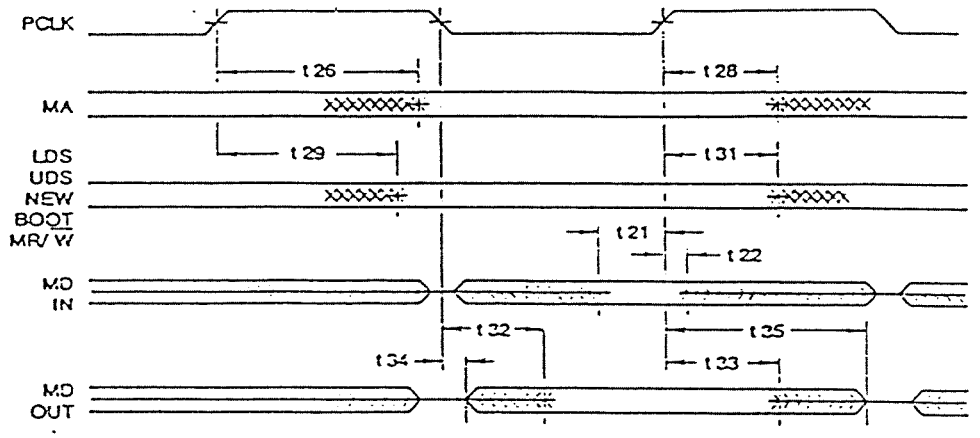


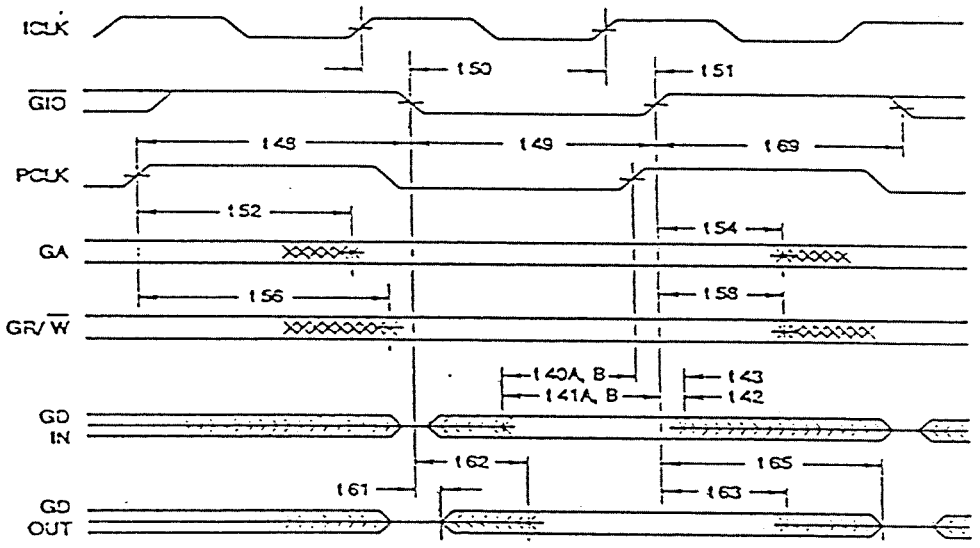
FIGURE 8B. TIMING DIAGRAMS-TIMER/COUNTER TIMING



NOTES: 1. If both LDS and UDS are low, no memory access is taking place in the current cycle. This only occurs during streamed instructions that do not access memory.

2. During a streamed single cycle instruction, the Memory Data Bus is driven by the processor.

FIGURE 8C. TIMING DIAGRAMS-MEMORY BUS TIMING



NOTES: 1. GIO remains high for internal ASIC bus cycles.

2. GR/W goes low and GD is driven for all ASIC write cycles, including internal ones.

3. During non-ASIC write cycles, GD is not driven by the RTX 2010. Therefore, it is recommended that all GD pins be pulled to VCC or GND to minimize power supply current and noise.

4. t40B and t41B specifications are for Streamed Mode of operation only.

FIGURE 8D. TIMING DIAGRAMS-ASIC BUS TIMING

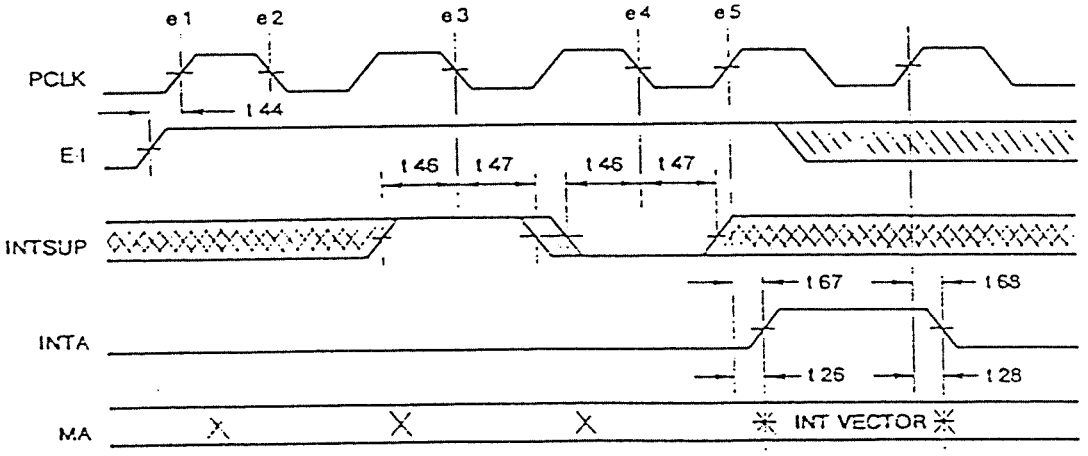


FIGURE 8E. TIMING DIAGRAMS-INTERRUPT TIMING: WITH INTERRUPT SUPPRESSION

NOTES: 1. Events in an interrupt sequence are as follows:

e1. The Interrupt Controller samples the interrupt request inputs on the rising edge of PCLK. If NMI rises between e1 and the rising edge of PCLK prior to e5, the interrupt vector will be for NMI.

e2. If any interrupt requests were sampled, the Interrupt Controller issues an interrupt request to the core on the falling edge of PCLK.

e3. The core samples the state of the interrupt requests from the Interrupt Controller on the falling edge of PCLK. If INTSUP is high, maskable interrupts will not be detected at this time.

e4. When the core samples an interrupt request on the falling edge of PCLK, an Interrupt Acknowledge cycle will begin on the next rising edge of PCLK.

e5. Following the detection of an interrupt request by the core, an Interrupt Acknowledge cycle begins. The interrupt vector will be based on the highest priority interrupt request active at this time.

2. t44 is only required to determine when the Interrupt Acknowledge cycle will occur.

3. Interrupt requests should be held active until the Interrupt Acknowledge cycle for that interrupt occurs.

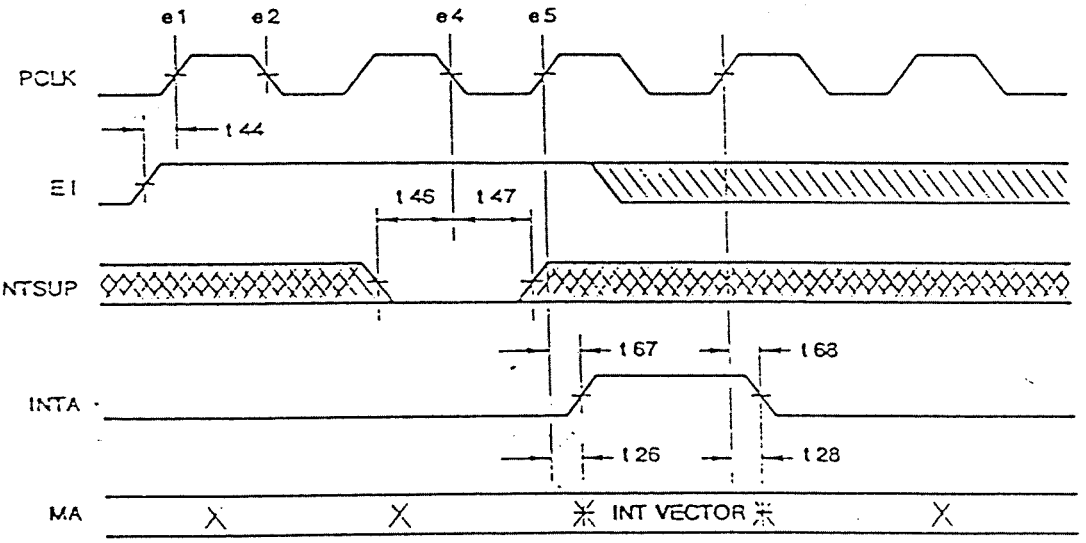
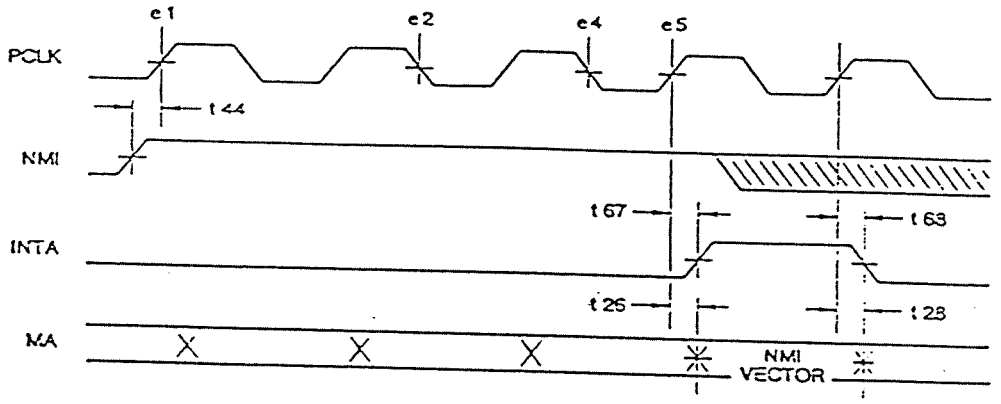


FIGURE 8F. TIMING DIAGRAMS-INTERRUPT TIMING: WITH NO INTERRUPT SUPPRESSION



Notes:

1. Events in an interrupt sequence are as follows:

   e1. The Interrupt Controller samples the Interrupt request inputs on the rising edge of PCLK. If NMI rises between e1 and the rising edge of PCLK prior to e5, the interrupt vector will be for NMI.

   e2. If any interrupt requests were sampled, the Interrupt Controller issues an interrupt request to the core on the falling edge of PCLK.

   e3. The core samples the state of the interrupt requests from the Interrupt Controller on the falling edge of PCLK. If INTSUP is high, maskable interrupts will not be detected at this time. e3 is not applicable to figures 8F and 8G herein.

   e4. When the core samples an interrupt request on the falling edge of PCLK, an interrupt Acknowledge cycle will begin on the next rising edge of PCLK.

   e5. Following the detection of an interrupt request by the core, an Interrupt Acknowledge cycle begins. The interrupt vector will be based on the highest priority interrupt request active at this time.

2. t44 is only required to determine when the Interrupt Acknowledge cycle will occur

3. Interrupt Requests should be held active until the Interrupt Acknowledge cycle for that interrupt occurs.

FIGURE 8G. TIMING DIAGRAMS-NON-MASKABLE INTERRUPT TIMING

NOTATIONS	
m-read	Read data (byte or word) from memory location addressed by contents of TOP Register into TOP Register.
m-write	Write contents (byte or word) of NEXT Register into memory location addressed by contents of TOP Register.
g-read	Read data from the ASIC address (address field *ggggg* of instruction) into TOP Register. A read of one of the on-chip peripheral registers can be done with a *g-read* command.
g-write	Write contents of TOP Register to ASIC address (address field *ggggg* of instruction). A write to one of the on-chip peripheral registers can be done with a *g-write* command.
u-read	Read contents (word only) of User Space location (address field *uuuuu* of instruction) into TOP Register.
u-write	Write contents (word only) of TOP Register into User Space location (address field *uuuuu* of instruction).
SWAP	Exchange contents of TOP and NEXT registers
DUP	Copy contents of TOP Register to NEXT Register, pushing previous contents of NEXT onto Stack Memory.
OVER	Copy contents of NEXT Register to TOP Register, pushing original contents of TOP to NEXT Register and original contents of NEXT Register to Stack Memory.
DROP	Pop Parameter Stack, discarding original contents of TOP Register, leaving the original contents of NEXT in TOP and the original contents of the top Stack Memory location in NEXT.
inv	Perform 1's complement on contents of TOP Register, if I bit in instruction is 1.
alu-op	Perform appropriate *cccc* or *aaa* ALU operation from Table 23 on contents of TOP and NEXT registers.
shift	Perform appropriate shift operation (*ssss* field of instruction) from Table 24 on contents of TOP and/or NEXT registers.
d	Push short literal *d* from *ddddd* field of instruction onto Parameter Stack (where *ddddd* contains the actual value of the short literal). The original contents of TOP are pushed into NEXT, and the original contents of NEXT are pushed onto Stack Memory.
D	Push long literal *D* from next sequential location in program memory onto Parameter Stack. The original contents of TOP are pushed into NEXT, and the original contents of NEXT are pushed onto Stack Memory.
R	Perform a Return From Subroutine if bit = 1.

NOTE: All unused opcodes are reserved for future architectural enhancements.

TABLE 1A. INSTRUCTION CODES-INSTRUCTION SET SUMMARY

FUNCTION CODE	DEFINITION
ggggg	Address field for ASIC Bus locations
uuuuu	Address field for User Space memory locations
cccc *aaa*	ALU functions (see Table 23)
ddddd	Short literals (containing a value from 0 to 31)
ssss	Shift Functions (see Table 24)

TABLE 1B. INSTRUCTION CODES-REGISTER BIT FIELDS (BY FUNCTION)

OPERATION *(g-read, g-write)*	RETURN BIT VALUE	ASIC ADDRESS *ggggg*	REGISTER	FUNCTION
Read mode	0	00000	[]	Pushes the contents of [] into TOP (with no pop of the Return Stack)
Read mode	1	00000	[]	Pushes the contents of [] into TOP, then performs a Subroutine Return
Write mode	0	00000	[]	Pops the contents of TOP into [] (with no push of the Return Stack)
Write mode	1	00000	[]	Performs a Subroutine Return, then pushes the contents of TOP into []
Read mode	0	00001	[]	Pushes the contents of [] into TOP, popping the Return Stack
Read mode	1	00001	[]	Pushes the contents of [] into TOP without popping the Return Stack, then executes the Subroutine Return
Write mode	0	00001	[]	Pushes the contents of TOP into [] popping the Parameter Stack
Write mode	1	00001	[]	Performs a Subroutine Return, then pushes the contents of TOP into []
Read mode	0	00010	[]	Pushes the contents of [] shifted left by one bit into TOP (the Return Stack is not popped)
Read mode	1	00010	[]	Pushes the contents of [] shifted left by one bit into TOP (the Return Stack is not popped), then performs a Subroutine Return
Write mode	0	00010	[]	Pushes the contents of TOP into [] as a "stream" count, indicating that the next instruction is to be performed a specified number of times; the Parameter Stack is popped
Write mode	1	00010	[]	Performs a Subroutine Return, then pushes the stream count into []
Read mode	0	00111	PC	Pushes the contents of PC into TOP
Read mode	1	00111	PC	Pushes the contents of PC into TOP, then performs a Subroutine Return
Write mode	0	00111	PC	Performs a Subroutine Call to the address contained in TOP, popping the Parameter Stack
Write mode	1	00111	PC	Pushes the contents of TOP onto the Return Stack before executing the Subroutine Return

* See the RTX Programmer's Reference Manual for a complete listing of typical software functions.

TABLE 1C. INSTRUCTION CODES-RTX2010 I AND PC ACCESS OPERATIONS*

INSTRUCTION CODE																OPERATION
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	0	1	1	0	0	0	0	1	0	R	0	1	1	0	1	Select IPR
1	0	1	1	0	0	0	0	0	0	R	0	1	1	0	1	Select CPR
1	0	1	1	0	0	0	0	1	0	R	1	0	0	0	0	Set SOFTINT
1	0	1	1	0	0	0	0	0	0	R	1	0	0	0	0	Clear SOFTINT

TABLE 1D. INSTRUCTION CODES-RESERVED I/O OPCODES

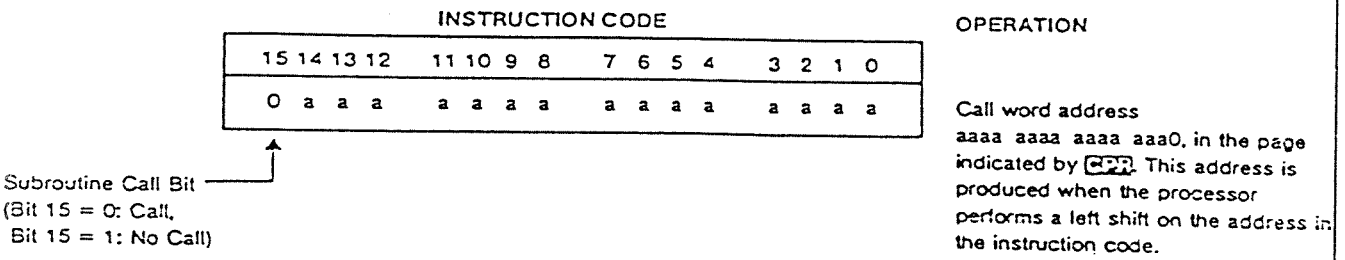
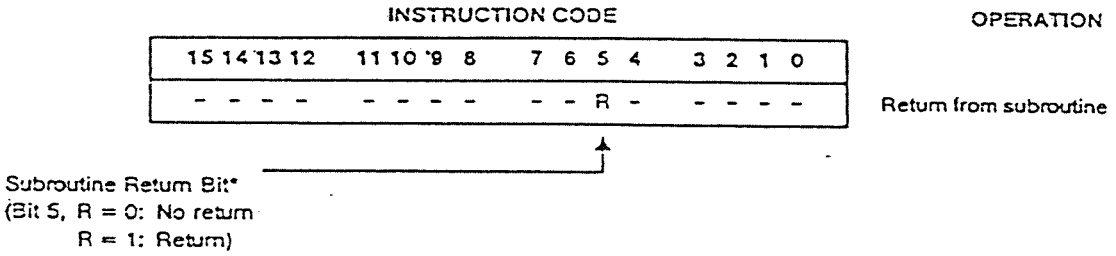
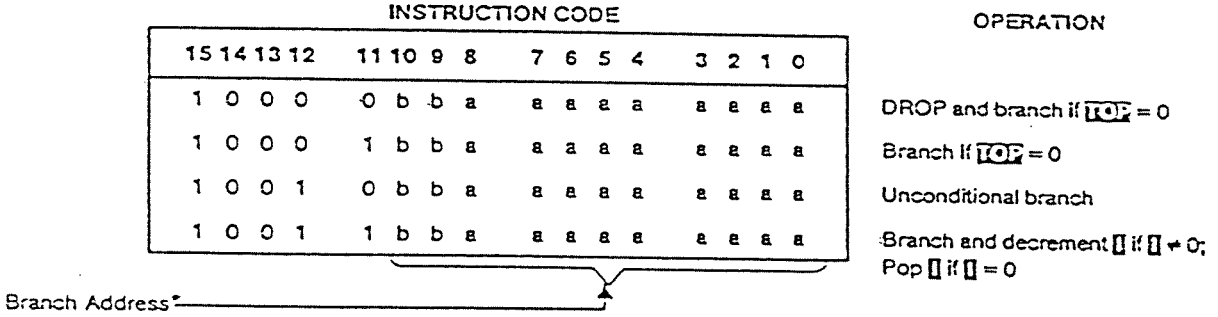


TABLE 1E. INSTRUCTION CODES-SUBROUTINE CALL INSTRUCTIONS



* Does not apply to Subroutine Call or Branch Instructions. A Subroutine Return can be combined with any other instruction (as implied here by hyphens).

TABLE 1F. INSTRUCTION CODES-SUBROUTINE RETURN



* See the Programmer's Reference Manual for further information regarding the branch address field.

TABLE 1G. INSTRUCTION CODES-BRANCH INSTRUCTIONS

INSTRUCTION CODE																OPERATION	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	(1ST CYCLE)	(2ND CYCLE)
1	0	1	1	0	0	0	i	0	0	R	g	g	g	g	g	*g-read* DROP	inv
1	0	1	1	1	1	1	i	0	0	R	g	g	g	g	g	*g-read*	inv
1	0	1	1	c	c	c	c	0	0	R	g	g	g	g	g	*g-read* OVER	alu-op
1	0	1	1	0	0	0	i	1	0	R	g	g	g	g	g	DUP *g-write*	inv
1	0	1	1	1	1	1	i	1	0	R	g	g	g	g	g	*g-write*	inv
1	0	1	1	c	c	c	c	1	0	R	g	g	g	g	g	*g-read* SWAP	alu-op

TABLE 1H. INSTRUCTION CODES-REGISTER AND I/O ACCESS INSTRUCTIONS

INSTRUCTION CODE																OPERATION	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	(1ST CYCLE)	(2ND CYCLE)
1	0	1	1	0	0	0	I	0	1	R	d	d	d	d	d	d DROP	inv
1	0	1	1	1	1	1	i	0	1	R	d	d	d	d	d	d	inv
1	0	1	1	c	c	c	c	0	1	R	d	d	d	d	d	d OVER	alu-op
1	0	1	1	1	1	1	I	1	1	R	d	d	d	d	d	d SWAP DROP	inv
1	0	1	1	c	c	c	c	1	1	R	d	d	d	d	d	d SWAP	alu-op

TABLE 1I. INSTRUCTION CODES-SHORT LITERAL INSTRUCTIONS

INSTRUCTION CODE																OPERATION	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	(1ST CYCLE)	(2ND CYCLE)
1	1	0	1	0	0	0	i	0	0	R	0	0	0	0	0	D SWAP	inv
1	1	0	1	1	1	1	i	0	0	R	0	0	0	0	0	D SWAP	SWAP inv
1	1	0	1	c	c	c	c	0	0	R	0	0	0	0	0	D SWAP	SWAP OVER alu-op
1	1	0	1	1	1	1	I	1	0	R	0	0	0	0	0	D SWAP	DROP inv
1	1	0	1	c	c	c	c	1	0	R	0	0	0	0	0	D SWAP	alu-op

TABLE 1J. INSTRUCTION CODES-LONG LITERAL INSTRUCTIONS

INSTRUCTION CODE																OPERATION	
																(1ST CYCLE)	(2ND CYCLE)
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
1	1	1	s	0	0	0	I	0	0	R	0	0	0	0	0	*m-read* SWAP	inv
1	1	1	s	1	1	1	i	0	0	R	0	0	0	0	0	*m-read* SWAP	SWAP inv
1	1	1	s	c	c	c	c	0	0	R	0	0	0	0	0	*m-read* SWAP	SWAP OVER alu-op
1	1	1	s	0	0	0	p	0	1	R	0	0	0	0	0	{SWAP DROP} DUP *m-read* SWAP	NOP
1	1	1	s	1	1	1	p	0	1	R	d	d	d	d	d	{SWAP DROP} *m-read d*	NOP
1	1	1	s	a	a	a	p	0	1	R	d	d	d	d	d	{SWAP DROP} DUP *m-read* SWAP d SWAP alu-op	NOP
1	1	1	s	0	0	0	i	1	0	R	0	0	0	0	0	OVER SWAP *m-write*	inv
1	1	1	s	1	1	1	i	1	0	R	0	0	0	0	0	OVER SWAP *m-write*	DROP inv
1	1	1	s	c	c	c	c	1	0	R	0	0	0	0	0	*m-read* SWAP	alu-op
1	1	1	s	0	0	0	p	1	1	R	0	0	0	0	0	{OVER SWAP} SWAP OVER *m-write*	NOP
1	1	1	s	1	1	1	p	1	1	R	d	d	d	d	d	{OVER SWAP} *m-write d*	NOP
1	1	1	s	a	a	a	p	1	1	R	d	d	d	d	d	{OVER SWAP} SWAP OVER *m-write* d SWAP alu-op	NOP

If s = 0, Memory is accessed by word
If s = 1, Memory is accessed by byte

If (p = 0), perform either {SWAP DROP} or {OVER SWAP}

Note: SWAP d SWAP = d ROT

TABLE 1K. INSTRUCTION CODES-MEMORY ACCESS INSTRUCTIONS

INSTRUCTION CODE																OPERATION	
																(1ST CYCLE)	(2ND CYCLE)
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
1	1	0	0	0	0	0	I	0	0	R	u	u	u	u	u	*u-read* SWAP	inv
1	1	0	0	1	1	1	i	0	0	R	u	u	u	u	u	*u-read* SWAP	SWAP inv
1	1	0	0	c	c	c	c	0	0	R	u	u	u	u	u	*u-read* SWAP	SWAP OVER alu-op
1	1	0	0	0	0	0	I	1	0	R	u	u	u	u	u	DUP *u-write*	inv
1	1	0	0	1	1	1	I	1	0	R	u	u	u	u	u	DUP *u-write*	DROP inv
1	1	0	0	c	c	c	c	1	0	R	u	u	u	u	u	*u-read* SWAP	alu-op

TABLE 1L. INSTRUCTION CODES-USER SPACE INSTRUCTIONS

INSTRUCTION CODE																OPERATION	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	(1ST CYCLE)	(2ND CYCLE)
1	0	1	0	0	0	0	i	0	0	R	0	s	s	s	s		inv shift
1	0	1	0	1	1	1	I	0	0	R	0	s	s	s	s	DROP DUP	Inv shift
1	0	1	0	c	c	c	c	0	0	R	0	s	s	s	s	OVER SWAP	alu-op shift
1	0	1	0	0	0	0	I	0	1	R	0	s	s	s	s	SWAP DROP	inv shift
1	0	1	0	1	1	1	i	0	1	R	0	s	s	s	s	DROP	inv shift
1	0	1	0	c	c	c	c	0	1	R	0	s	s	s	s		alu-op shift
1	0	1	0	0	0	0	i	1	0	R	0	s	s	s	s	SWAP DROP DUP	inv shift
1	0	1	0	1	1	1	i	1	0	R	0	s	s	s	s	SWAP	inv shift
1	0	1	0	c	c	c	c	1	0	R	0	s	s	s	s	SWAP OVER	alu-op shift
1	0	1	0	0	0	0	I	1	1	R	0	s	s	s	s	DUP	inv shift
1	0	1	0	1	1	1	i	1	1	R	0	s	s	s	s	OVER	inv shift
1	0	1	0	c	c	c	c	1	1	R	0	s	s	s	s	OVER OVER	alu-op shift

TABLE 1M. INSTRUCTION CODES-ALU FUNCTION INSTRUCTIONS

INSTRUCTION CODE																OPERATION
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	0	1	0	-	-	-	-	-	-	-	1	-	-	-	-	(See the Programmer's Reference Manual)

* These instructions perform multi-step math functions such as multiplication, division and square root functions. Use of either the Streamed Instruction mode or masking of interrupts is recommended to avoid erroneous results when performing Step Math operations. The following is a summary of these operations:

Unsigned Division:
- Load dividend into TOP and NEXT
- Load divisor into MD
- Execute single step form of D2* instruction 1 time
- Execute opcode A41A 1 time
- Execute opcode A45A 14 times
- Execute opcode A458 1 time
- The quotient is in NEXT, the remainder in TOP

Square Root Operations:
- Load value into TOP and NEXT
- Load 8000H into SR
- Load 0 into MD
- Execute single step form of D2* instruction 1 time
- Execute opcode A51A 1 time
- Execute opcode A55A 14 times
- Execute opcode A558 1 time
- The root is in NEXT, the remainder in TOP

TABLE 1N. INSTRUCTION CODES-STEP MATH* FUNCTIONS

cccc	*aaa*	FUNCTION
0010	001	AND
0011		NOR
0100	010	SWAP -
0101		SWAP - c With Borrow
0110	011	OR
0111		NAND
1000	100	+
1001		+c With Carry
1010	101	XOR
1011		XNOR
1100	110	-
1101		-c With Borrow

TABLE 1O. INSTRUCTION CODES-ALU LOGIC FUNCTIONS/OPCODES

SHIFT *ssss*	NAME	FUNCTION	STATUS OF C	TOP REGISTER			NEXT REGISTER		
				T15	Tn	T0	N15	Nn	N0
0000		No Shift	CY	Z15	Zn	Z0	TN15	TNn	TN0
0001	0<	Sign extend	CY	Z15	Z15	Z15	TN15	TNn	TN0
0010	2*	Arithmetic Left Shift	Z15	Z14	Zn-1	0	TN15	TNn	TN0
0011	2*c	Rotate Left	Z15	Z14	Zn-1	CY	TN15	TNn	TN0
0100	cU2/	Right Shift Out of Carry	0	CY	Zn+1	Z1	TN15	TNn	TN0
0101	c2/	Rotate Right Through Carry	Z0	CY	Zn+1	Z1	TN15	TNn	TN0
0110	U2/	Logical Right Shift	0	0	Zn+1	Z1	TN15	TNn	TN0
0111	2/	Arithmetic Right Shift	Z15	Z15	Zn+1	Z1	TN15	TNn	TN0
1000	N2*	Left Shift of NEXT	CY	Z15	Zn	Z0	TN14	TNn-1	0
1001	N2*c	Rotate NEXT Left	CY	Z15	Zn	Z0	TN14	TNn-1	CY
1010	D2*	32-bit Left Shift	Z15	Z14	Zn-1	TN15	TN14	TNn-1	0
1011	D2*c	32-bit Rotate Left	Z15	Z14	Zn-1	TN15	TN14	TNn-1	CY
1100	cUD2/	32-bit Right Shift Out of Carry	0	CY	Zn+1	Z1	Z0	TNn+1	TN1
‡ 1101	cD2/	32-bit Rotate Right Through Carry	TN0	CY	Zn+1	Z1	Z0	TNn+1	TN1
1110	UD2/	32-bit Logical Right Shift	0	0	Zn+1	Z1	Z0	TNn+1	TN1
1111	D2/	32-bit Right Shift	Z15	Z15	Zn+1	Z1	Z0	TNn+1	TN1

‡ See the Programmer's Reference Manual

Where: T15 -Most significant bit of TOP
Tn -Typical bit of TOP
T0 -Least significant bit of TOP
N15 -Most significant bit of NEXT
Nn -Typical bit of NEXT
N0 -Least significant bit of NEXT

C -Carry bit
CY -Carry bit before operation
Zn -ALU output
Z15 -Most significant bit 15 of ALU output
TNn -Original value of typical bit of NEXT

TABLE 1P. INSTRUCTION CODES-SHIFT FUNCTIONS

INSTRUCTION CODE																OPERATION
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	0	1	1	0	0	0	0	0	0	R	0	1	0	0	0	Forth 0 =
1	0	1	1	0	0	0	0	0	0	R	0	1	0	0	1	Double Shift Right Arithmetic
1	0	1	1	0	0	0	0	0	0	R	0	1	0	1	0	Double Shift Right Logical
1	0	1	1	0	0	0	0	0	0	R	0	1	1	0	0	Clear MAC Accumulator
1	0	1	1	0	0	0	0	0	0	R	0	1	1	1	0	Double Shift Left Logical
1	0	1	1	0	0	0	0	0	0	R	0	1	1	1	1	Floating Point Normalize
1	0	1	1	0	0	0	0	0	0	R	1	0	0	0	1	Shift MAC Output Regs Right
1	0	1	1	0	0	0	0	0	0	R	1	0	0	1	0	Streamed MAC Between Stack and Memory
1	0	1	1	0	0	0	0	1	0	R	1	0	0	1	0	Streamed MAC Between ASIC Bus and Memory
1	0	1	1	0	0	0	0	0	0	R	1	0	0	1	1	Mixed Mode Multiply
1	0	1	1	0	0	0	0	1	0	R	1	0	1	1	0	Unsigned Multiply
1	0	1	1	0	0	0	0	1	0	R	1	0	1	1	1	Signed Multiply
1	0	1	1	0	0	0	0	0	0	R	1	0	1	0	0	Signed Mpy and Subtract from Accumulator
1	0	1	1	0	0	0	0	0	0	R	1	0	1	0	1	Mixed Mode Multiply Accumulate
1	0	1	1	0	0	0	0	0	0	R	1	0	1	1	0	Unsigned Multiply Accumulate
1	0	1	1	0	0	0	0	0	0	R	1	0	1	1	1	Signed Multiply Accumulate
1	0	1	1	1	1	1	0	0	0	R	1	0	0	1	0	Load MXR Register
1	0	1	1	1	1	1	0	0	0	R	1	0	1	1	0	Load MLR Register
1	0	1	1	1	1	1	0	0	0	R	1	0	1	1	1	Load MHR Register
1	0	1	1	1	1	1	0	1	0	R	1	0	0	1	0	Store MXR Register
1	0	1	1	1	1	1	0	1	0	R	1	0	1	1	0	Store MLR Register
1	0	1	1	1	1	1	0	1	0	R	1	0	1	1	1	Store MHR Register

TABLE 1Q. INSTRUCTION CODES-MAC/BARREL SHIFTER/LZD INSTRUCTIONS

TABLE 2A. ELECTRICAL PERFORMANCE CHARACTERISTICS

Parameter	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{CC} = 4.5 V and 5.5 V, Unless otherwise specified		Group A Sub-groups	Limits		Unit
					Min	Max	
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5 V		1, 2, 3	V_{CC}x0.7	- - -	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5 V		1, 2, 3	- - -	0.8	V
High Output Voltage	V_{OH1}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA		1, 2, 3	3.5	- - -	V
	VOH2	V_{CC} = 4.5 V, I_{OH} = -100 µA			V_{CC}-0.4	- - -	
Low Output Voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 4.0 mA		1, 2, 3	- - -	0.4	V
Input Leakage Current	I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND	TC = +25°C TC = -55°C	1, 2, 3	-1	1	µA
			TC = +125°C		-5	5	µA
I/O Leakage Current	I_{IO}	V_{CC} = 5.5 V, V_O = V_{CC} or GND		1, 2, 3	-10	10	µA
Standby Power Supply Current	I_{CCSB}	V_I = V_{CC} or GND, 1/	TC = +25°C TC = -55°C	1, 2, 3	- - -	500	µA
		10/	TC = +125°C			2.5	mA
Operating Power Supply Current	I_{CCOP}	V_I = V_{CC} or GND, f_{CLK} = 1 MHz, Outputs Unloaded (I_O = 0 mA), 2/		1, 2, 3	- - -	35	mA
Input Capacitance	C_I	V_{CC} = Open, f = 1 MHz, T_C = +25°C		3/	10 TYPICAL		pF
I/O Capacitance	$C_{I/O}$	V_{CC} = Open, f = 1 MHz, T_C = +25°C		3/	10 TYPICAL		pF
Functional Test	F_T	See 4.3.1 herein.		7,8A,8B	- - -	- - -	V

See footnotes at end of table.

TABLE 2A. ELECTRICAL PERFORMANCE CHARACTERISTICS (continued)

Parameter	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{CC} = 4.5 V and 5.5 V, V_{IH} = 4.0 V, V_{IL} = 0.4 V, C_L = 50 pF, Unless otherwise specified	Group A Sub-groups	Limits		Unit
				Min	Max	
CLOCK, WAIT, and TIMER TIMING - REQUIREMENTS						
ICLK Period	t_1		9, 10, 11	62	---	ns
ICLK High Time	t_2		9, 10, 11	24	---	ns
ICLK Low Time	t_3		9, 10, 11	24	---	ns
WAIT Setup Time	t_4		9, 10, 11	5	---	ns
WAIT Hold Time	t_5		9, 10, 11	5	---	ns
EI High to EI High	t_6	External Clock/Timer Input	9, 10, 11	t_1=4	---	ns
EI High Time	t_7		9, 10, 11	20	---	ns
EI Low Time	t_8		9, 10, 11	15	---	ns
CLOCK, WAIT, and TIMER TIMING - RESPONSES						
ICLK to TCLK High	t_{11}		9, 10, 11	5	35	ns
TCLK Low Time	t_{12}	6/	9, 10, 11	55	---	ns
TCLK High Time	t_{13}		9, 10, 11	55	---	ns
ICLK to PCLK High	t_{15}		9, 10, 11	5	35	ns
PCLK Low Time	t_{16}	6/, 5/	9, 10, 11	55	---	ns
PCLK High Time	t_{17}		9, 10, 11	55	---	ns
ICLK to TCLK Low	t_{19}		9, 10, 11	---	36	ns
ICLK to PCLK Low	t_{20}		9, 10, 11	---	35	ns
MEMORY BUS TIMING - REQUIREMENTS						
MD Setup Time	t_{21}	Read Cycle	9, 10, 11	25	---	ns
MD Hold Time	t_{22}		9, 10, 11	4	---	ns
MEMORY BUS TIMING - RESPONSES						
PCLK to MA Valid	t_{24}	6/	9, 10, 11	---	62	ns
MA Hold Time	t_{25}	6/	9, 10, 11	20	---	ns

See footnotes at end of text.

TABLE 2A. ELECTRICAL PERFORMANCE CHARACTERISTICS (continued)

Parameter	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{CC} = 4.5 V and 5.5 V, V_{IH} = 4.0 V, V_{IL} = 0.4 V, C_L = 50 pF, Unless otherwise specified	Group A Sub-groups	Limits		Unit
				Min	Max	
PCLK to MR/$\overline{W}$, UDS, LDS, NEW, and BOOT Valid	t_{29}	6/	9, 10, 11	- - -	50	ns
MR/$\overline{W}$, UDS, LDS, NEW and BOOT Hold Time	t_{31}	6/	9, 10, 11	20	- - -	ns
PCLK to MD Valid	t_{32}	Write Cycle	9, 10, 11	- - -	20	ns
MD Hold Time	t_{33}	Write Cycle, 6/	9, 10, 11	20	- - -	ns
MD Enable Time	t_{34}	Write Cycle	8/	-3	- - -	ns
PCLK to MD Disable Time	t_{35}	Write Cycle, 6/	8/	- - -	60	ns
ASIC BUS and INTERRUPT TIMING - REQUIREMENTS						
GD Read Setup to PCLK	t_{40A}	Read Cycle (not Streamed)	9, 10, 11	55	- - -	ns
	t_{40B}	Streamed Mode	9, 10, 11	28	- - -	ns
GD Read Setup to $\overline{GIO}$	t_{41A}	Read Cycle (not Streamed)	9, 10, 11	60	- - -	ns
	t_{41B}	Streamed Mode	9, 10, 11	33	- - -	ns
GD Read Hold from $\overline{GIO}$	t_{42}	Read Cycle	9, 10, 11	0	- - -	ns
GD Read Hold from PCLK	t_{43}		9, 10, 11	0	- - -	ns
EI/NMI Setup Time	t_{44}	INT/NMI Cycle	9, 10, 11	40	- - -	ns
INTSUP Setup Time	t_{46}		9, 10, 11	22	- - -	ns
INTSUP Hold Time	t_{47}		9, 10, 11	0	- - -	ns
ASIC BUS and INTERRUPT TIMING - RESPONSES						
PCLK High to $\overline{GIO}$ Low	t_{48}	4/	9, 10, 11	52	- - -	ns
$\overline{GIO}$ Low Time	t_{49}	4/, 9/	9, 10, 11	52	- - -	ns

See footnotes at end of table.

TABLE 2A. ELECTRICAL PERFORMANCE CHARACTERISTICS (continued)

Parameter	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{CC} = 4.5 V and 5.5 V, V_{IH} = 4.0 V, V_{IL} = 0.4 V, C_L = 50 pF, Unless otherwise specified	Group A Sub-groups	Limits		Unit
				Min	Max	
ICLK High to $\overline{GIO}$ Low	t_{50}		9, 10, 11	- - -	43	ns
ICLK High to $\overline{GIO}$ High	t_{51}		9, 10, 11	- - -	40	ns
PCLK to GA Valid	t_{52}	6/	9, 10, 11	- - -	49	ns
$\overline{GIO}$ to GA Hold Time	t_{54}	6/	9, 10, 11	12	- - -	ns
PCLK to GR/$\overline{W}$ Valid	t_{56}	6/	9, 10, 11	- - -	50	ns
$\overline{GIO}$ to GR/$\overline{W}$ Hold Time	t_{58}	6/	9, 10, 11	15	- - -	ns
GD Enable Time	t_{61}	Write Cycle	8/	-7	- - -	ns
GD Valid Time	t_{62}		9, 10, 11	- - -	16	ns
$\overline{GIO}$ to GD Hold Time	t_{63}	Write Cycle, 6/	9, 10, 11	12	- - -	ns
$\overline{GIO}$ to GD Disable Time	t_{65}	Write Cycle, 6/	8/	- - -	60	ns
PCLK to INTA High Time	t_{67}	INTA Cycle	9, 10, 11	- - -	25	ns
INTA Hold Time	t_{68}		9, 10, 11	0	- - -	ns
$\overline{GIO}$ High Time	t_{69}	4/, 9/	9, 10, 11	52	- - -	ns

1/ Typical I_{CCSB}: 10μA. The RTX 2010RH is a static SOS CMOS part. Therefore $I_{CCSB} > 0$ is due to leakage currents.

2/ Operating supply current is proportional to frequency.

3/ All measurements referenced to device GND. The values provided represent typical measurements only. This parameter is neither characterized, tested, sampled, or guaranteed.

4/ Tested with $t_1 = t_{1(min)}$. For $t_1 > t_{1(min)}$, add $t_1 - t_{1(min)}$ to this parameter.

5/ If CYCEXT and/or ARCE bit is set, add 1 x $t_{1(min)}$ to this parameter for USER memory access (CYCEXT case), or external ASIC Bus read (ARCE case).

6/ Tested with t_1 at specified minimum and $t_2 = 0.5 \times t_1$. For $t_2 > 0.5 \times t_{1(min)}$, add $t_2 - (0.5 \times t_{1(min)})$ to this parameter.

8/ Output enable and disable times are characterized and guaranteed, but not 100% tested or sampled.

9/ If ARCE bit is set, add 1 x $t_{1(min)}$ to this parameter for external ASIC Bus Read Cycles.

10/ Measurement is made with the RAM sense AMPs disabled.

TABLE 2B. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 test requirements		Subgroups (per method 5005, table I)
Initial electrical parameters		1, 7, 9
Interim and Post Burn-in electrical parameters		1*, 7*, 9, (Deltas)*
Final electrical parameters **		2, 3, 8A, 8B, 10, 11
Group A electrical parameters		1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B electrical parameters	B5	1, 2, 3, 7, 8A, 8B, 9, 10, 11
	Others	1, 7
Group D electrical parameters		1, 7
Group E2 electrical parameters		1, 7, 9

Notes:

* PDA applies to subgroups 1, 7 and deltas (see TABLE 5 herein).

** Per MIL-STD-883, Method 5004, paragraph 3.5.2, tests conducted during Post Burn-in electrical measurements (i.e., subgroups 1, 7 and 9) need **not** be repeated during Final electrical measurements.

TABLE 3. GROUP B INSPECTION SMALL LOT SAMPLING PLAN 1/

TEST	MIL-STD-883 METHOD	CONDITION	LOT SIZE/QUANTITY (ACC NO) OR LTPD 0-50	51-100	101-200	>200 9/
Subgroup 1						
a. Physical Dimension 2/	2016		1(0)	1(0)	2(0)	2(0)
b. Internal Water-vapor Content 3/	1018	5,000 ppm maximum water content at 100°C	1(0)	1(0)	2(0)	3(0)
Subgroup 2						
a. Resistance to Solvents	2015		2(0) 4/	2(0) 4/	4(0)	4(0)
b. Internal Visual and Mechanical	2013, 2014		1(0)	1(0)	1(0)	2(0)
c. Bond Strength # Devices # Bond Pulls	2011	Test Condition C & D	1 5/	1 5/	1 5/	3 LTPD=10
d. Die Shear	2027	see 4.2a(3) herein.	1(0)	1(0)	1(0)	3(0)
Subgroup 3						
a. Solderability # Devices # Bond Pulls	2003 or 2022		1 5/	2 5/	3 LTPD=10	3 LTPD=10
Subgroup 4						
a. Lead Integrity	2004	Test condition B2	1(0) 6/	2(0) 6/	2(0) 6/	3 LTPD = 5 10/
b. Seal 1. Fine 2. Gross	1014					
c. Lid Torque						
Subgroup 5			8(0)	15(0)	20(0)	77(1)
a. End-Point Elect. Parameters		See TABLE 2B herein.				
b. Steady State Life	1005	See Figure 6B herein.				
c. End-Point Elect. Parameters		See TABLE 2B herein.				
Subgroup 6			3(0)	3(0)	5(0)	25(1)
a. End-Point Elect. Parameters		See TABLE 2B herein.				
b. Temp Cycling	1010	Cond. C, 100 cycles				

TABLE 3. GROUP B INSPECTION SMALL LOT SAMPLING PLAN (CONT.) 1/

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LOT SIZE/QUANTITY (ACC NO) OR LTPD 0-50	51-100	101-200	>200 2/
c. Constant Acceler.	2001	Cond. D, Y1 orient				
d. Seal 1. Fine 2. Gross	1014					
e. End-Point Elect. Parameters		See TABLE 2B herein.				
Subgroup 7 a. End-Point Elect. Parameters		Group A and delta limits in accordance with method 3015	8/	8/	8/	15(0) 8/
b. Electrostatic Discharge	3015					
c. End-Point Elect. Parameters		Group A and delta limits in accordance with method 3015				
TOTAL # OF GOOD DEVICES REQUIRED:			12 (a) 11 (b)	19 (a) 18 (b)	27 (a) 25 (b)	102(a) 99 (b)

NOTES: (a) = Frit seal (b) = Other seal

1/ The notes of table IIa, MIL-STD-883, method 5005 shall apply in addition to the notes specified herein. This table is used for reference to sampling plan only. The actual tests and sub groups required to be inspected shall be in accordance with the latest revision of table IIa, MIL-STD-883, method 5005.

2/ Units may be selected at any time after device sealing operation and in the final lead finish. Rejects may be used for these subgroup tests.

3/ Units may be selected at any time after burn-in and need not be branded.

4/ Resistance to solvent testing shall consist of subjecting 1 unit to solvent C and 1 unit to solvent D only.

5/ All wires or leads (as applicable) shall be tested for packages with lead counts ≤ 22. For packages with lead counts ≥ 23, the number of wires or leads shall be based upon an LTPD of 10.

6/ 3 leads per device shall be sampled.

TABLE 3. GROUP B INSPECTION SMALL LOT SAMPLING PLAN (CONT.)
1/

7/ Subgroup B-6 is nondestructive based on Harris test results of this subgroup per MIL-M-38510. However, this subgroup is considered to be destructive by Goddard Space Flight Center (GSFC) Parts Branch. Any devices used for this subgroup shall not be used as deliverable against the flight quantities (see paragraph 4.6.2 herein).

8/ Subgroup 7 is performed for initial qualification and product redesign as a minimum. Sample size will be 3(0) with repeat for cumulative effects 15(0). Per MIL-STD-883, Revision D, Subgroup 7 has been deleted for Table IIa. The requirements for ESD shall be as specified in MIL-M-38510.

9/ The > 200 column sample sizes are based on those currently specified in method 5005.

10/ LTPD = 5 based on the number of leads, 3 devices minimum.

TABLE 4. GROUP D INSPECTION SMALL LOT SAMPLING PLAN 1/

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LOT SIZE/QUANTITY (ACC NO) OR LTPD 0-50	51-100	101-200	>200 3/
Subgroup 1						
a. Physical Dimension 2/	2016		3(0)	3(0)	5(0)	15(0)
Subgroup 2						
a. Lead Integrity 5/	2004					
# Devices			1	2	3	3
# Leads			5(0)	10(0)	15(0)	LTPD = 5
b. Seal	1014		1(0)	2(0)	3(0)	15(0)
1. Fine						
2. Gross						
Subgroup 3 4/			3(0)	3(0)	5(0)	25(1)
a. Thermal Shock	1011	Per applicable				
b. Temperature Cycling	1010					
c. Moisture Resistance	1004					
d. Visual Examination	1004, 1010					
e. Seal	1014					
1. Fine						
2. Gross						
f. End-Point Elect. Parameters		See TABLE 2B herein.				
Subgroup 4			3(0)	3(0)	5(0)	25(1)
a. Mechanical Shock	2002					
b. Vibration, Variable Frequency	2007					
c. Constant Acceleration	2001					
d. Seal	1014					
1. Fine						
2. Gross						
e. Visual Examination	1010 or 1011					
f. End-Point Elect. Parameters		See TABLE 2B herein.				

TABLE 4. GROUP D INSPECTION SMALL LOT SAMPLING PLAN (CONT.) 1/

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LOT SIZE/QUANTITY (ACC NO) OR LTPD 0-50	51-100	101-200	>200 2/
Subgroup 5			3(0)	3(0)	5(0)	15(0)
a. Salt Atmosphere	1009					
b. Seal	1014					
1. Fine						
2. Gross						
c. Visual Examination	1009	Visual criteria only				
Subgroup 6						
a. Internal Water-vapor Content	1018	5,000 ppm maximum water content at 100°C	1(0) or 3(0)	1(0) or 3(0)	2(0) or 4(1)	3(0) or 5(1)
Subgroup 7						
a. Adhesion of Lead Finish	2025					
# Devices			1	2	3	3
# Leads			5(0)	10(0)	15(0)	15(0)
Subgroup 8						
a. Lid Torque	2024		1(0)	2(0)	3(0)	5(0)
TOTAL # OF GOOD DEVICES REQUIRED:			9	9	14	55

NOTES:

1/ The notes of table IV, MIL-STD-883, method 5005 shall apply in addition to the notes specified herein. This table is used for reference to sampling plan only. The actual tests and sub groups required to be inspected shall be in accordance with the latest revision of table IV, MIL-STD-883, method 5005.

2/ Units may be selected at any time after device sealing operation and in the final lead finish. Rejects may be used for these subgroup tests.

3/ The > 200 column sample sizes are based on those currently specified in method 5005.

4/ Since the package has gold-plated lids, the inspection criteria for illegiable marking of paragraph 3.3, Method 1010, and paragraph 3.8a, Method 1004, of MIL-STD-883, shall not apply. Marking is not jeopardized, however, because the same package types meet the resistance to solvents requirements of Group B, Subgroup 2, Method 2015, of MIL-STD-883.

5/ LTPD = 5 based on the number of leads, 3 devices minimum.

TABLE 5. POST BURN-IN DELTAS

DELTA CALCULATION	INITIAL READING	FINAL READING
I (POST STATIC B-I)	INITIAL ELECTRICAL TEST	INTERIM ELECTRICAL TEST
II (POST DYNAMIC B-I)	INITIAL ELECTRICAL TEST	INTERIM ELECTRICAL TEST

Delta Read and Record Points

PARAMETER	ABSOLUTE LIMIT	Final reading
ICCSB	500µA	±150µA
VOL	400MV	±60MV
VOH1	3.5V	±550MV
IIO	10µA	±2µA