MAPLD 2008 - Annapolis, Maryland

September 15–18, 2008

Sponsored by NASA Electronic Parts and Packaging (NEPP) Program

Conference Program

Initiated in 1998, the Military/Aerospace Programmable Logic Device (MAPLD) conference addresses the unique issues surrounding the use of PLDs for military/aerospace applications that must operate with a high degree of reliability, often in harsh environments. For more information on MAPLD 2008, please visit http://nepp.nasa.gov/mapld_2008/.

Seminars

"Design for Radiation Effects" - Melanie Berg, Muniz Engineering Inc. (MEI)

"FPGA Design Review Preparation" - Brian Smith, Stargazer Systems

"Accelerating FPGA Designs and Design Work: Implementing Faster Designs Faster" - Heather Quinn, Los Alamos National Laboratory; Mike Wirthlin, Brigham Young University; Tim Gallagher, Lockheed Martin Corporation; Miriam Leeser, Northeastern University; Ray Andraka, Andraka Consulting Group, Inc.; George Harper, Bluespec, Inc.; Bryan Penner, Xilinx

Program Sessions

Session A - "PLD Applications"
Co-Chair: John Harkins, Department of Defense
Co-Chair: Damon Bradley, NASA Goddard Space Flight Center

Session B - "PLDs and Supporting Devices"
Co-Chair: Joe Fabula, Xilinx Corporation
Co-Chair: Sana Rezgui, Actel Corporation

Session C - "Radiation Effects and Mitigation in PLDs"
Co-Chair: Mike Wirthlin, Brigham Young University
Co-Chair: Heather Quinn, Los Alamos National Laboratory

Session D - "Design and Verification Tools and Methodologies"
Co-Chair: Tim Gallagher, Lockheed Martin Corporation
Co-Chair: Craig Kief, FPGA Mission Assurance Center

Session E - "PLD-Based System Architectures"
Co-Chair: John Demello, Air Force Research Laboratory
Co-Chair: Mythi To, Sandia National Laboratories
Co-Chair: Phyllis Hestnes, NASA Goddard Space Flight Center

Poster Session
Chair: David Meshel, The Aerospace Corporation

Additional Information

For additional information regarding the conference, please visit the MAPLD 2008 website (http://nepp.nasa.gov/mapld_2008). If you have questions regarding the conference, please feel free to contact:

Wesley Powell	Wesley.A.Powell@nasa.gov	Conference Chair
Ken LaBel	Kenneth.A.Label@nasa.gov	Conference Co-Chair
Mike Sampson	Michael.J.Sampson@nasa.gov	Conference Co-Chair

Monday (9/15/08)

Seminars	
7:30 - 8:00	Registration & Continental Breakfast
8:00-10:00	"Design for Radiation Effects" As core voltages and transistor geometries decrease, FPGA sensitivity to Single Event Upsets (SEUs) while operating in harsh radiation environments has increased. It has become imperative to bridge the gap between the radiation effects research community and the FPGA design application community. In many cases, key considerations pertaining to ionization and fault tolerance are only being addressed during design reviews or not at all. Consequently, it can be too late or extremely expensive to resolve subsequent critical design limitations and issues. The presentation will give a unique perspective of current radiation affects to state of the art design strategy and implementation. The goal is to (1) bridge the gap between radiation effects and design communities, (2) answer common designers' questions so that flight-project design cycle time and system cost can be effectively reduced and (3) help prevent the creation of impracticable systems due to the incorrect implementation of COTS insertion within space flight projects. Melanie Berg, Muniz Engineering Inc. (MEI)
10:00-12:00	"FPGA Design Review Preparation" We all know that the most enjoyable part of space electronics design is the design review. Well, for me anyway! We'll discuss the preparation process; focusing on a structured approach, beginning when the FPGA is just a gleam in the designers eye, and ending with a completed design review package. Audience participation will be expected, since we are all experts here ... or at least have opinions! Brian Smith, Stargazer Systems
12:00-1:00	Lunch
1:00-5:00	"Accelerating FPGA Designs and Design Work: Implementing Faster Designs Faster" Designing fast FPGA user circuits is often a time-consuming process that involves determining the optimal bit width, modeling the algorithm, and finding the best possible implementation for the architecture. Often times this design work is at odds with a project's deadlines and causes designers to balance the need for the fastest design implementation possible with the need to finish the design work as fast as possible. One aspect that hinders quick algorithm prototyping and design work is the hardware description languages used to describe hardware circuits, such as VHDL and Verilog. In this seminar we will explore both topics of faster FPGA designs and faster FPGA design work so that designers will have a better idea of the options available to them. Heather Quinn, Los Alamos National Laboratory Mike Wirthlin, Brigham Young University Tim Gallagher, Lockheed Martin Corporation Miriam Leeser, Northeastern University Ray Andraka, Andraka Consulting Group, Inc. George Harper, Bluespec, Inc. Bryan Penner, Xilinx

Seminar Presenters

Melanie Berg - Melanie Berg received her MS degree in Electrical Engineering from the University of Pittsburgh in 1990. She began writing VHDL in 1988 for Digital Systems creating logic modules as part of a small design group. Ms. Berg started her formal career with IBM in 1990 as a member of the ASIC Advance Logic Design Team in Poughkeepsie NY. Over the past 18 years, she has been part of several development teams responsible for high speed multi-million gate ASIC and complex FPGA implementations. Ms. Berg is currently a member of IEEE and has joined the Radiation Effects and Analysis group at NASA Goddard Space Flight Center. She has published and presented several papers concerning such topics as Reliable Synchronous Design Methodology, Mitigation Strategies for Critical Circuitry, and Hardness Assurance for Space Flight Projects. Ms. Berg is presently investigating radiation effects and applicable mitigation strategies for the potential insertion of Field Programmable Gate Arrays (FPGAs) and ASICS into critical space flight projects.

Brian Smith - Brian Smith is the President and Chief Engineer of Stargazer Systems Inc. His over 20 years experience has been gained through employment at defense contractors, as a civil servant designing successful spacecraft electronics for NASA, and as a chip designer in a high technology startup. Mr. Smith's experience ranges from board-level design, through digital system-level design, to FPGA and ASIC implementations. Mr. Smith has participated in over 50 FPGA design reviews in the past few years, and has helped NASA Goddard develop a design, analysis, and review strategy. He is also serving as Consultant to the NASA Engineering and Safety Center (NESC) Avionics Fellow for FPGA-related matters.

Heather Quinn - Heather Quinn has been at Los Alamos National Laboratory since 2004 as first a post-doctoral research associate and then a technical staff member. She received a BS in Mathematics and Physics from Knox College in 1992, a MS in Electrical Engineering in 2000, and a PhD in Electrical Engineering in 2004. Her specialty is Computer Engineering.

Mike Wirthlin - Mike Wirthlin is currently an Associate Professor in the Department of Electrical and Computer Engineering at Brigham Young University (BYU). He has been actively involved in FPGA design for over 16 years and is active in the FPGA design, architecture, and tool research communities. His research interests include Configurable Computing Systems, FPGA reliability, fault tolerant computing, high-level synthesis, and computer-aided design for application-specific computing.

Tim Gallagher - Tim Gallagher is currently a researcher on space-based reconfigurable technologies at Lockheed Martin Space System Company in Denver. His main focus is on joint High-Order Languages (HOL/ESL) and RTL design methodologies to increase designer productivity and tool usability. He is involved with outreach to experts in FPGA and HPEC (high-performance embedded computing) technologies such as CHREC (Center for High Performance Reconfigurable Computing) and associated universities. Tim received his Bachelors in Engineering at University of Maryland College Park and his Masters in Engineering at University of Colorado Boulder.

Miriam Leeser - Miriam Leeser is currently a full professor in the Electrical and Computer Engineering department of Northeastern University. Her specialty is Computer Engineering. She received a BS in Electrical Engineering from Cornell University, and Diploma and PhD degrees in Computer Science from Cambridge University in England. She joined the faculty of Cornell University's Department of Electrical Engineering in 1988. She received a National Science Foundation Young Investigator Award in 1992. Her research interests are in the areas of design and design tools for field programmable logic, and high level design tools for digital systems.

Ray Andraka - Raymond J. Andraka, P.E. is the president of the Andraka Consulting Group, Inc., a digital hardware design firm he founded in 1994. His company is focused exclusively on high performance DSP designs using FPGAs. He has applied FPGAs to signal processing applications including radar processors, radar environment simulators, sonar, HDTV, digital radio, spectrum analyzers, image processing, medical imaging, and communications test equipment. His accomplishments include development of the fastest FFTs available for FPGAs, as well as several firsts in FPGA based signal processing. Ray's prior signal processor design experience includes 5 years with Raytheon Missile Systems designing radar signal processors, and 3 years of signal detection and reconstruction algorithm development for the US Air Force. He also spent

2 years developing image readers and processors for G-Tech, where he set the company time-to-market record for a new product. He has also authored many conference papers dealing with high performance FPGA design and signal processing applications, and is a regular contributor to the comp.arch.fpga, comp.lang.vhdl and comp.dsp newsgroups. Ray earned his BSEE from Lehigh University in Jan 1984 and his MSEE from the University of Massachusetts in June 1992.

George Harper - Mr. Harper has more than 20 years of marketing and engineering experience from the semiconductor, communications, and storage industries. He has overall responsibility for Bluespec's product planning and marketing initiatives. Previously, Mr. Harper was director of marketing at Trebia Networks, where he managed the product planning and marketing initiatives for a storage network processor family. Prior to that, he held senior marketing positions at Conexant Systems (formerly Maker Communications) and Shiva Corporation, and engineering positions at LSI Logic, in both California and Massachusetts, specifically in the areas of chip design and microprocessor sales. Harper has a B.S. and an M.S. in electrical engineering from Stanford University and an M.B.A. from Harvard University.

Bryan Penner - Bryan Penner has been at Xilinx since 2001 and for the last five years has been working as a Field Applications Engineer. Before Xilinx, he was at Storage Technology for three years. He has received a BS in Electrical Engineering from Purdue University in 1998 and a MS in Electrical Engineering from the University of Colorado in 2003.

Tuesday (9/16/08)

7:30 - 8:00	Registration & Continental Breakfast	
8:00-8:20	Conference Welcome – Mr. Arthur F. Obenschain, Deputy Director, NASA Goddard Space Flight Center	
8:20- 8:40	Session A	"Performance Study of Matrix Operations on Homogeneous and Heterogeneous Reconfigurable Computing Systems" - Melissa C. Smith, Clemson University
8:40- 9:00		"A 600-Mb/s (8158,7136) Low-Density Parity-Check Decoder Utilizing a Vertex 4 LX200 FPGA" - Sterling Whitaker, University of Idaho
9:00- 9:20		"Lunar Applications for Reconfigurable Processing" - Kevin Somervill, NASA Langley Research Center
9:20- 9:40		"Achieving High Performance Computing and Application Flexibility within the Spacecraft Payload" - Ian Troxel, SEAKR Engineering
9:40- 10:00		"Implementing Image Registration Algorithms on Reconfigurable Computer" - Miaoqing Huang, The George Washington University
10:00-10:50	Break - Industrial Exhibits	
10:50-11:10	Special Topic	"SpaceWiki : Bridging the Research-Application Gap and Enabling a Living Collaborative Environment" - John Demello, United States Air Force
11:10-11:30	Session A	"Secure Software Defined Radio in Space" - Ian Land, John Corbett, Xilinx Corporation
11:30-11:50		"GPS Receiver for LEO, GEO and Beyond" - Steve Sirotzky, NASA Goddard Space Flight Center
11:50-12:10		"SpaceCube: A Reconfigurable Processing Platform For Space" - John Godfrey, NASA Goddard Space Flight Center
12:10-1:10	Lunch - "FPGAs and the Quest for New Relevance of America's Space Program" – Dr. Steven Suddarth, FPGA Mission Assurance Center (FMAC)	
1:10-1:30	Session A	"Turbo-coding: Merits of implementation in Actel RTAX FPGA" - Charlie Howard, Southwest Research Institute
1:30-1:50		"SmartCell Reconfigurable Architecture for Low-Power Stream Processing" – Xinming Huang, Worcester Polytechnic Institute
1:50-2:10		"Assessment of Proper Bonding Methods and Mechanical Characterization FPGA CQFP Components" - Milton Davis, NASA Goddard Space Flight Center
2:10-2:30	Session B	"Single Event Effects of Accelerated Terrestrial Cosmic Rays on Ferroelectric RAM" - Lindsay O'Brien Quarrie, New Mexico Tech METTOP
2:30-2:50		"NESC Actel RTAX-S FPGA Risk Reduction Life Testing" - Brian Smith, Stargazer Systems
2:50-3:10		"ATF280E Rad-Hard SRAM Based FPGA" - Bernard Bancelin, Atmel Nantes SAS
3:10-3:40	Break - Industrial Exhibits	
3:40-4:00	Session B	"RTA3P Qualification Plan" - Marco Cheung, Solomon Wolday, Actel Corporation
4:00-4:20		"Converting PLD-based SoC into RadSafe™ ASIC" - Ran Ginosar, Ramon Chips, Ltd.
4:20-4:40		"A Comprehensive Skew Analysis of Routed Clocks in Actel's SX32-A" – Parag Shekher, Actel Corporation
4:40-5:00		"Reconfigurable, High Density, High Speed, Low Power, Radiation" - Shankarnarayanan Ramaswamy, BAE Systems

Wednesday (9/17/08)

7:30 - 8:00	Registration & Continental Breakfast	
8:00-8:20	Session B	"Radiation Hardened FPGA Technology for Space Applications" - Dinu Patel, BAE Systems Inc.
8:20-8:40		"Current Status of the SIRF Program" - Joseph Fabula, Xilinx Corporation
8:40-9:00		"ASIC Building Blocks for Space" - Uwe Hoch, Richard Wiest, Astrium GmbH
9:00-9:20	Session C	"Results from the Cibola Flight Experiment's 1st Year On-Orbit" - Michael Caffrey, Los Alamos National Laboratory
9:20-9:40		"Reliability Concerns with Logical Constants in Xilinx FPGA Designs" - Heather Quinn, Los Alamos National Laboratory
9:40-10:00		"A Few Guidelines for the SET Characterization of Non-Volatile FPGAs: Lessons Learned" - Sana Rezgui, Actel Corporation
10:00-10:40	Break - Industrial Exhibits	
10:40-11:00	Session C	"Characterizing the Vulnerability of an Onboard Computation to Silent Data Corruption" - Kenneth Zick, University of Michigan
11:00-11:20		"Hardening-by-design techniques using residue number system in SRAM-based FPGAs: an experiment on a FIR filter" - Andrea Manuzzato, Università di Padova
11:20-11:40		"Practical Analysis of SEU-induced Errors in an FPGA-based Digital Communications System" - Brian Pratt, Brigham Young University
11:40-12:00		"A High-Level Tool for Bit-level SEU Sensitivity Analysis in DSP Filters" - Srinivas Katkoori, University of South Florida
12:00-1:00	Lunch - "Meeting Technology Needs through Innovative Partnerships at NASA" – Doug Comstock, NASA Innovative Partnership Program (IPP) Office	
1:00-1:20	Session C	"The TID Performance of Deep Submicron CMOS Processes" - Joseph Fabula, Xilinx Corporation
1:20-1:40		"FPGA System Error Rate Analysis for Harsh Radiation Environments" - Keith Morgan, Los Alamos National Laboratory
1:40-2:00		"TID Characterization Results of Actel ProASIC3, ProASIC3E, and IGLOO Flash-based Field Programmable Gate Arrays" - Gregory Allen, Jet Propulsion Laboratory/California Institute of Technology
2:00-2:20		"On the Enlargement of Single Event Transients' Width in Flash-based FPGAs" - Simone Gerardin, Universita` di Padova
2:20-2:50	Break	
2:50-4:00	Invited Speaker - Dr. Harley Thronson, NASA Headquarters "Past, Present, and Future of In-Space Servicing of Major Scientific Spacecraft"	
4:00-4:20	Session D	"ESL for Image Processing" - Saul Weiss, Lockheed Martin Corporation
4:20-4:40		"A System Architecture for Aerospace Applications Employing Partial Reconfiguration and High-Level Simulation" - Ross Hymel, Daniel McMurtrey, Sandia National Laboratories
4:40-5:00		"Accelerated FPGA Verification" - Gary Burke, Jet Propulsion Laboratory

Thursday (9/18/08)

7:30 - 8:00	Registration & Continental Breakfast	
8:00-8:20	Session D	"The Use of Fault Injection to Simulate Upsets in Reconfigurable FPGAs" - Gary Swift, Xilinx Corporation
8:20-8:40		"Mitigation, Design Flow and Troubleshooting a soft processor in a complex FPGA" - Greg Miller, Xilinx Corporation
8:40-9:00		"Low power algorithm implementation and verification using C++" - Dan Gardner, Mentor Graphics Corporation
9:00-9:20		"Application Acceleration within a High-level Language Reconfigurable Computing Framework" - Melissa C. Smith, Clemson University
9:20-9:40		"DO-254 Compliance: Pitfalls, Challenges and Solutions" - Michelle Lange, Mentor Graphics Corporation
9:40-10:00		"Structured Assertion Design Verification for Complex Safety-Critical Hardware" - Kristoffer Karlsson, Håkan Forsberg
10:00-10:20	Break	
10:20-10:50	Special Topic	"Reliability Guidelines for DC/DC Converters" - Jack Shue, NASA Goddard Space Flight Center
10:50-11:10	Session E	"LEON3FT Processor with PCI, Ethernet and Reed-Solomon SDRAM protection" – Per Danielsson, Gaisler Research
11:10-11:30		"Reliability Prediction of a Fault Tolerant COTS Parallel Computing Payload" - Sharon Lim Siok Lin, Nanyang Technological University
11:30-11:50		"Fault Tolerant FPGA Reconfigurable Hardware Architecture" - Robert L. Shuler, NASA Johnson Space Center
11:50-12:10		"A breadboard for real time image processing on board Gaia" - Shan Mignot, Observatoire de Paris
12:10-1:10	Lunch - "Reformation, Formulation, and the Future of Reconfigurable Computing" – Dr. Alan George, University of Florida, NSF Center for High Performance Reconfigurable Computing (CHREC)	
1:10-1:30	Session E	"Unifying Spacecraft Payload Interconnects Using the Reprogrammable Space Network Interface Controller" - Ian Troxel, SEAKR Engineering
1:30-1:50		"A Reconfigurable Multi-Core Architecture to Support SPMD Applications" - John K. Antonio, University of Oklahoma
1:50-2:10		"Bitstream Compression using Partial Reconfiguration" - Benjamin Sellers, Brigham Young University
2:10-3:40	Poster Session	
3:40-4:00	Session E	"Single Event Upset Xilinx-Sandia Experiment (SEUXSE) on the International Space Station" - Ethan Blansett, Sandia National Laboratories
4:00-4:20		"The AFRL-UNM High-End Reconfigurable System. Analyses of a Reconfigurable Multiprocessor Architecture for Space Missions" - L. Howard Pollard, Jorge Parra, University of New Mexico
4:20-4:40		"On Certain New Methodology for Reducing Sensor and Readout Integration Circuitry Digitization Noise" - Semion Kizhner, NASA Goddard Space Flight Center
4:40-5:00		"Reconfigurable Fault Tolerance for FPGA-based Space Computing" - Grzegorz Cieslewski, Chris Conger, Alan D. George, Brandon Kilpatrick, NSF Center for High-Performance Reconfigurable Computing (CHREC), University of Florida
5:00-5:10	Closing Remarks – Wesley Powell, NASA Goddard Space Flight Center	

Invited Speakers

Mr. Arthur F. Obenschain - Conference Welcome

Mr. Obenschain is the Deputy Director for Goddard Space Flight Center. He shares with the Director and the Deputy Director for Science and Technology responsibility for executive leadership and overall direction and management of the Center and its assigned programs and projects. He is also responsible for providing executive oversight and technical evaluation for the development, delivery for launch and operations of the space systems assigned to the GSFC.

Previously, Mr. Obenschain was appointed as the Director of Flight Projects Directorate in September of 2004 and was responsible for the day-to-day management of the more than 40 Space and Earth Science missions in formulation or implementation at Goddard as well as the coordination of the Earth Science Technology Office.

Mr. Obenschain began his career with NASA at GSFC in the early 60's as a summer engineering aide, accepting a full-time position in the power systems development area in 1966 upon his graduation. He has worked almost exclusively on hardware development projects since 1966, with emphasis in electrical systems. In 1982, after serving 5 years as a supervisor in the GSFC Engineering Directorate, Mr. Obenschain assumed the position of Observatory Manager for the Compton Gamma-Ray Observatory.

Upon his return to NASA in 1988 after working in private industry as a Program Manager for an aerospace company, Mr. Obenschain served as the Deputy Project Manager for the GSFC Space Station Freedom Development Project. In October 1989, he was appointed Project Manager for the EOS Platforms Project, a position he maintained until his selection as the GOES Project Manager. With the successful launch and in-orbit checkout of GOES-8, Mr. Obenschain transferred to the Landsat Project.

Mr. Obenschain was appointed to the position of Project Manager in September 1994 with the transfer of Landsat-7 from the Department of Defense. In December 1996, he was appointed Project Manager of the Earth Science Data and Information System (ESDIS) Project, a position he held until October 1998 when he assumed responsibility for the leadership of the Electrical Systems Center within AETD.

Mr. Obenschain was selected as the Director of the Applied Engineering and Technology Directorate in June 2000, having previously served as the Deputy Director of AETD since October 1999.

Mr. Obenschain earned a B.S. in Electrical Engineering from the University of Maryland. He is the recipient of NASA's Distinguished Service Medal, Exceptional Service Medal, Outstanding Leadership Medal, Equal Opportunity Medal, and Goddard's Award of Merit. He is the 1995 recipient of the American Institute of Aeronautics and Astronautics (AIAA) von Braun Award for Excellence in Space Program Management.

Dr. Steven Suddarth - "FPGAs and the Quest for New Relevance of America's Space Program"

Steve Suddarth is the Director of the FPGA Mission Assurance Center (FMAC). As such, he is responsible for leading a funded collaboration between Academe, Government and Industry to ensure design success and deployment of programmable logic in space, military and civil applications.

A retired Air Force Colonel with 24 years of service, Dr. Suddarth served his last assignment as the liaison from U.S. Strategic Command to the National Laboratories. Located in Los Alamos, NM, Col Suddarth initiated and oversaw a development team for key technologies in the war on terror, creating and leading a team of 60 people spanning four sites.

Steve has also served in key leadership capacities in the Air Force Research Laboratory, Air Force Materiel Command, and the Air War College. In these, Dr. Suddarth organized, led and contributed to several efforts within the Air Force to rejuvenate interest and investment in technology, assembling plans to expand graduate education by a factor of 5, restoring the Air Force Institute of Technology. Further efforts included developing a course of instruction that is in wide use within the Air Force for the indoctrination and instruction of incoming scientists and engineers, while contributing to current war efforts as well as demonstrating a data-sharing capability among fighter aircraft.

Dr. Suddarth has led as well as participated technically on several substantial computer engineering/embedded systems projects. These include the development of a first-ever 3-dimensional mixed analog/digital image processor operating 3

orders of magnitude faster than state-of-the-art, build and test of several airborne optical sensing systems, robotics systems to include small unmanned helicopters, and software systems for a large military space program.

Steve is a 1982 graduate of the U.S. Air Force Academy (B.S. in Electrical Engineering and Humanities), and he holds an M.S. and Ph.D. in Electrical Engineering from the University of Washington. Steve is also a graduate of the Brazilian Air Command and Staff College, U.S. Joint Forces Staff College, and the U.S. Air War College. He has authored over 20 papers, and is fluent in French and Portuguese.

Douglas Comstock - "Meeting Technology Needs through Innovative Partnerships at NASA"

Douglas A. Comstock is the director of NASA's Innovative Partnerships Program (IPP). The IPP provides leveraged technology for NASA's mission directorates, programs and projects through investments and technology partnerships with industry, academia, government agencies and national laboratories.

Comstock also is responsible for directing the IPP portfolio of technology investments and partnering mechanisms including Small Business Innovation Research, Small Business Technology Transfer Research, the Centennial Challenges and the Innovative Partnerships Seed Fund. Additionally, he is responsible for intellectual property management and technology transfer that will provide broad societal benefits from the nation's investment in NASA's space and aeronautics missions, and for encouraging and facilitating partnerships with the emerging commercial space sector including the agency's purchase of emerging commercial services.

Comstock previously served as the NASA comptroller, responsible for the preparation, tracking, presentation and defense of NASA's budget to the White House Office of Management and Budget (OMB) and the Congress. As the founding director of NASA's Strategic Investments Division, he was responsible for integrating NASA's strategic planning and program analysis supporting budget decisions into a single organization. Under his leadership, NASA was the first agency to achieve GREEN status as part of the President's Management Agenda for Budget and Performance Integration and NASA received its first honorable mention for the President's Quality Award.

Before coming to NASA, Comstock spent four years as a program examiner in OMB, with responsibility for NASA's human space flight activities, biological and physical research and personnel. Prior to his government service, he was Director of Engineering with the Futron Corporation, a Bethesda, Md.-based technology consulting firm, and began his career with General Dynamics Space Systems Division, conducting preliminary design and systems analysis for numerous aerospace systems, from strategic defense to advanced space transportation.

Comstock has undergraduate degrees from the University of Washington in both mechanical engineering and architecture. He did his graduate studies at the Massachusetts Institute of Technology and received masters degrees in both aeronautics and astronautics, and technology and policy.

Dr. Harley Thronson - "Past, Present, and Future of In-Space Servicing of Major Scientific Spacecraft"

Dr. Thronson's responsibilities include identification, assessment, and advocacy for advanced human/robotic programs at NASA Goddard Space Flight Center in coordination with other NASA Centers, industry, and the scientific community.

Previously, while working at NASA Headquarters, he was responsible for selection and development of advanced technologies that will significantly enhance future science missions such as large astronomical observatories in space and robotic missions to Mars, other planets, and the Moon. He has also served as the program scientist for the Hubble Space Telescope (HST), the Spitzer Space Telescope (SIRTF), the James Webb Space Telescope (JWST), and the Stratospheric Observatory for Infrared Astronomy (SOFIA), among other missions. Over the past few years, he has served as senior scientist on a variety of long-range planning activities and led three NASA HQ teams that developed science and technology priorities for President George Bush's *Vision for Space Exploration*.

Dr. Thronson received his Ph.D. in astrophysics in 1978 from the University of Chicago and has been a faculty member and on the senior staff of the Universities of Arizona and Wyoming, and the Royal Observatory, Edinburgh. He has published more than 100 research papers and co-edited 12 books.

Dr. Alan George - "Reformation, Formulation, and the Future of Reconfigurable Computing"

Dr. Alan D. George is a professor of electrical and computer engineering (ECE) at the University of Florida, the flagship university in the fourth most populous state in the US. He leads the National Science Foundation's Center for High-Performance Reconfigurable Computing (CHREC, pronounced "shreck"). He also chairs the university committee on high-performance computing (HPC).

His career has included two decades in academia and almost a decade in industry, primarily focusing upon ECE-centric research challenges in HPC and high-performance embedded computing (HPEC). Professor George earned his B.S. in Computer Science and M.S. in ECE from the University of Central Florida, and Ph.D. in Computer Science from Florida State University. He can be reached by email at george@chrec.org. More information on CHREC can be found at www.chrec.org.

Poster Presentations

Title	Author(s)
Retention Projections for SONOS Nonvolatile Semiconductor Memories (NVSMs) Based on Activation Energy Studies	Dennis Adams, Northrop Grumman Corporation
Ultra-High Speed Rad Hard PLD/FPGA Interconnects Technique for the next Generation High Performance on Board Computing	Vladimir Katzman, Jeb Binkley, ADSANTEC Inc.
Low power fault tolerant state machine design using reversible logic gates	Kaushal D. Buch, eInfochips Ltd.
Meeting DO-254 Compliance Requirements	David Lundgren, Aldec, Inc.
Reprogrammable Prototyping for Rad-Hard FGPAs	Igor Tsapenko, Aldec, Inc.
SpaceWire Based Fault Tolerant Architecture for Redundant Systems	Doug Cornelsen, Bristol Aerospace Limited
Reconfigurable Computing in Practice: Demonstrations and Benchmarking for Avionics	Clint Patrick, NASA Marshall Space Flight Center
A breadboard for real time image processing on board Gaia	Shan Mignot, Observatoire de Paris
Optimized Virtex-4 FPGA Self Hosting Configuration Management	Chen Wei Tseng, Xilinx Corporation
Virtex-4 FPGA SEU Mitigation Design Consideration	Chen Wei Tseng, Xilinx Corporation
A Power-Efficient Design Approach to Radiation Hardened Digital Circuitry using Dynamically Selectable Triple Modulo Redundancy	Brock J. LaMeres, Montana State University
A Device-Level Architecture for FPGA Co-Processors in Embedded Computing Platforms	Chris Conger, Honeywell Inc., Space Electronic Systems
A New Radiation Tolerant Field Programmable Gate Array Based on Non-Volatile Flash Configuration Switches	Jih-Jong Wang, Actel Corporation
A Multi-Mode Reconfigurable OFDM Communication System on FPGA	Viktor Prasanna, University of Southern California
FPGA-Based High Altitude Aircraft Systems	Paul Graham, Los Alamos National Laboratory
SET Characterization and Mitigation in RTAX-S Antifuse FPGAs	Sana Rezgui, Actel Corporation
Actel RTAX4000S Space Qualification Update	Solomon Wolday, Actel Corporation
An FPGA-Enhanced Ball Stack Rad-Hard Non-Volatile Memory	Don Hayashigawa, NxGen Electronics Inc
Using Fusion Mixed-signal Programmable System Chips to Implement System Management in uTCA Applications	Ken O'Neill, Actel Corporation
Performance Improvement in FPGA-based Data Acquisition Systems using PCI-Express	Melissa C. Smith, Clemson University
Computational Modeling Using FDTD Methods on Reconfigurable Co-Processor Platform	Xinming Huang, Worcester Polytechnic Institute
An Area-Efficient LDPC Decoder Architecture and Design on FPGA	Xinming Huang, Worcester Polytechnic Institute
Power Conscious Design Methodology for Actel FPGA	Mir Sayed Ali, Actel Corporation
RTAX-S Design Checklist	Min Nguyen, Actel Corporation
Tracing Requirements from the System Level to Subsystem Implementation and Verification with ReqTracer	Pete Decher, Mentor Graphics Corporation
Modern Verification Methods for Safety-Critical and DO-254 Compliant FPGA/ASIC Devices	David Landoll, Mentor Graphics Corporation
Constrained Random Verification with VHDL	Jim Lewis, SynthWorks Design Inc.
Functional and Performance validation of the 80S32 uC for Space Applications	Stefanos Skoulaxinos, Integrated System Development (ISD)
"Hard real-time operation in Gigabit-Ethernet networks using FPGA-based TTEthernet IP"	Guenter Motzet, TTTech
"Fault Tolerant, Reconfigurable FPGAs in High-Speed Encryption Application"	Edward Li, SpaceMicro

Industrial Exhibits

3D Plus USA	NASA Electronic Parts and Packaging (NEPP) Program
Actel	National Reconnaissance Office
Aeroflex Colorado Springs /Aeroflex Gaisler	Northrop Grumman
Agility Design Solutions	NSF Center for High Performance Reconfigurable Computing (CHREC)
Aldec, Inc.	Pico Computing, Inc.
Atmel	SEAKR Engineering, Inc.
BAE Systems	Synplicity, a Synopsys Company
Mentor Graphics	US Semiconductor
NASA Innovative Partnership Program (IPP) Office	Xilinx