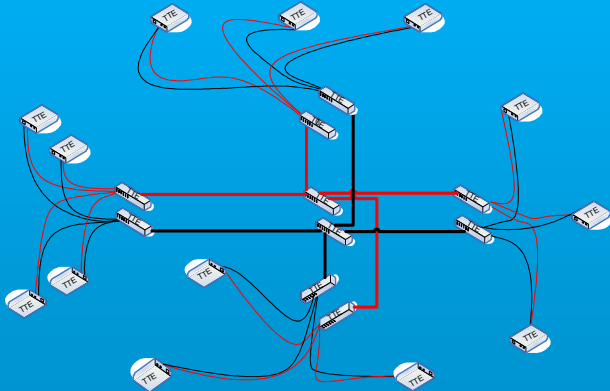
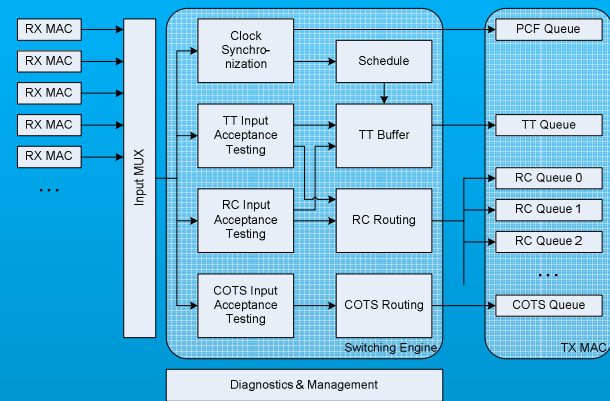


Fault-tolerant Synchronization in Complex Ethernet Networks

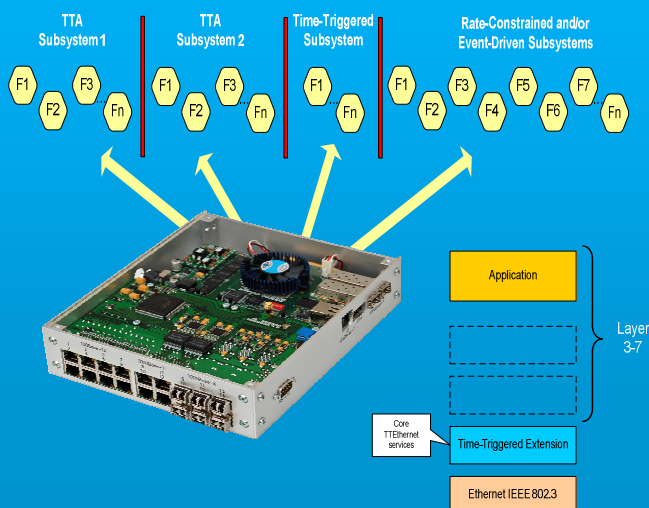


COTS TTEthernet Switch IP*

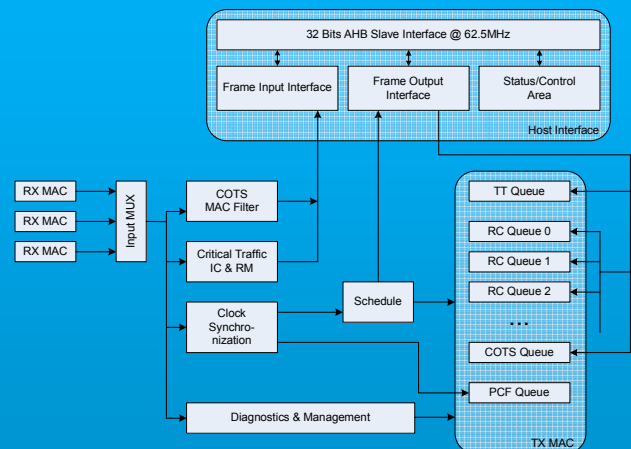


*Implementation example: Stratix II GX FPGA Family

Robust Partitioning among Distributed System Functions



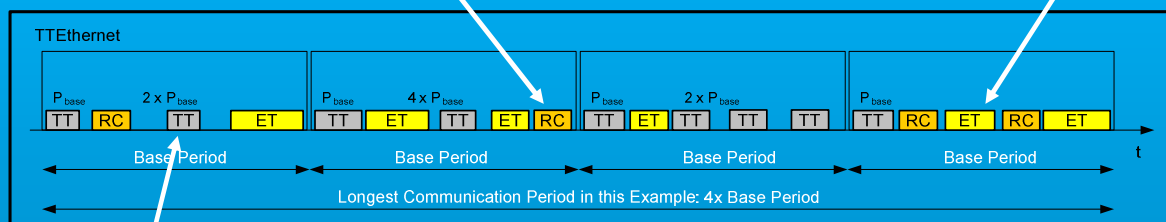
COTS TTEthernet Controller IP*



TTEthernet Principle: Compatible with COTS Ethernet Hardware

Rate-Constrained (RC)

Non-critical Standard Ethernet (ET)



Pre-planned Time-Triggered (TT) Data Flows

TTTech