MAPLD 2009 - Greenbelt, Maryland

August 31 - September 3, 2009

Sponsored by NASA Goddard Space Flight Center and the NASA Electronic Parts and Packaging (NEPP) Program

Workshop Program

Initiated in 1998, the Military/Aerospace Programmable Logic Device (MAPLD) workshop addresses the unique issues surrounding the use of PLDs for military/aerospace applications that must operate with a high degree of reliability, often in harsh environments. For more information on MAPLD 2009, please visit http://nepp.nasa.gov/mapld_2009/.

Seminars

"DO-254 Overview, Pro's, Con's, and Discussion" - Michelle Lange, Mentor Graphics
"Packaging Concerns/Techniques for Large Devices" - Mike Sampson, NASA Goddard Space Flight Center
"OPERA RHBD Multi-Core" - Mike Malone, Draper Labs
"CHREC Novo-G" - Alan George, University of Florida
"Micro/NanoSats/SpaceCube" - Steve Suddarth, Configurable Space Microsystems Innovations & Applications Center (COSMIAC)
"Memory Technology for Space" - Ian Troxel, SEAKR Engineering
"Tools for FPGA SEU Mitigation/Fault Tolerance" - Heather Quinn, Los Alamos National Laboratory

Program Sessions

Session A - "PLD Applications"
Co-Chair: David Podany, Department of Defense
Co-Chair: Matthew French, University of Southern California Information Sciences Institute (USC ISI)

Session B - "PLDs and Supporting Devices"
Co-Chair: Joe Fabula, Xilinx Corporation
Co-Chair: Sana Rezgui, Actel Corporation

Session C - "Radiation Effects and Mitigation in PLDs"
Co-Chair: Heather Quinn, Los Alamos National Laboratory
Co-Chair: Gary Swift, Xilinx Corporation

Session D - "Design and Verification Tools and Methodologies"
Co-Chair: Tim Gallagher, Lockheed Martin Corporation
Co-Chair: Craig Kief, Configurable Space Microsystems Innovations & Applications Center (COSMIAC)

Session E - "PLD-Based System Architectures"
Co-Chair: John Demello, Air Force Research Laboratory
Co-Chair: Mythi To, Sandia National Laboratories

Poster Session
Chair: Maxime Pinchinat, NASA Goddard Space Flight Center

Industrial Exhibits
Chair: Teresa Farris, Aeroflex

Additional Information

For additional information regarding the workshop, please visit the MAPLD 2009 website (http://nepp.nasa.gov/mapld_2009/). If you have questions regarding the workshop, please feel free to contact:

Wesley Powell	Wesley.A.Powell@nasa.gov	Workshop Chair
Ken LaBel	Kenneth.A.Label@nasa.gov	Workshop Co-Chair
Mike Sampson	Michael.J.Sampson@nasa.gov	Workshop Co-Chair

Monday (8/31/09)

Seminars	
7:30 - 9:00	**Registration**
9:00-9:05	**Seminar Introduction** – Tim Gallagher, Lockheed Martin
9:05-9:50	**"DO-254 Overview, Pro's, Con's, and Discussion"** - Michelle Lange, Mentor Graphics
9:50-10:40	**"Packaging Concerns/Techniques for Large Devices"** - Michael Sampson, NASA Goddard Space Flight Center
10:40-11:30	**"OPERA RHBD Multi-Core"** - Michael Malone, Draper Labs
11:30-1:00	**Lunch**
1:00-1:50	**"CHREC Novo-G"** - Alan George, University of Florida
1:50-2:40	**"Micro/NanoSats/SpaceCube"** - Steve Suddarth, Configurable Space Microsystems Innovations & Applications Center (COSMIAC)
2:40-3:00	**Break**
3:00-3:50	**"Memory Technology for Space"** - Ian Troxel, SEAKR Engineering
3:50-4:40	**"Tools for FPGA SEU Mitigation/Fault Tolerance"** - Heather Quinn, Los Alamos National Laboratory
4:40-5:00	**Questions and Answers**

Seminar Presenters

Micelle Lange - Michelle Lange, the DO-254 program manager at Mentor Graphics Corporation, has held various technical and business-oriented roles in the field of electronic design automation (EDA) for nearly 20 years. In her current role, Michelle has taken a variety of DO-254 training classes, forged relationships with the industry leaders in the DO-254 community, discussed DO-254 issues and challenges with numerous companies, and is an active member of both the original European DO-254 Users Group as well as the newly formed US DO-254 Users Group. Michelle has a BSEE maxima cum laude from the University of Portland and an MBA summa cum laude from University of Phoenix.

Michael Sampson - Mike Sampson has been co-Manager of the NASA EEE Parts (NEPP) Program since October 1, 2003. The NEPP program is a cross-Agency activity that evaluates new and emerging EEE part technologies, shares information and develops tools for EEE parts assurance. He has also been the NASA Goddard Space Flight Center (GSFC) Alert Coordinator for the past 6 years. Mike has worked for NASA for almost 15 years. Before joining NASA, Mike spent five years as a NASA support contractor and before that, more than twenty years as an engineer and engineering manager in manufacturing. Mike has a Master of Science degree in Engineering Management from the University of Maryland.

Michael Malone - Michael Malone is a program manager for Draper Laboratory in Cambridge, MA. For the last three years, Mike has supported the government on the On-board Processing Expandable Reconfigurable Architecture (OPERA) program. OPERA is developing a next generation multicore space processor using Radiation Hardened by Design (RHBD) techniques. He has also worked numerous space flight missions including four Hubble Space Telescope instruments. Mike received his Masters and Bachelors in Electrical Engineering from the University of Colorado at Boulder.

Alan George - Alan D. George is Professor of Electrical and Computer Engineering at the University of Florida, where he founded and directs the NSF Center for High-performance Reconfigurable Computing (CHREC). His research interests focus upon new theories, concepts, methods, architectures, systems, tools, and applications in reconfigurable, parallel, and fault-tolerant computing, for embedded, general-purpose, or high-performance systems, from satellites to supercomputers. He received the B.S. degree in Computer Science and M.S. in Electrical and Computer Engineering from the University of Central Florida, and the Ph.D. in Computer Science from the Florida State University.

Steve Suddarth - Steve Suddarth is the Director of the Configurable Space Microsystems Innovations and Applications Center. As such, he is responsible for leading a funded collaboration between Academe, Government and Industry to ensure design success and deployment of reconfigurable systems in space, military and civil applications. Steve has also served in key leadership capacities in the Air Force Research Laboratory, Air Force Materiel Command, and the Air War College. Steve is a 1982 graduate of the U.S. Air Force Academy (B.S. in Electrical Engineering and Humanities), and he holds an M.S. and Ph.D. in Electrical Engineering from the University of Washington.

Ian Troxel - Ian Troxel is currently the Future Systems Architect at SEAKR Engineering, Inc. His research interests include next-generation aerospace processing systems and radiation effect characterization and mitigation for commercial microprocessors. Ian earned a Ph.D. in ECE from the University of Florida in 2006 in which his dissertation focused on the design and development of a mission and fault management middleware for the Dependable Multiprocessor developed for NASA's New Millennium Program Space Technology 8 mission.

Heather Quinn - Heather Quinn has a B.A. in mathematics and physics from Knox College, and a M.S. and Ph.D. in Electrical Engineering from Northeastern College. She has been researching FPGAs for ten years, including software/hardware codesign issues with integrating FPGAs into traditional computation systems and fault-tolerant space-based FPGA computation. For the last five years she has focused on radiation effects on the Xilinx Virtex devices.

Tuesday (9/1/09)

7:30 - 9:00	Registration	
9:00-9:20	Conference Welcome – Orlando Figueroa, NASA Goddard Space Flight Center	
9:20- 9:40	Session A	Sandi Habinc - Using a FLASH Based FPGA in a Miniaturized Motion Control Chip
9:40- 10:00		Doug Cornelsen - Implementation of a Sigma Delta Analog to Digital Converter in an RTAX FPGA
10:00-10:20		John Dickinson - Architectural Tradeoffs for CCSDS Formatting and High Speed SSR Interface
10:20-10:40	Break	
10:40-11:00	Session A	Wilfried Steiner - Reliable Synchronization for Multi-Hop Networks and its Realization in FPGA
11:00-11:20		Thomas Kong - Hardware Implementation of a Novel Method for Reducing Sensor and Readout Electronic Circuitry Noise in Digital Domain
11:20-11:40		Semion Kizhner - On DESTINY Science Instrument Electrical and Electronics Subsystem Framework
11:40-12:00		David Guzman - Versatile board to study the in-orbit radiation effects on microelectronics components
12:00-1:30	Lunch	
1:30-1:50	Session A	David Petrick - Application of SpaceCube in a Space Flight Systems
1:50-2:10	Session B	Douglas Sheldon - FPGAs, Scaling and Reliability
2:10-2:30		Edward Leventhal - Universal Reconfigurable Translator Module (URTM)
2:30-3:15	Industrial Exhibits Introductions (Building 8)	
3:15-6:00	Industrial Exhibits (Building 28 Atrium) – Light refreshments provided by Actel Corporation	

Wednesday (9/2/09)

8:00-8:20	Session B	Gerry Maloney - Non Hermetic Ceramic Flip Chip Package Reliability Assessment
8:20-8:40		Charlie Howard - FLASH Mitigation Strategies and Tradeoffs
8:40-9:00		Gary Swift - Maximizing the Robustness of Applications using Advanced Reconfigurable FPGAs in Upset Environments
9:00-9:20		Solomon Wolday - Actel Power Supply Transient Evaluation on RTAX-S and RTSX-SU Devices
9:20-9:40		Vladimir Katzman - Fully TID-Hardened Space Wire/Gigabit Ethernet SerDes Based On A Proprietary Library Of SCL Cells.
9:40-10:00	Break	
10:00-10:20	Session C	Shankarnarayanan Ramaswamy - Reconfigurable, High Density, High Speed, Low Power, Radiation Hardened FPGA Technology
10:20-10:40		G. Alonzo Vera - A Programmable Configuration Scrubber for FPGAs
10:40-11:00		Yubo Li – Synchronization Issues of TMR Crossing Multiple Clock Domains
11:00-11:20		Gregory Miller – Preliminary Analysis of a soft-core processor in a Rad Hard By Design Field Programmable Gate Array
11:20-11:40		Nathaniel Rollins - Low-Cost High-Performance Reprogrammable Processors for Space-Based Applications
11:40-12:00		Joseph Fabula - Initial Dose Rate Testing of the SIRF FX-1
12:00-1:30	Lunch	
1:30-1:50	Session C	Roberto Monreal - Interaction of Ionized-Particles with Advanced Signal Processing Devices in Field-Programmable Gate Arrays and Development of Mitigation Techniques for Space Applications
1:50-2:10		Melanie Berg - Embedding Asynchronous FIFO Memory Blocks in Xilinx Virtex Series FPGAs Targeted for Critical Space System Applications
2:10-2:30		John Cochran - A SET Resistant Majority Voting Circuit
2:30-2:50		Sana Rezgui - Radiation Performance of Embedded CoreABC Controller on the New Radiation-Tolerant
2:50-3:10		Bernard Bancelin - ATMEL ATF280E Rad Hard SRAM Based FPGA: SEE test results and fault injection
3:10-6:00	Poster Session/Industrial Exhibits (Building 28 Atrium)	

Thursday (9/3/09)

8:00-8:20	Session D	Jaroslaw Kaczynski - Can Assertions Save Military PLD Designs?
8:20-8:40		Jaroslaw Kaczynski (for Igor Tsapenko) - DO-254 Trends and Efficient Methods for Hardware Verification
8:40-9:00		Steven Suddarth - DO-254: Reliability, Cost and Payoff
9:00-9:20		Anant kumar Jain - Formal Verification of Advanced Synthesis Optimizations
9:20-9:40		Walid Najjar - Modular Design of FPGA-Based Accelerators in C
9:40-10:00		Ely Soto - DSP development and verification issues with Matlab generated RTL
10:00-10:20	Break	
10:20-10:40	Session D	Buu Huynh - RTL and Synthesis Design Approach to Radiation-Harden and Fail-Safe Targeted Applications
10:40-11:00		Grzegorz Cieslewski - Simple Portable FPGA Fault Injector
11:00-11:20		Jon-Paul Anderson - Reduced Cost Reliability via Statistical Model Detection
11:20-11:40	Session E	Vladimir Katzman - Fully Space Wire Compatible Switching Fabric With Improved TID Tolerance, Reliability, and Speed
11:40-12:00		Matthew French - Fault Tolerant Techniques for System on a Chip Devices
12:00-1:30	Lunch	
1:30-1:50	Session E	Sam Stratton - Fault Tolerant LEON Processing, Devices and Circuit Cards
1:50-2:10		Shaon Yousuf - Run-Time FPGA Partial Reconfiguration for Image Processing Applications
2:10-2:30	Break	
2:30-3:30	Invited Speaker - Dr. Douglas Sheldon, Jet Propulsion Laboratory “Reliability Considerations”	
3:30-3:40	Break	
3:40-4:00	Session E	Brock LaMeres - Design of a Radiation Tolerant Computing System Based on a Many-Core FPGA Architecture
4:00-4:20		David Petrick - SpaceCube: Current Missions and Ongoing Platform Advancements
4:20-4:40		Dorian Seagrave - Universal Reconfigurable Processing Platform for Space
4:40-4:50	Closing Remarks – Wesley Powell, NASA Goddard Space Flight Center	

Invited Speakers

Orlando Figueroa - Conference Welcome

Mr. Orlando Figueroa was appointed the Director for the Applied Engineering and Technology Directorate at the Goddard Space Flight Center in August 2005. Mr. Figueroa directs an organization of approximately 1300 civil servants responsible for providing the full range of engineering disciplines needed to enable end-to-end conceptualization, development, and use of advanced technologies in exploration and science missions for NASA or NASA-related projects. As AETD Director, Mr. Figueroa is the delegated Engineering Technical Authority and is responsible for Engineering Technical Excellence for the Center.

Mr. Figueroa has been a U.S. Government Senior Executive since 1996. Throughout his career he has a record of consistent achievements in the planning, design, development and oversight of multi-faceted scientific space missions. Well versed in interacting with multiple national and international government and non-government organizations, and considered a highly competent strategist and director of scientific systems and technology, with vast experience in the management of complex multi-project programs with total budgets in excess of $4 billion.

His past experiences include the following positions at NASA Headquarters: Deputy Associate Administrator for Programs in the Science Mission Directorate; Director for the Solar System Exploration Division; Director for Mars Exploration; and NASA Deputy Chief Engineer for Systems Engineering. Experience prior to NASA Headquarters include 22 years at Goddard as: Director of Systems, Technology and Advanced Concepts; Explorers Program Manager; Manager for the Small Explorers (SMEX) project; Manager for the Superfluid Helium On Orbit Transfer (SHOOT) Shuttle Experiment; Head of the Cryogenics Technology Section; and Lead Cryogenic Engineer for the Cosmic Background Explorer mission.

Throughout his career, Mr. Figueroa has received numerous awards. Among them are: the 2005 Service to America Medal Federal Employee of the Year, the 2004 Distinguished Presidential Rank Award, and the 2002 Meritorious Presidential Rank Award for sustained extraordinary accomplishment in management of programs of the United States Government; Hispanic Business Magazine ranking as one the most influential Hispanics in the Nation in 2004 and 2005; the 2002 Pioneer Award from the Hispanic Engineer National Achievement Awards Corporation for his contribution to the advancement of science and technology and for promoting the education of our youth; NASA Outstanding Leadership Medals in 2004 and 1993; and the 1994 Community Stars Award from the Maryland Science Week Commission, for his work and support of innovative education programs between NASA, industry and Maryland Schools.

Mr. Figueroa received an honorary doctorate degree in science from Dominican College in New York in 2004. He is the author of several technical publications in the field of cryogenics, the SMEX missions, and the Mars Exploration Program. He obtained a Bachelor of Science Degree in Mechanical Engineering from the University of Puerto Rico, Mayaguez Campus in 1978, and completed advanced courses in Mechanical Engineering at the University of Maryland. Mr. Figueroa is fully bilingual in English and Spanish and lives in Silver Spring, Maryland, with his wife, Josephine, and two sons, Daniel and Alexis.

Dr. Douglas Sheldon - "Reliability Considerations"

Dr. Sheldon is currently the Group Supervisor for Electronic Parts Engineering at the Jet Propulsion Laboratory. He is also a principal investigator in areas of non-volatile memory and FPGA research and has been at JPL since 2003. Dr. Sheldon has over 25 years experience in the development, manufacture and application of semiconductors. He has held various engineering and management positions at companies that include Agilent Technologies, Lattice Semiconductor, Racom Systems, Ramtron and Inmos.

Dr. Sheldon has a BA in Physics from the University of Colorado, an MS in Physics from the University of Oregon and a Doctorate in Management from Colorado Technical University.

Poster Presentations

Title	Author(s)
Development of FPGA Based Verification Simulation Accelerator	Gary Burke
PaSiVe: A Design Workflow for Fast Prototyping Innovative Signal Processing Applications on FPGA	Zhongren Cao
A Requirements-Driven PLD Design Flow	Dominic Lucida
Solder Joint Health Monitoring Testbed System	Mike Delaney
Synthesis of fault tolerant circuits for FSMs & RAMs	Rajiv Garg
Aeroflex Solutions for Stacked Memory Packaging	Ronald Lake
Avoiding Metastability in FPGA Devices	David Landoll
Architectural Analysis for Quantifying Trade-offs to Make the Right Decision for Implementation	John McDonald
Vendor Independent SEE mitigation solution for FPGAs	Kamesh Ramani
Functional Verification in Space Applications	Gary Roosevelt
Enabling Security in ProASIC3 FPGAs, with Hardware and Software Features	Hans Schmitz
Comparison of Single-Event Effect Mitigation Methods using Design Impact and Application Performance Metrics	Ian Troxel
Re-programmable Prototyping for Actel™ RTAX and RTSX space-flight systems designs	Igor Tsapenko
Electrostatic Discharge (ESD) performance simulation enabled IC design kit for robust ESD reliability design	Vesselin Vassilev

Industrial Exhibits

3D Plus USA	Micro-RDC
Actel	NASA Electronic Parts and Packaging (NEPP) Program
Aeroflex Colorado Springs /Aeroflex Gaisler/Aeroflex Metelics/Aeroflex Plainview	NASA Innovative Partnership Program (IPP) Office
AiTech Defense Systems	NSF Center for High Performance Reconfigurable Computing (CHREC)
Aldec, Inc.	Pico Computing, Inc.
Atmel Nantes S.A.S.	Sital Technology LTD
BAE Systems	Southwest Research Institute (SWRI)
Configurable Space Microsystems Innovations & Applications Center (COSMIAC)	Space Micro/NxGen
Doulos	Synthworks
Element CXI	TTTech
Mentor Graphics	Xilinx Inc.