OPERA RHBD Multi-core

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MAPLD – 2009

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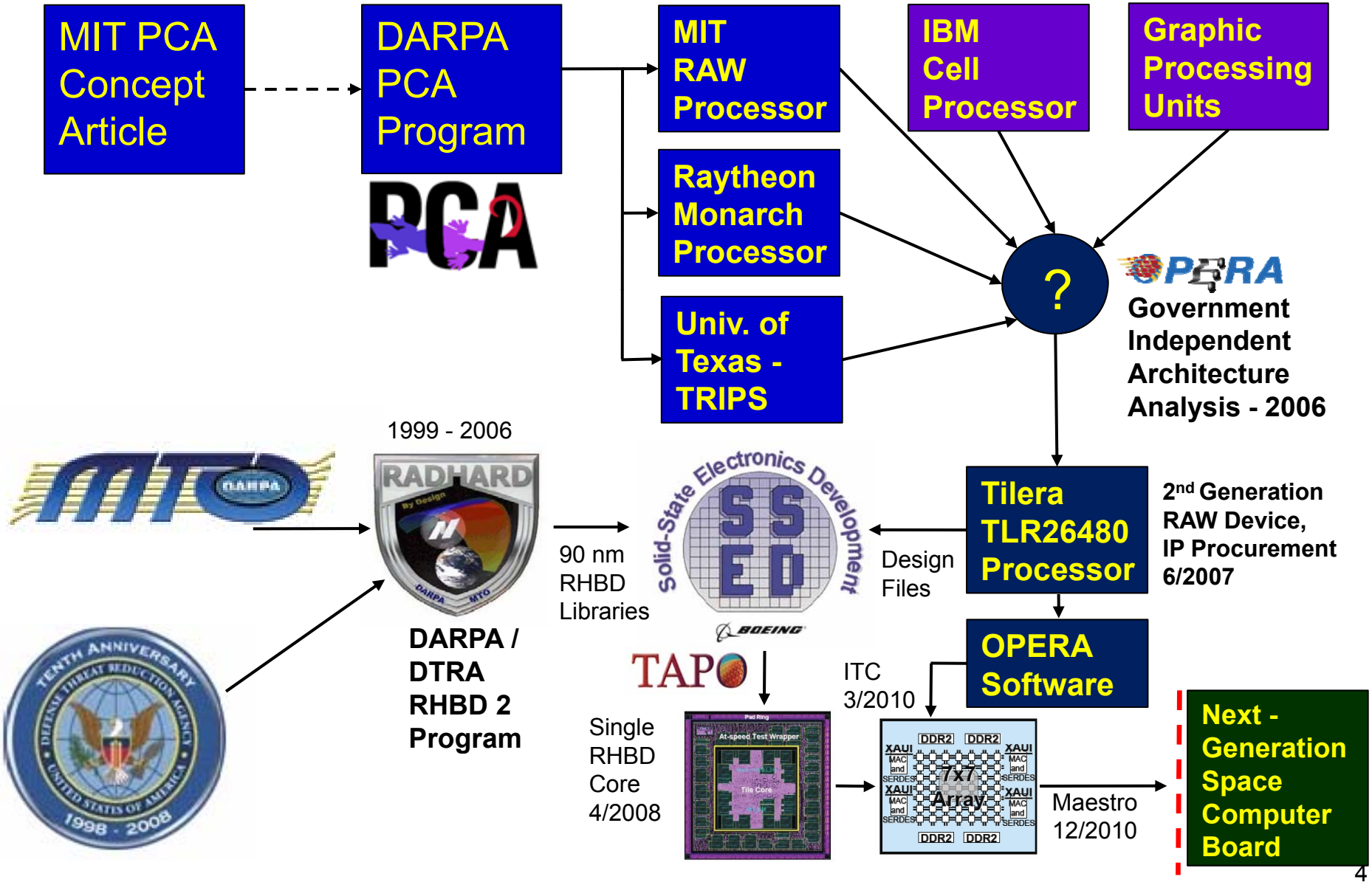
OPERA RHBD Multi-core Agenda

- **OPERA Program History**
- **Multi-core Motivation**
  - Why Multi-core For Space
- **The OPERA Hardware and Software**
  - The Maestro chip
  - Opera Software Architecture
- **Radiation Hardening By Design Overview**
  - Single tile radiation performance
- **Roadmaps and Summary**

OPERA Definitions

- **OPERA Program**
  - The On-board Processing Expandable Reconfigurable Architecture (OPERA) Program
- **RHBD Program**
  - DTRA / DARPA's Radiation Hardened By Design (RHBD) II Program
- **OPERA Single Core (or Tile) – Product Demonstration Vehicle (PDV) #1**
  - Single RHBD core with test wrapper
  - RHBD Program Product Demonstration Vehicle #1 (PDV1)
- **Integrated Test Chip (ITC)**
  - First pass Maestro device testing scheduled to be complete March, 2010
    - It becomes Maestro should no errors exist
- **Maestro – The RHBD 49 core processor**
  - Maestro is the radiation hardened by design 49 core general purpose processor based on the Tilera TILE64™
  - TRL 6 devices scheduled to be available December, 2010
- **MDE – Tilera's Multi-core Development Environment (MDE) for the Tile64™**
- **OSA – OPERA Software Architecture**
- **ODE – OPERA Development Environment**
- **Core or Tile – Single processor within the Maestro device**
- **SHIM – Interfaces between the core array and chip I/Os**
- **CHREC**
  - National Science Foundation's Center for High-Performance Reconfigurable Computing (CHREC)
    - University centers include Florida, George Washington, BYU, and Virginia Tech

OPERA Program History



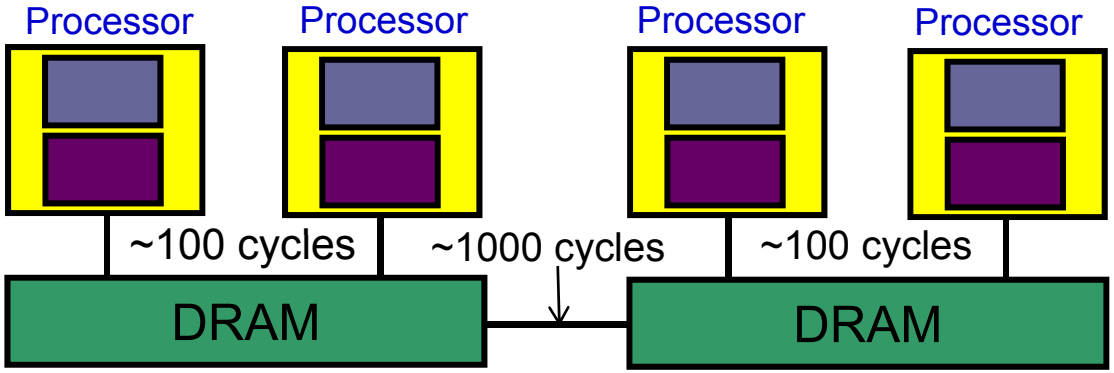
OPERA Acquisition Model

- **Leverage existing microprocessor and software advances**
  - **Program origins: DARPA Polymorphic Computer Architecture (PCA) Program**
  - **Purchase the Tilera Corporation's Intellectual Property (IP) for Government spaced-based applications**
  - **Utilize DARPA / DTRA Radiation Hardened By Design (RHBD) program libraries**
    - **Hardened 90 nm IBM 9SF CMOS design libraries**
  - **License existing 3rd party silicon designs**
    - **Floating point unit, serial – deserializer, phase locked loop, memory interfaces**
  - **Participate in the NSF's Center for High-Performance Reconfigurable Computing (CHREC) software consortium**
- **Provide OPERA hardware IP and software free to contractors involved with US space-based applications**

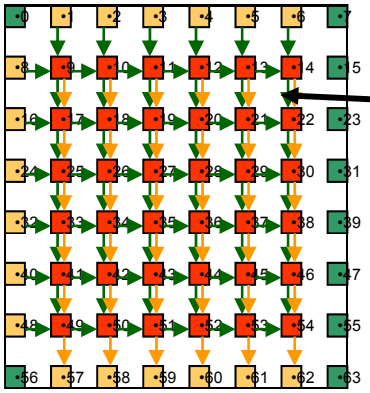
Multi-core's Advantage

- **Multi-core's advantage**
  - Improved performance per watt for most applications
  - Low latency connections between processors
  - Parallel processing capability
  - Commercial industry support

Traditional Multiprocessor



Multi-Core Architecture



On-chip interface: <10 cycle latency between processors

Multi-core architecture has inherently faster processor communication

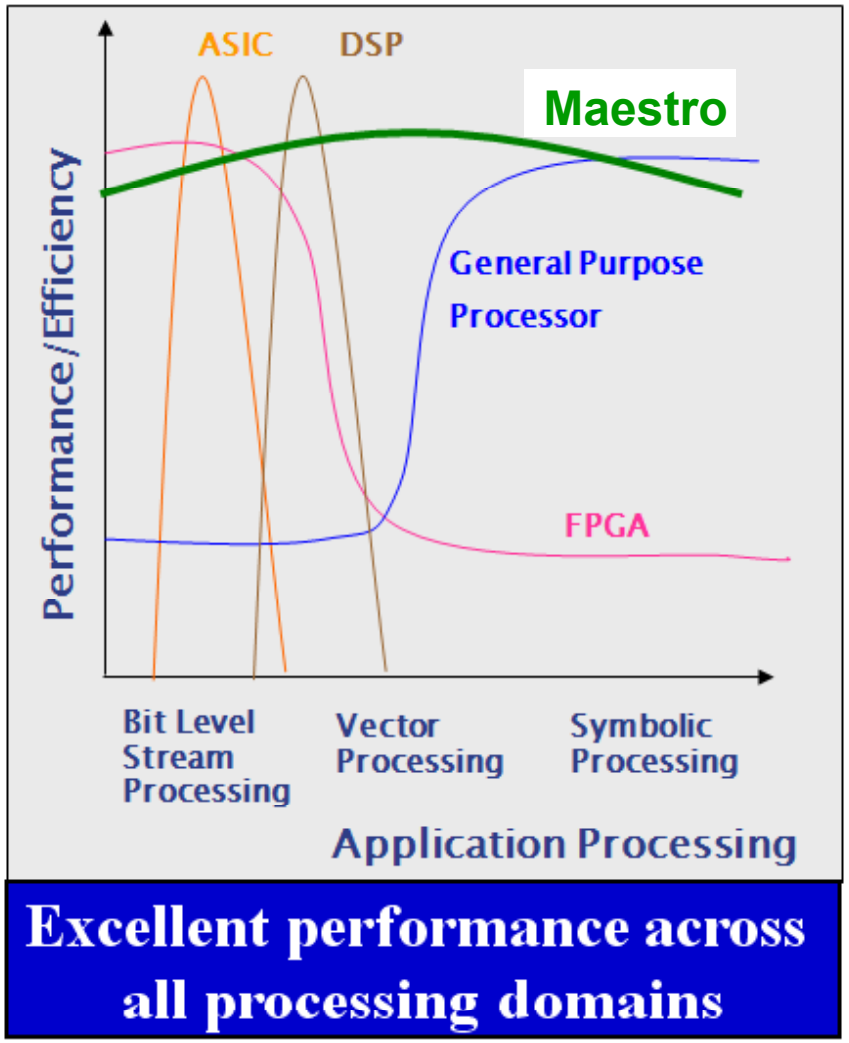
Why Multi-core for Space?

OPERA's Goal - Revolutionary Improvement in Processor Capabilities for Space Applications

- **Space processing challenges**
  - **Advancing mission requirements**
  - **Shrinking decision timelines**
  - **Providing a common high-performance hardware and software technology foundation**
- **OPERA is the Government's near-term low cost multi-core processor solution**
  - **US Government owns the OPERA multi-core intellectual property**
  - **The OPERA program's Maestro chip provides processing leap-ahead capability for space applications**
    - **Breaks the paradigm of space electronics being a decade behind the commercial sector**
    - **Produces a radiation hardened state of the art general purpose processor**
    - ***100x more capable than current space qualified general purpose processors***

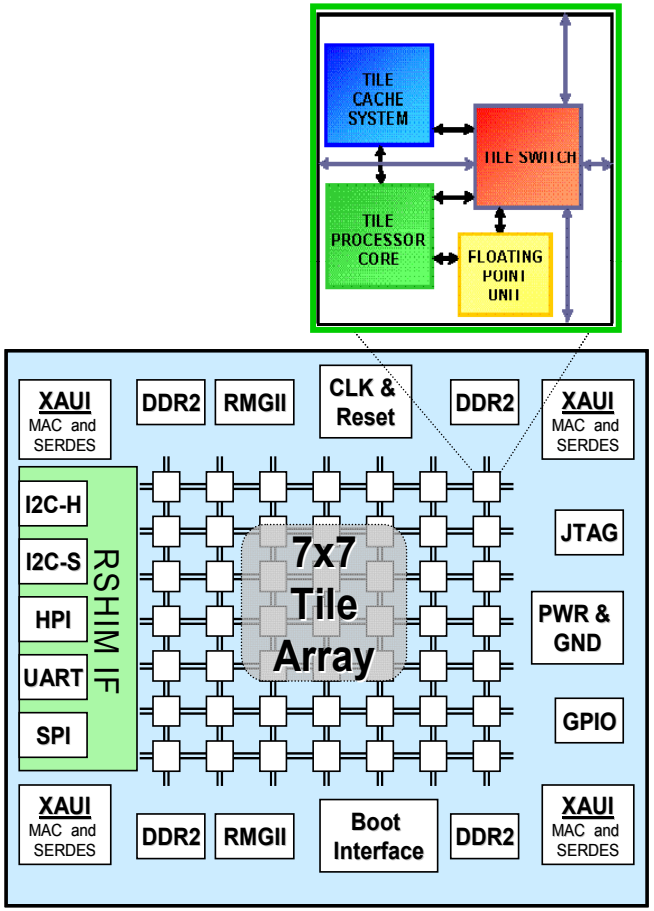
OPERA Components

- **Hardware – Maestro Chip**
  - 49 core general purpose multi-core processor
  - 45 GOPS at 310 MHz
    - 22 GFLOPS (theoretical) at 310 MHz
    - Clock speed limited by memory
  - Four - 10 Gbps SERDES XAUI interfaces
  - Radiation Hard By Design (RHBD)
  - Developed by Boeing SSED
    - Uses Tilera Corporation IP
    - Additional third party IP
- **Software**
  - Basic compiler tools
    - Complements Tilera's toolset
  - Benchmark code
  - Performance and productivity tools
    - Parallel libraries, analyzer, debugger, run time monitor, OS ports



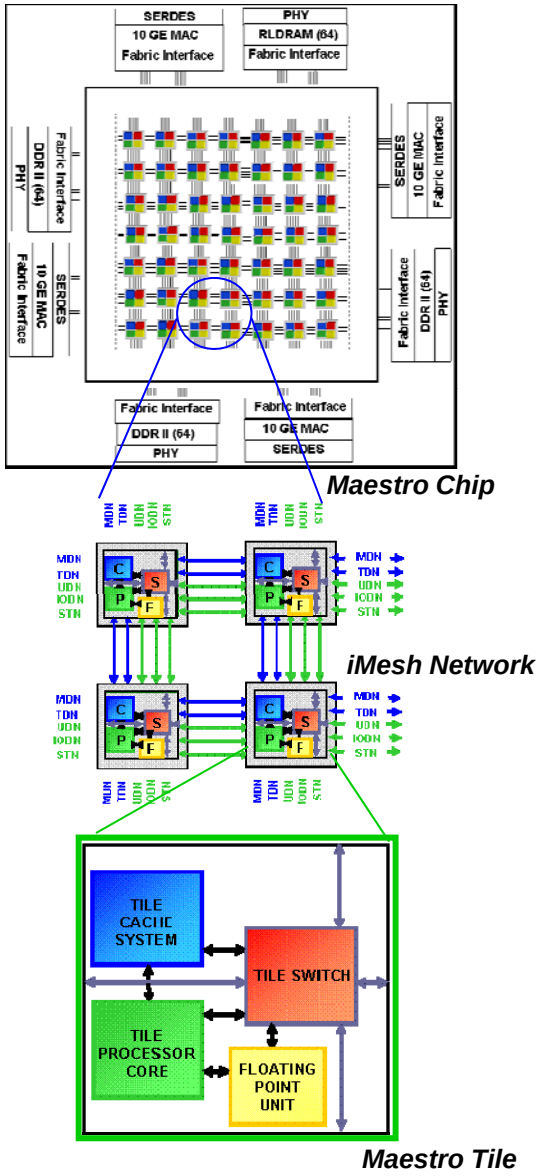
The Maestro Chip

- **RHBD version of the Tilera TLR26480**
  - 7 x 7 core array
  - IBM 9SF 90 nm CMOS process
  - < 28 Watts Peak (selectable), 20 Watts typical (using 49 cores)
    - Can “nap” cores and reduce power
    - ~ 270 mW per core
  - Floating point unit in each processing core
    - IEEE 754 compliant, single and double precision
    - Aurora FPU IP
  - 500 Krad TID
  - Demonstrate NASA TRL-6 by December 2010
  - Software compatible with the Tilera TLR26480
    - Reduced number of cores, slower clock speed, added FPU
  - Tilera TLR26480 information can be found at www.tilera.com

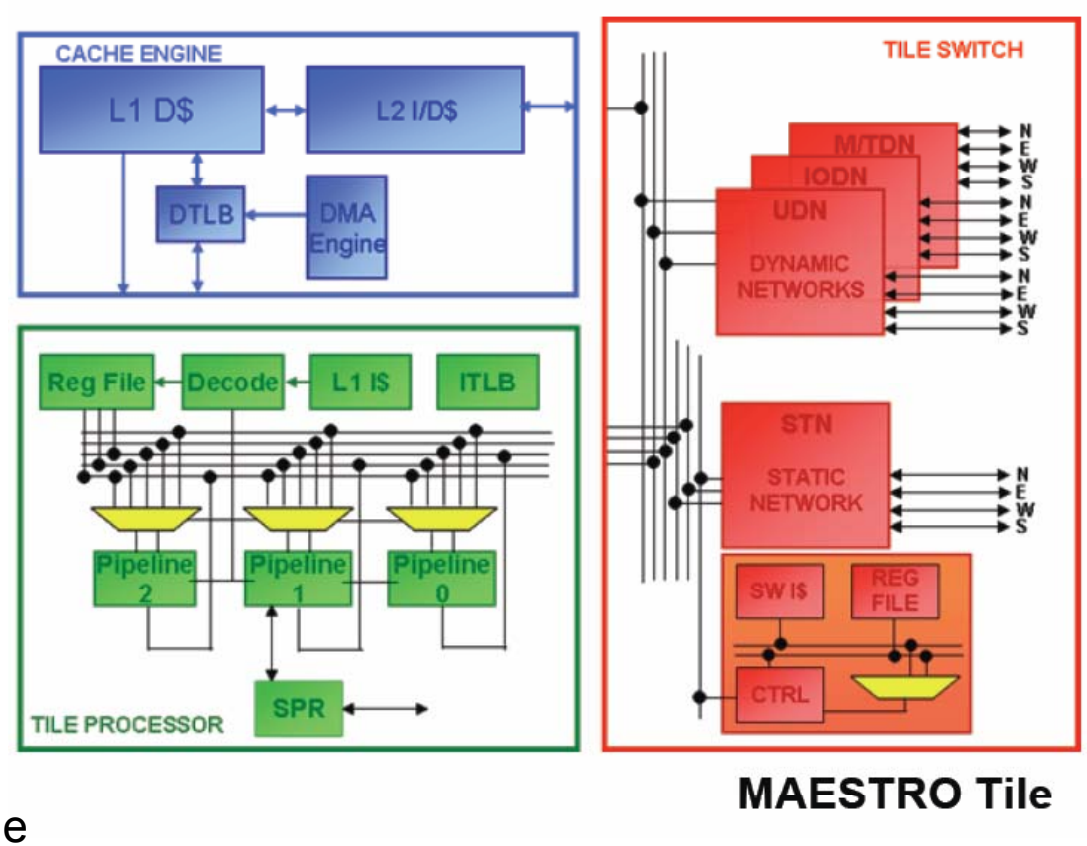


Maestro / Tilera Performance Features

- **Tiled Architecture**
  - 2-D mesh of processors, connected by low-latency high- bandwidth register-mapped networks
  - Intra-tile (i.e., intra-core) VLIW performance
  - Multi-tile ILP compilation
  - Inter-module communication acceleration at compile time
- **Processors**
  - Main processor: 3 way VLIW CPU, 64-bit instruction bundles, 32-bit integer operations
  - Static switch processor: 16-bit instructions
- **Memory**
  - L1 cache: 2 cycle latency
  - L2 cache: 7 cycle latency
  - Caches not automatically coherent across cores/tiles
  - Cores/tiles can access other cores L2 cache (“L3”)
  - Off-chip main memory, ~ 88 cycle latency
  - 32-bit virtual address space per core
- **I/O Interfaces**
  - Four integrated XAUI MACs
  - Two 10/100/1000 Ethernet MACs



Maestro / Tilera Tile Block Diagram



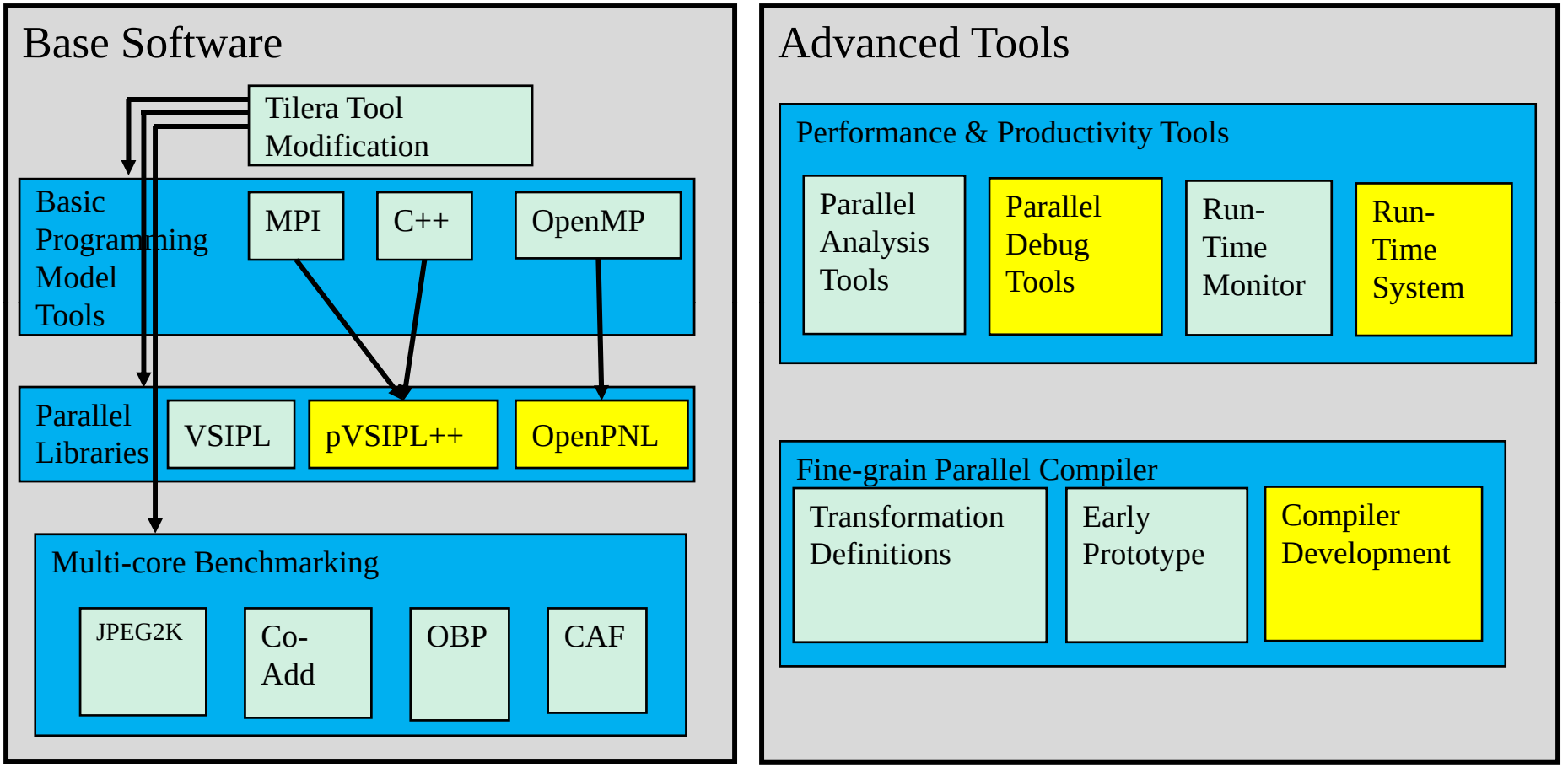
MAESTRO Tile

- **Core/Tile Processor**
  - 3 way VLIW processor
  - 8 KB L1 Instruction cache
  - Instruction Translation Look-aside Buffer (TLB)
- **Cache System**
  - 8 KB L1 Data Cache
  - 64 KB L2 I/D Cache
  - Data TLB
  - DMA Engine
- **Core/Tile Switch**
  - Switch processor
    - 2 KB switch instruction cache
    - Switch TLB
  - Static network (STN)
  - Dynamic networks
    - MDN, TDN, UDN and IODN

Maestro is not the Tilera TILE64™

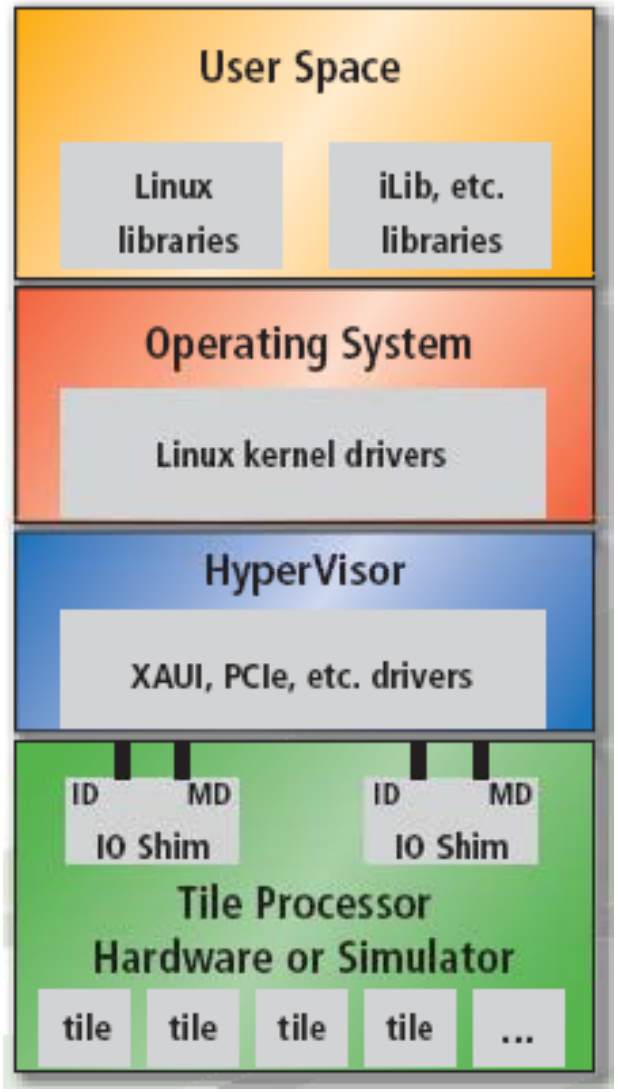
- **Maestro design modifications include:**
  - IEEE 754 compliant FPU added to every core
  - Artisan radiation tolerant commercial memories
    - 500 Krad TID
  - EDAC and scrubbing added to meet SEU rate requirements
  - DDR1/DDR2 memory interface pads
  - Cache parity
  - RHBD design techniques for radiation mitigation
    - Balanced drive strength, DICE latches, temporal filtering, guard rings, power rail sizing
  - Removed PCI Express interfaces
  - Added additional XAUI interfaces
- **With Tilera intellectual property and RHBD libraries, the OPERA program was able to design an optimized space multi-core processor for their customer**

OPERA Software Architecture



Future Activities

Maestro Software Stack



- **Complete Integrated Development Environment**
  - Eclipse based tool suite
- **User Libraries**
  - MPI, pthreads, TMC
  - Shared memory, message passing, channels, threads and processes
- **Tilera / Maestro operating systems**
  - Linux SMP 2.6
  - VxWorks SMP
    - Workbench 3.1 and VxWorks 6.7
- **Hypervisor**
  - Network interfaces
  - Tile protection

MPI = Message Passing Interface
TMC = Tilera Multi-core Components
SMP = Symmetric Multiprocessing

OPERA Intellectual Property Rollout Benefits

- **Benefits to releasing OPERA IP to contractors:**
  - Contractors can obtain the free OPERA IP if it is used in US space-based applications and they provide related IRAD / program results to the government
  - Allows industry to rapidly target US Space customers for missions with tailored multi-core solutions
  - Leverages existing and competitive space computer board markets
    - Space industry has succeeded in productizing PowerPC 750 and 603
  - Encourages growth of competitive multi-core architectures
    - Provides space industry access to a new TRL 6 RHBD multi-core processor
  - Creates innovation and sources of new space processing solutions
    - Quickens commercial/Government acceptance of multi-core architectures
    - Prompts new flight computer board development for space programs
    - Instigates ***multiple*** multi-core chip board solutions for space use
- **3rd party IP license fees apply only if the design is modified**

Radiation Hardening By Design (RHBD) Overview

OPERA Radiation Requirement

- **Radiation operating limits and specifications**
  - 500 Krad, no SEL
    - TID limited by commercial Artisan memory radiation performance
  - 1 hard reset per mission (10 year)
- **Radiation testing performed in accordance radiation test plan**
  - TID Testing
  - Dose Rate
  - Single Event Effects

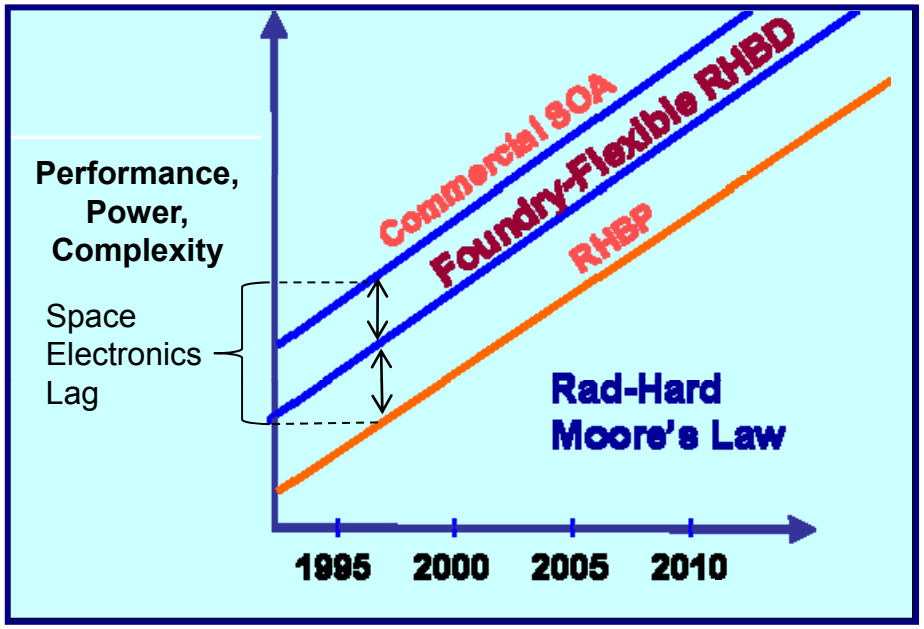
Parameter	Requirement
Total Ionizing Dose (rd(SiO_2)[3]	500 K
Single Event Effects (Latchup)[1]	
Single Event Latchup (LET in MeV-cm^2/mg)	≥ 100
Single Event Effects (Functional)[1]	
Destructive (errors/device-day)	0
Unrecoverable (errors/device-day)[4]	2.80E-04
Recoverable (errors/device-day)[5]	2.80E-03
Data Integrity (errors/device-day)	1
Dose Rate[2]	
Dose Rate Upset (rd(Si)/sec)	≥ 1E9
Dose Rate Survivability (rd(Si)/sec)	≥ 1E12

(1) Adams 10% Worst Case environment under worst-case operating conditions for voltage and temperature
(2) Dose rate testing shall be accomplished using a 20 to 50 nsec FWHM pulse, under worst-case voltage and nominal temperature operating conditions, for static and dynamic operation. The operation of the device under test shall be monitored for memory cell upset, I/O upset defined as a voltage excursion > Vdd/3
(3) Testing shall be done IAW MIL-T1019.7 using a Cobalt-60 source at a 50 to 300 rd(Si)/s dose-rate
(4) 1-error/device-mission (mission = 10 years); would require intervention of hard reset or power cycling
(5) 1-error/device-year; taken care of through an autonomous circuit such as a watch-dog-timer

RHBD Program Vision

Enable Rad-Hard ASICs on advanced commercial fabrication processes

- High performance, low power devices
- Leverage existing foundry capabilities
  - IBM 9SF 90 nm CMOS
- Reduces the space electronics lag



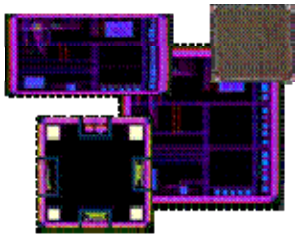
Hardness Goals	
Total Ionizing Dose	> 2 Mrad(Si) (OPERA > 500 Krad (Si))
Single Event Upset	< 1E-10 errors/bit-day (Adams), LET_{Th} > 20
Single Event Latchup	LET_{TH} > 120 Mev-cm^2/mg
Dose-Rate Upset	>1E10 rad(SiO_2)/sec

Acceptable RHBD Penalties	
Area	≤ 2X
Speed	≤ 1.5X
Power	≤ 2X

RHBD Design Enablement

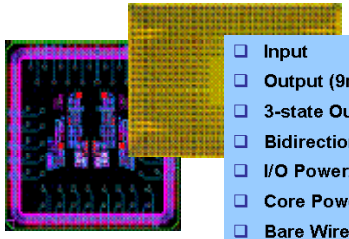
Standard Cell Libraries

- 1014 Cells
- Low Power & High Speed Variants



I/O Libraries

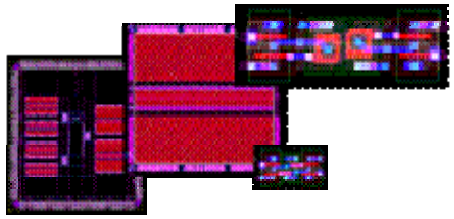
- 500MHz LVDS
- C4
- Wirebond
- 2.5V, 3.3V tolerant



- Input
- Output (9mA, 18mA)
- 3-state Output
- Bidirectional
- I/O Power/Ground
- Core Power/Ground
- Bare Wire (No ESD)
- Analog (ESD only)
- Corner

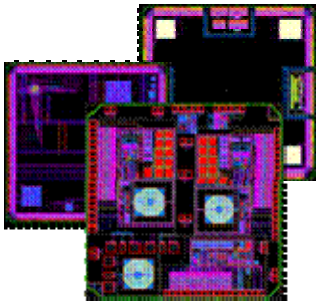
SRAM

- 1Mrad
- 500Krad
- 6 Types
- Generator in work



PLL

- Clock
- SERDES
- DDR2

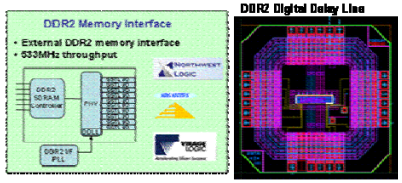


ASIC Design Flow

Development Step	Data included
Synthesis	• Liberty Format Files (.lib) • Synopsys Data Base Files (.db)
Simulation	• Verilog simulation models • VHDL VITAL simulation models • Cadence schematics
Placement & Routing	• Cell physical geometry • Cell frame views • Cell timing views • Cell power views • Technology file
Verification	• Cell SPICE netlist • Verification decks version
Support data	• Cell datasheets • Models & Design rules version

DDR 1 & 2 Interface

- High bandwidth external storage interface



SERDES

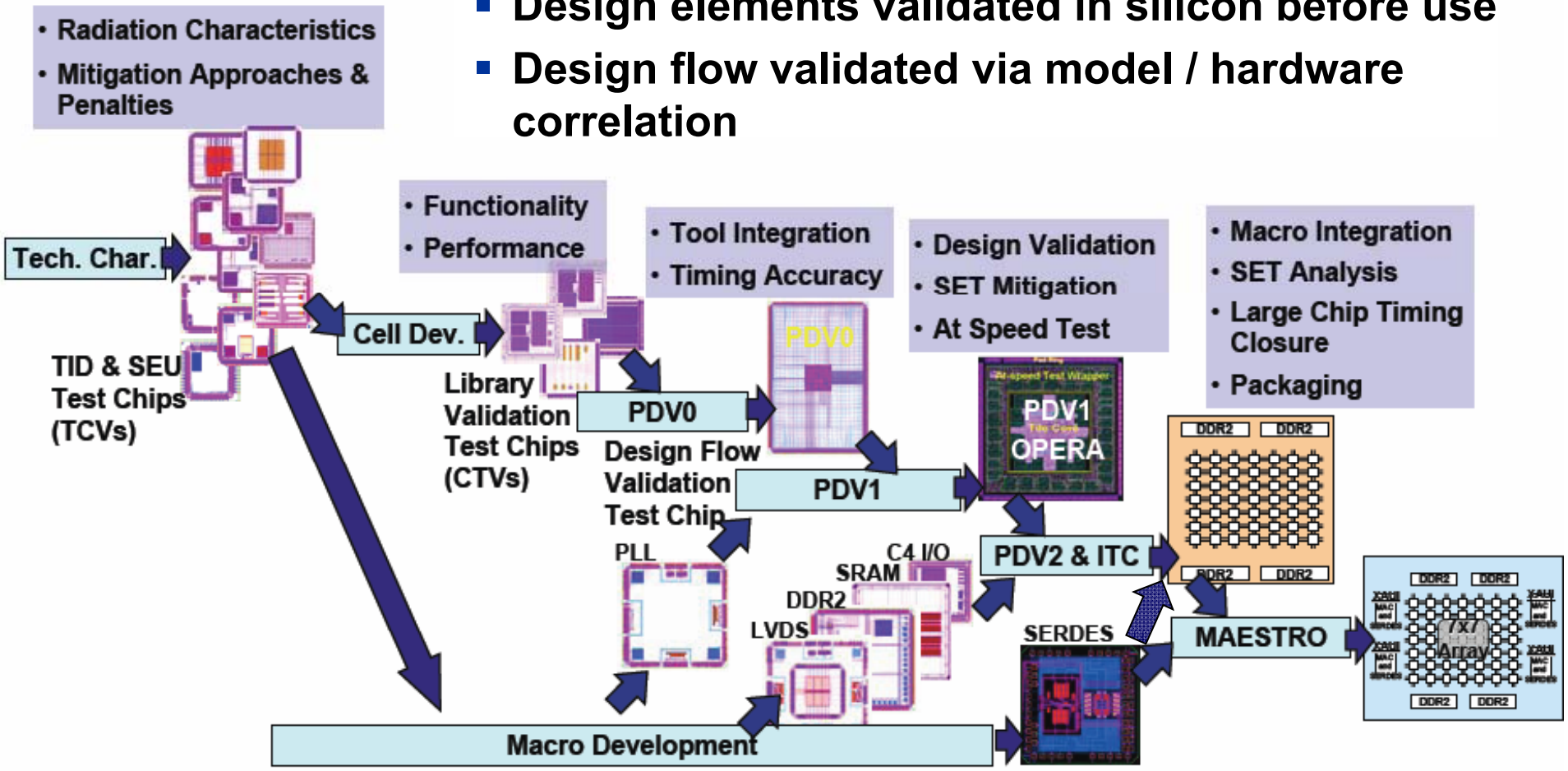
- 10Gbit/sec Ethernet
- Supports XAUI & PCI Express

Maestro Radiation Mitigation

Radiation Effect	Affects	Where used	Mitigation
TID	Thick oxide devices	I/O Circuitry	▪ Annular devices
	Thin oxide devices	All logic cells	▪ Balanced drive strength
SEL	All devices	All blocks	▪ Extensive use of substrate and well contacts
SEU	SRAM cells	Memory caches	▪ Bit-level, word-level, and instance level interleaving ▪ Error Detection and Correction (EDAC) ▪ Scrubbing
	Flip-Flops	Logic blocks	▪ Dual Interlocked Storage Cells (DICE) flip-flops
SET	Logic cells	Control and data paths	▪ Balance drive strength ▪ Pulse width filtering: temporal filters in the data/scan inputs
		Clock gating cells	▪ Balance drive strength ▪ Pulse width filtering: temporal filters in the data/scan and clock inputs
SET	Digital logic cells	Clock and reset distribution	▪ Single-stage high drive strength buffers ▪ Balanced drive strength
		Macros: PLL, SerDes	▪ High drive strength devices ▪ Balanced drive strength
	Analog logic cells	Macros: PLL, SerDes	▪ RC filtering in analog nodes ▪ Guard rings ▪ Increased bias current
Dose Rate Effects	All cells	All blocks	▪ Power rail sizing ▪ Balanced drive strength

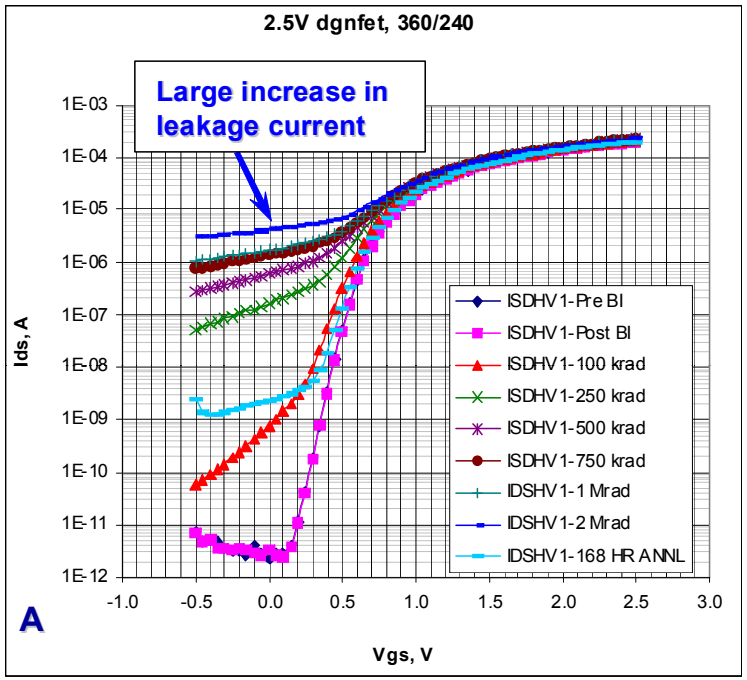
RHBD Risk Mitigation Approach

- Design elements validated in silicon before use
- Design flow validated via model / hardware correlation

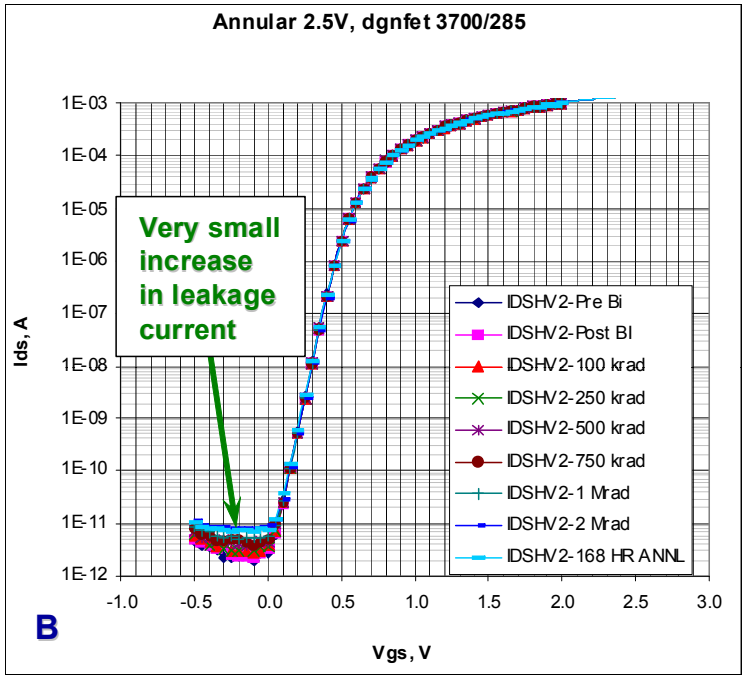


- PDV – Product Demonstration Vehicle
- ITC – Integrated Test Chip

RHBD Device Radiation Testing



Nominal Transistor Design

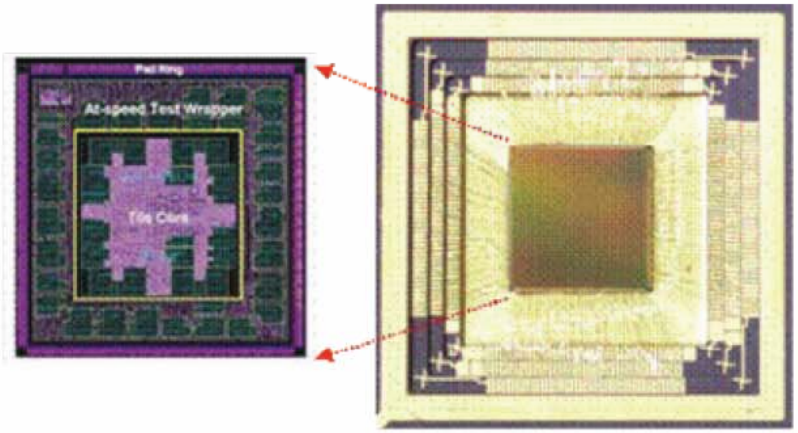


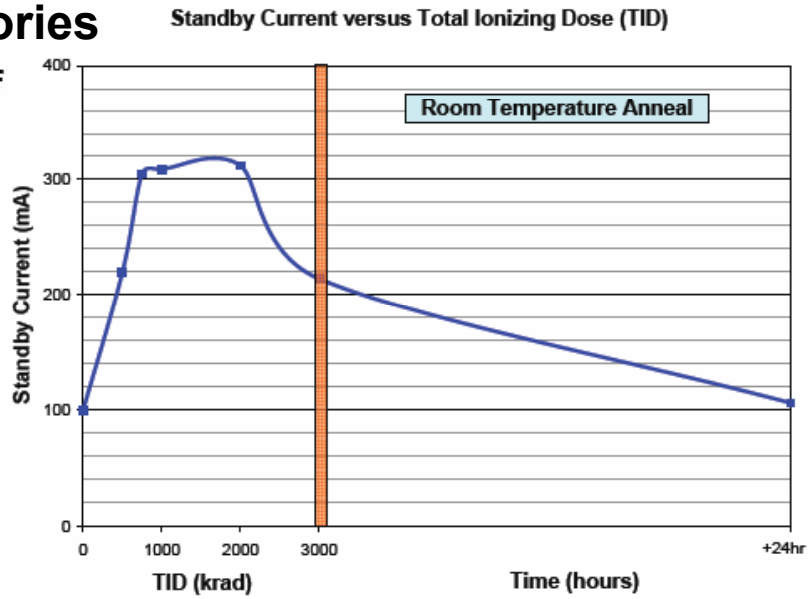
RHBD Transistor Design

- **Incorporating RHBD techniques as necessary, minimal device leakage can be ensured to 2 Mrad[Si]**

PDV1 (OPERA Tile) Radiation Test Results

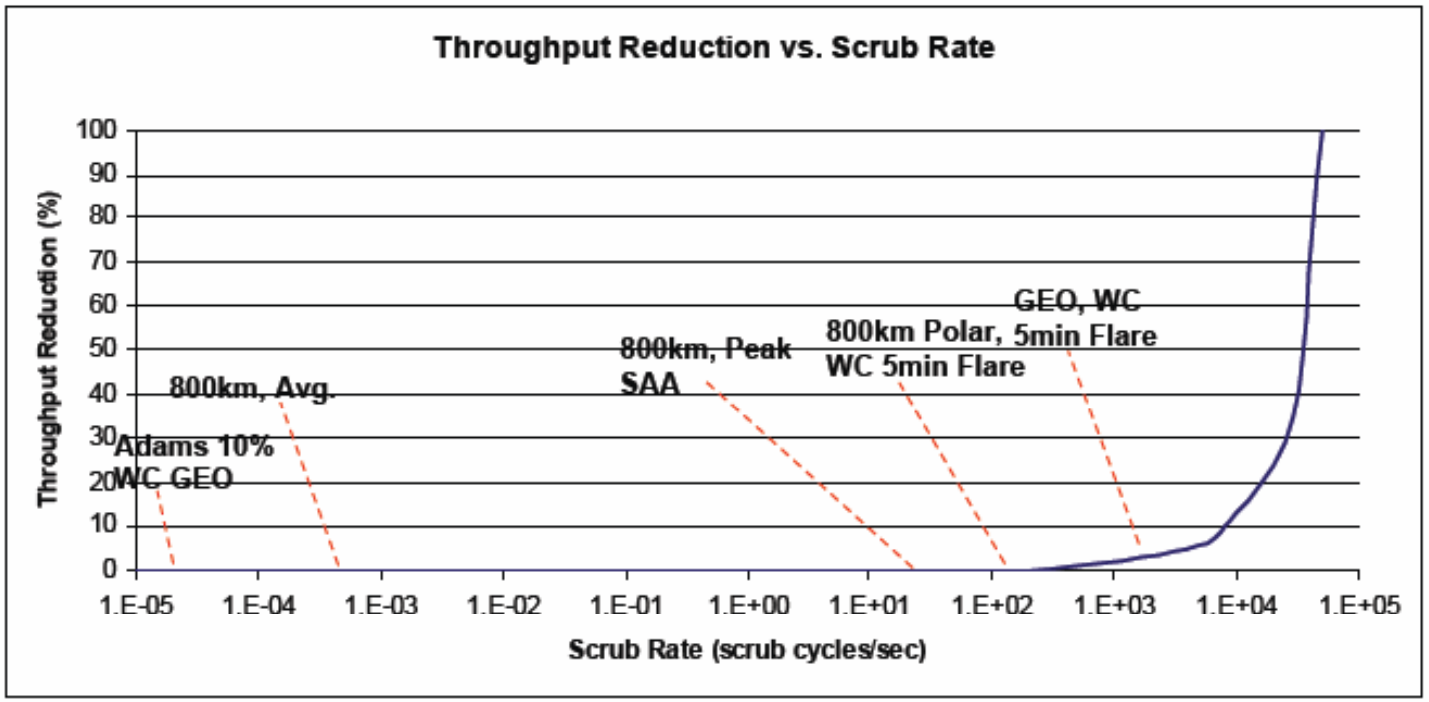
- At-speed test categorized SEU and SET effects
- Functional Testing
  - Passed the original Tilera tests
  - Passed all Memory Built-In-Self-Test (MBIST), scan, and Boeing at-speed tests
- Radiation Testing
  - Tile hard ≥ 2 Mrad TID with RHBD II memories
  - No Single Event Latchup (SEL) at an LET of 123 MeV-cm^2/mg
  - Successfully sorted SEE errors into categories:
    - No Destructive Errors
    - No Unrecoverable Errors
    - Recoverable Errors
    - Data Integrity Errors
  - Survived dose rate to 5E11





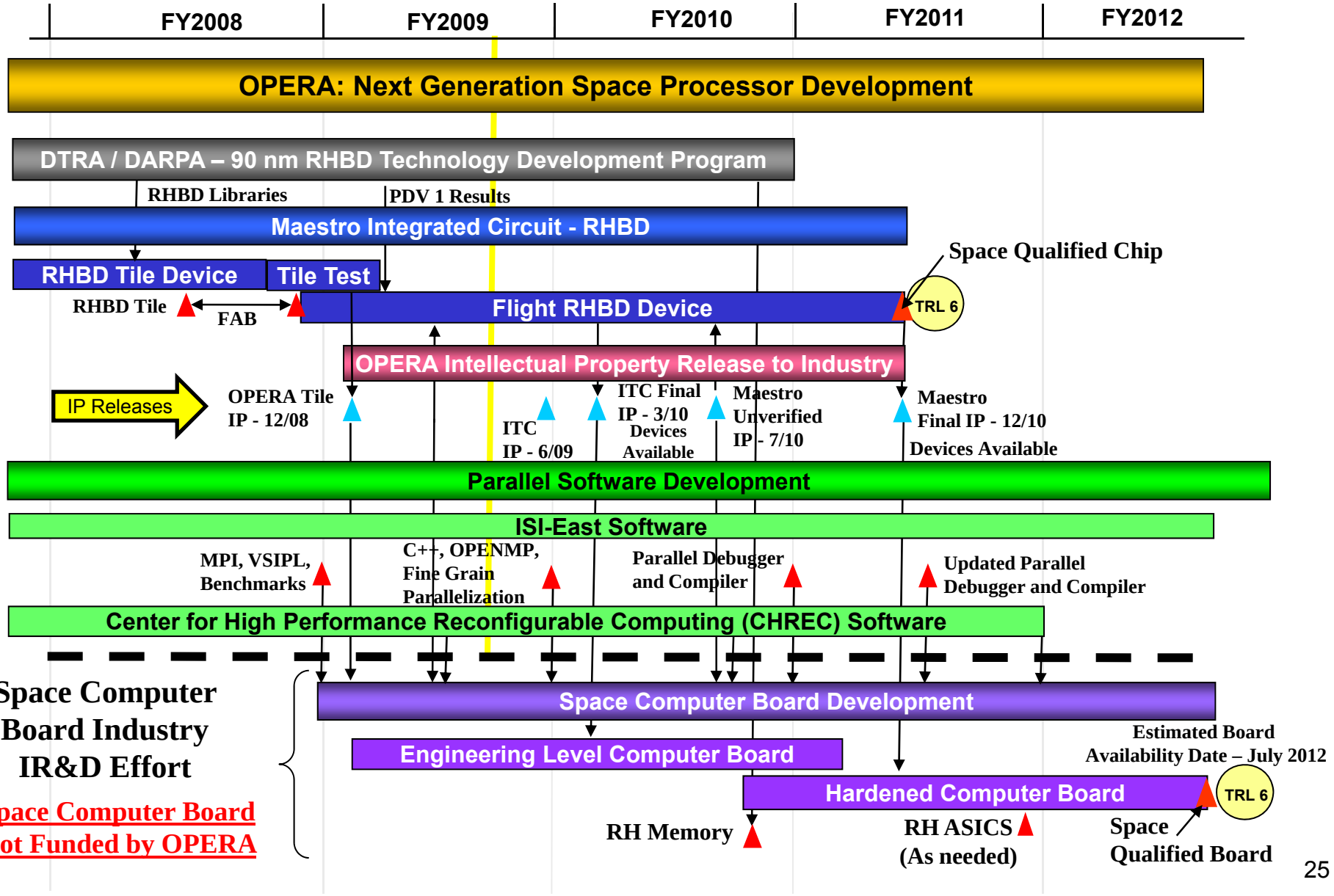
Memory Scrubbing Summary

- Maestro has built in single bit correct, double bit detect EDAC
- Memory scrubbing required to clear multiple bit errors



Scrubbing to achieve 2E-11 Errors/bit-day due to independent single errors has acceptable throughput impact in all environments

OPERA Program Roadmap



OPERA Summary

- **Multi-core processors offer improved performance per watt for most applications**
- **OPERA Integrated Test Chip on track for March, 2010 completion**
  - PDV1 radiation testing complete and meets requirements
  - ITC tapeout is currently scheduled for Q4, 2009
    - Tapeout date has slipped mainly due to memory timing model and design for test implementation issues
- **Maestro on track for December, 2010 completion (TRL 6)**
  - 2nd pass device if required
- **RHBD is a viable alternative to radiation hardened by process devices for select designs**
- **OPERA IP available for interested contractors / agencies working on US space-based applications**