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Aerospace Data Storage and Processing Systems

Memory Technology for Space

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Seminar Day
Military and Aerospace Programmable Logic Devices (MAPLD)
NASA Goddard Space Flight Center
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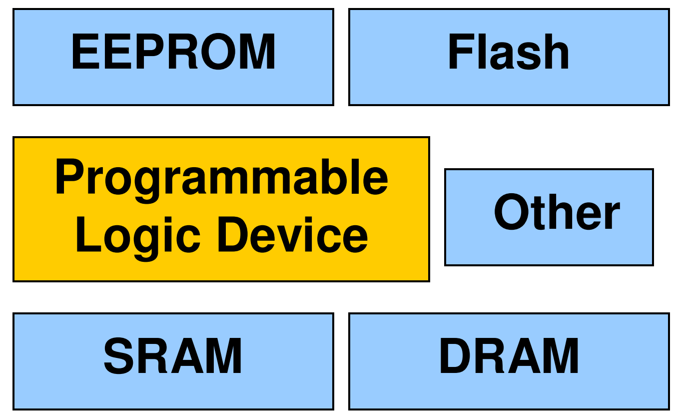
Motivation

- When considering PLD performance, peripheral devices must be included
- After the processor, memory is often *the* device limiting space system capability

c/o Flickr

Overview

- **Memory types covered**
  - **Non-volatile**
    - **EEPROM**
    - **Flash**
    - **Other**
  - **Volatile**
    - **SRAM**
    - **DRAM**



- **Other special types are used as well**
- **All results from the open literature and “ITAR safe”**
- **Internal PLD memory not included in this discussion**

Memory Specialization

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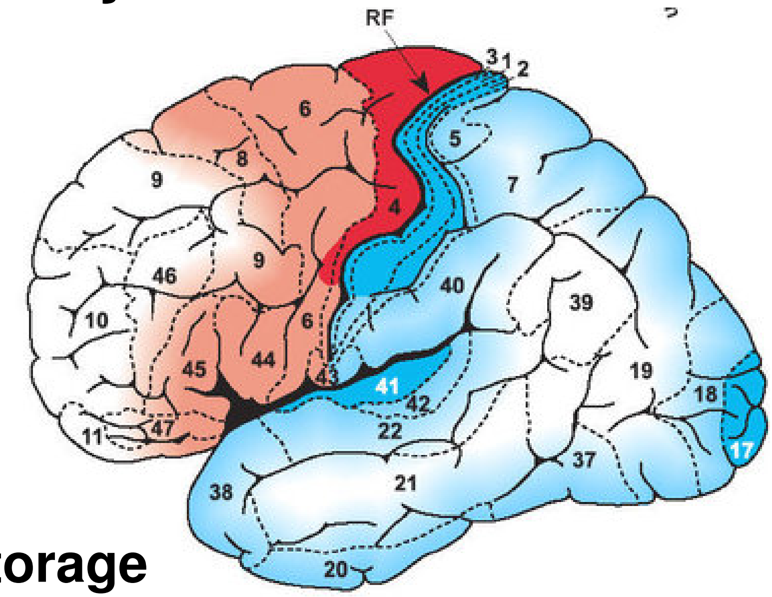
- Specialization seen in commercial systems also prevalent in space systems

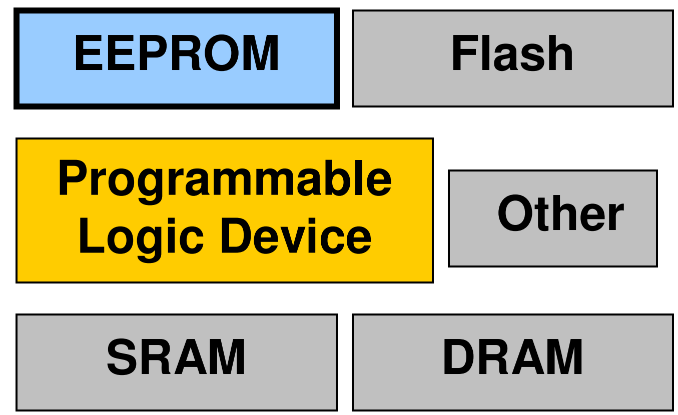


c/o Scholarpedia.com

- Non-volatile memory
  - Persistent values, also…
  - Greater capacity
  - Lower power dissipation
  - Slower access times, throughput
  - Apps: start-up memory, persistent storage
- Volatile memory
  - Values are not persistent, also …
  - Decreased capacity
  - Increased power dissipation
  - Fast access times, throughput
  - Apps: run-time memory, buffering

Non-volatile: EEPROM

- Electrically Erasable Programmable Read-Only Memory
- Typically used to store small amounts of data for startup
  - Device configuration
  - Calibration tables
  - Boot code
  - Debug information
- Typical device capabilities include*
  - 32Kb to 256Kb options
  - ~1,000,000 rewrite cycles
  - ~10-year data retention or more
  - 10K to 1M rad TID tolerance
- Options: Actel, Aeroflex, Atmel, Hitachi, Infineon, Maxwell, Samsung, etc.



***Data taken from open literature and company websites**

EEPROM Structure

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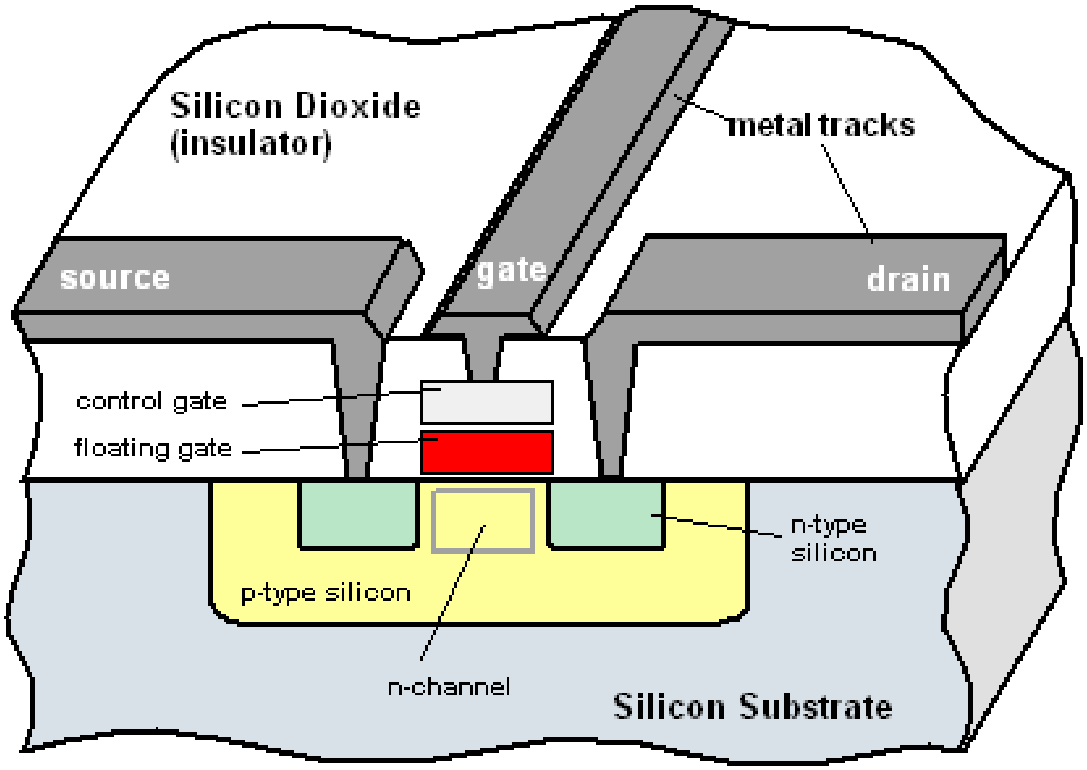
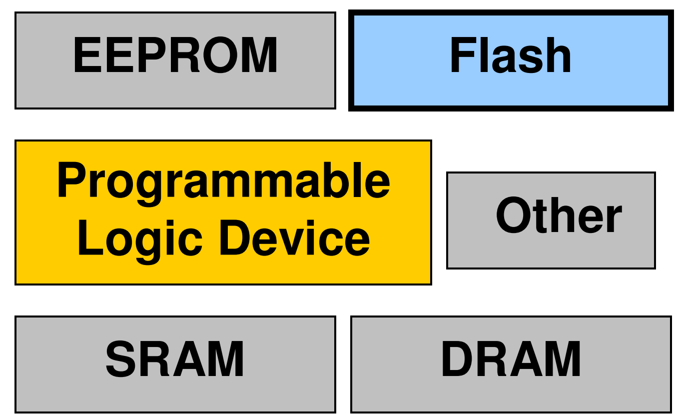


c/o The Computer Language Company

- **Arrays of floating gate transistors provide data persistence and relatively strong TID and SEE performance**
- **Control circuitry, especially charge pumps, susceptible**

Non Volatile: Flash

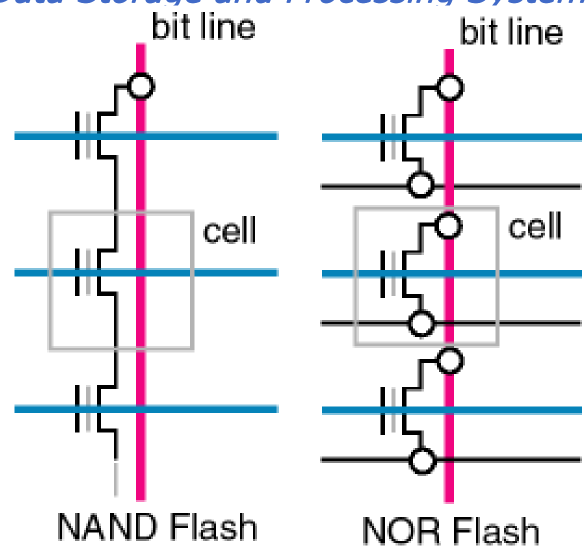
- Special type of EEPROM that offers fast erase
- NAND and NOR varieties
- Typically used to store large amounts of data for startup
  - Device configuration
  - Calibration tables
  - Boot code
  - Debug information
- Typical device capabilities include*
  - 256Mb to 8Gb options typical
  - ~5,000 to ~500,000 rewrite cycles
  - ~20-year data retention or more
  - 5K to hundreds of K rad TID tolerance typical (ELDRS effects)
- Options: Hynix, Intel, Micron, Samsung, Spansion, etc.
- Xilinx offers flash-based configuration memory as well



*Data taken from open literature and company websites

Flash Structure

- Arrays of floating gate transistors
- Different interfaces used in two options
  - NOR: random-access, NAND: page access
- NOR optimized for speed
  - Ideal for lower-density, high-speed read applications such as code-boot
- NAND optimized for small cell size
  - Random access traded for lower cost-per-bit and faster write/erase via block operations
  - Ideal for high-density, high-speed program and erase applications, i.e. data-storage
- Market driven by NAND applications
  - USB drives and iPhone/iPod
  - We are “safe” as long as interests overlap



c/o Eureka Technology


c/o mediahaven.com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NOR versus NAND Flash

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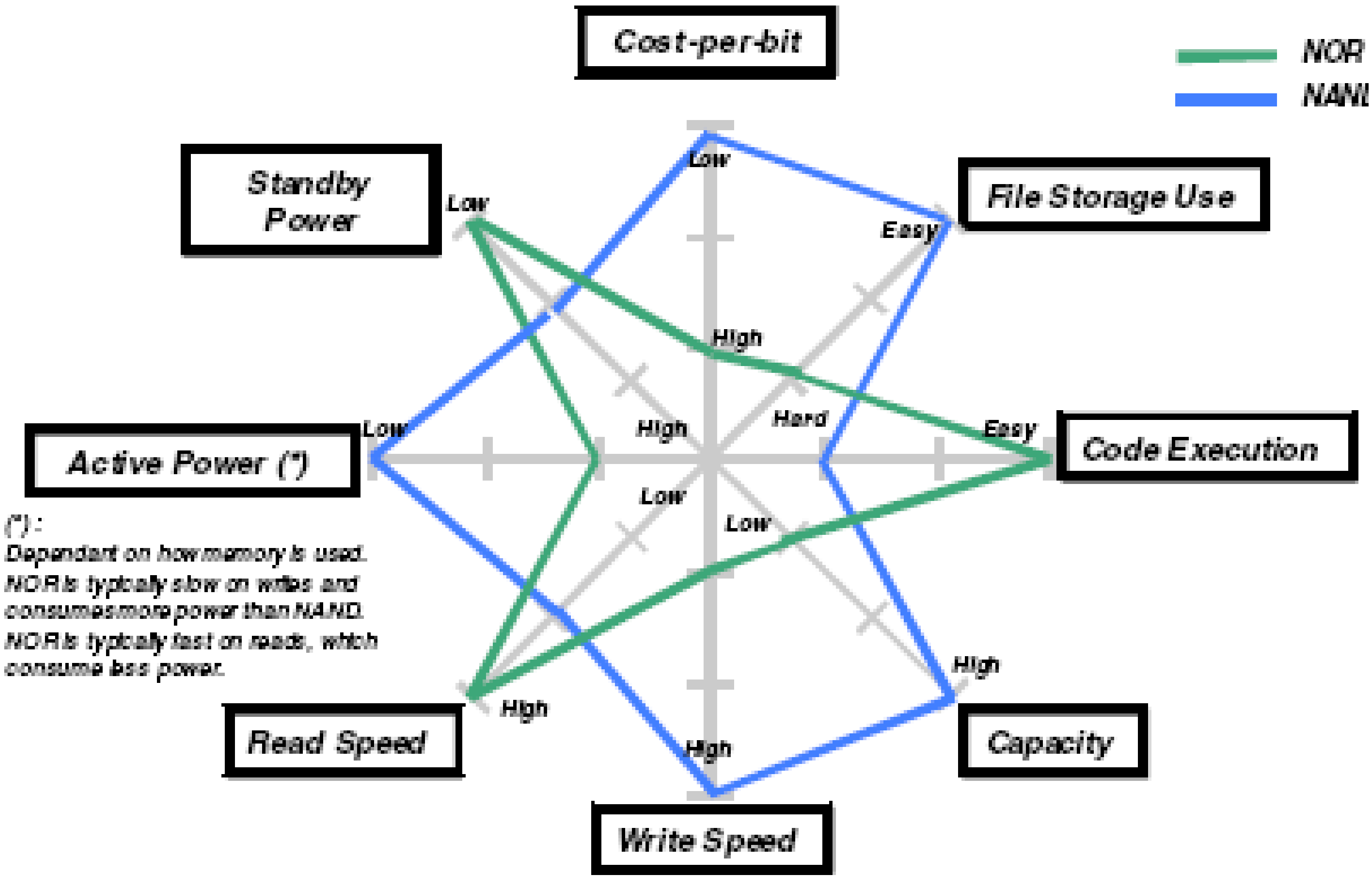


c/o Toshiba [2]

Flash Radiation Performance

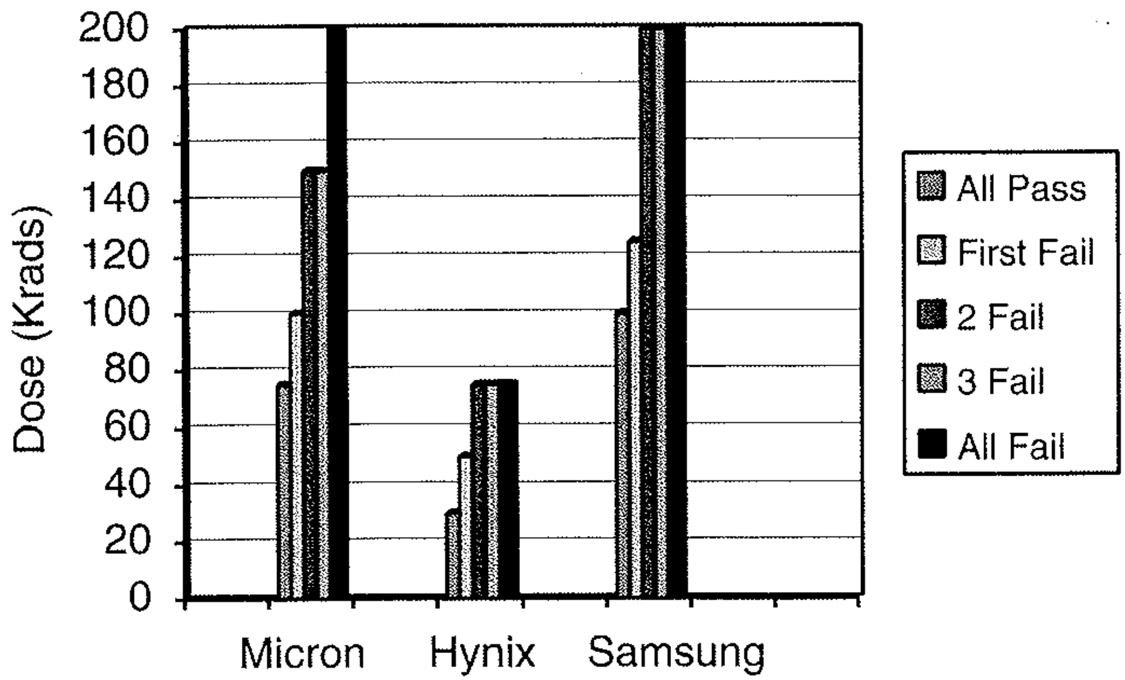
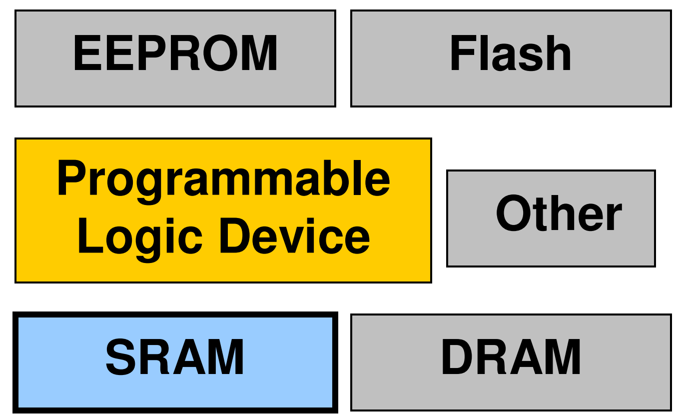


Fig 1. TID response for Micron, Hynix, and Samsung 4G NAND flash memories. ***c/o IEEE and Oldham et al. [3]***

- **Results reprinted from Oldham et al. [3] (NASA-NEPP/DTRA flash study)**
- **Static read results shown, other dynamic tests – devices up to 700Krad**
- **TID performance improving, due smaller feature size reduction “tricks”**
- **SEE affected by Multi-level Cell (MLC) trend and feature size reduction**

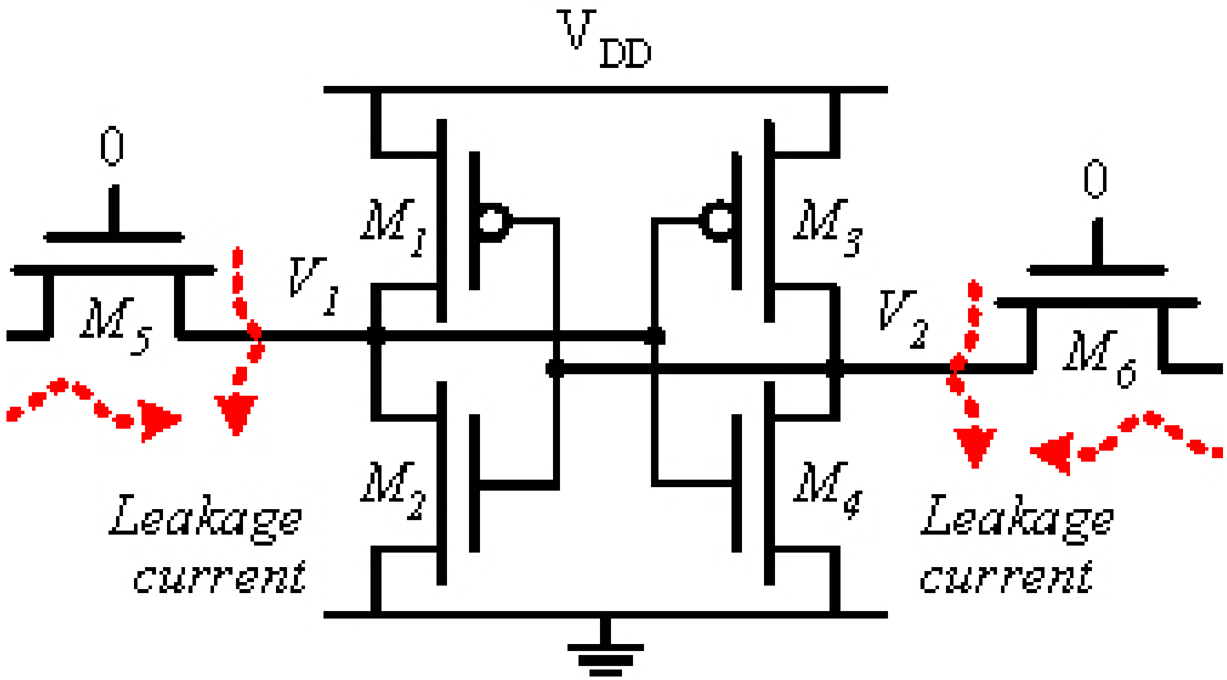
Volatile: SRAM

- Static Random Access Memory
- Typically used for control processing applications
  - Buffer between cache and storage
  - Processor's "main memory"
- Typical device capabilities include*
  - 4Mb to 64Mb options typical
  - "infinite" rewrite cycles
  - No data retention
  - 100K to 1M rad TID tolerance typical
  - ~10ns access latency typical
- Options: Aeroflex, BAE, Honeywell, Maxwell, Samsung, etc.



Data taken from open literature and company websites

SRAM Structure

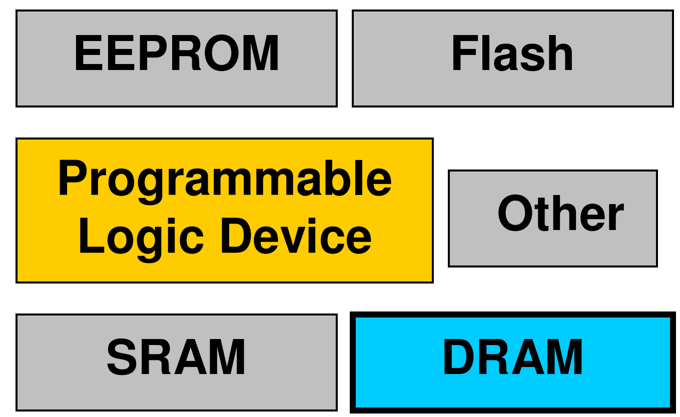


c/o Huifang Qin at UC Berkeley (lab web page)

- Cell uses bi-stable latching circuitry for bit storage
- Variations of the 6T cross-coupled inverters with buffers
- Self-reinforcing nature improves SEE performance
- SEFI modes not as varied and often not as complex

Volatile: DRAM

- **Dynamic Random Access Memory**
  - **Synchronous (S), Double Data Rate (DDR) options typical**
  - **e.g. DDR2 SDRAM**
- **Typically used to data processing applications**
  - **Buffer between cache and storage**
  - **Processor's "main memory"**
- **Typical device capabilities include***
  - **2Gb to 8Gb options typical**
  - **"infinite" rewrite cycles**
  - **No data retention**
  - **Variable TID tolerance**
  - **~50ns access latency typical**
- **Options: Hyundai, Micron, Samsung, etc. (commercial)**



****Data taken from open literature and company websites***

DRAM Structure

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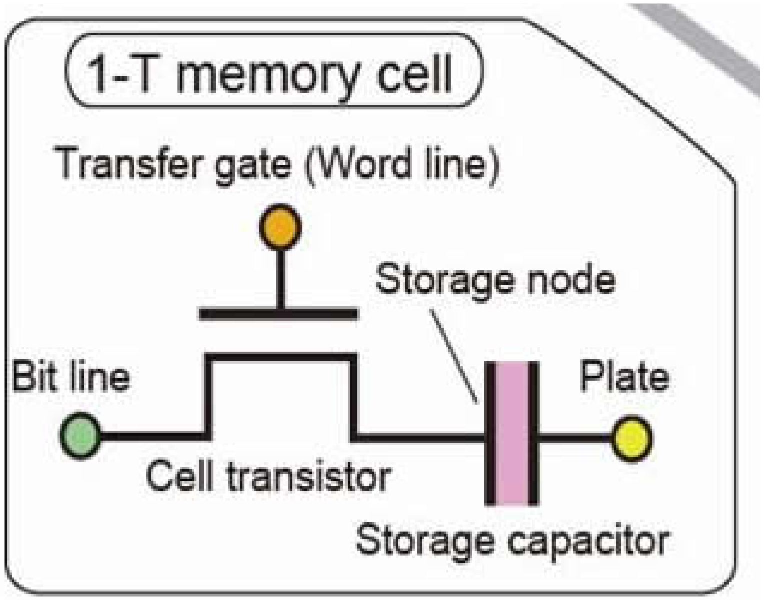
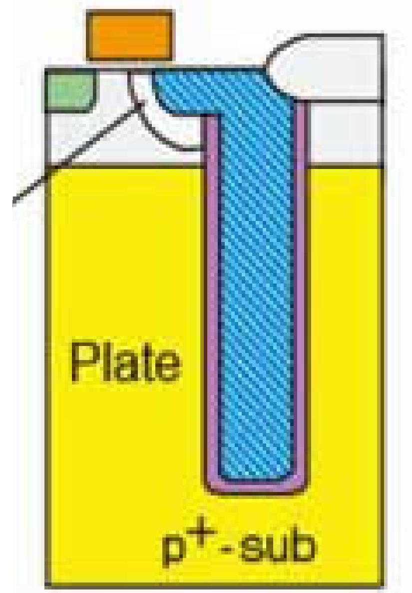


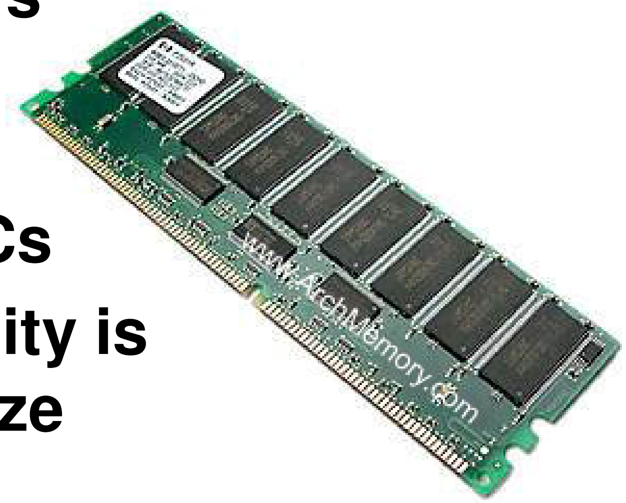


c/o IEEE.org

- **Cell uses pass transistor and capacitor for bit storage**
- **Density greatly improved over SRAM**
- **Constant updates required to keep cell charges**
- **Complex addressing and refresh modes increase SEFIs**

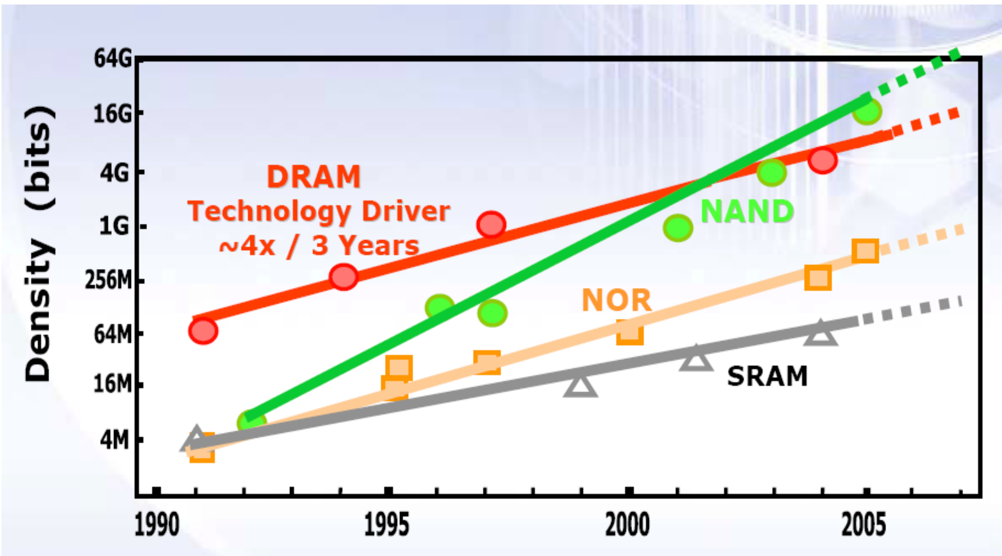
DRAM versus SRAM

- Density, cost, latency, power are drivers
  - DRAM: greater density and reduced $ per bit
  - SRAM: reduced latency, power and density
- Primary market driver is commodity PCs
- DRAM is typically preferred when density is the primary consideration (e.g. when size and weight are important) and SRAM is preferred when reducing data access latency is the primary concern
- The advent of synchronous and double data rate options have improved DRAM performance but has increased device access complexity and SEFI and SET effects

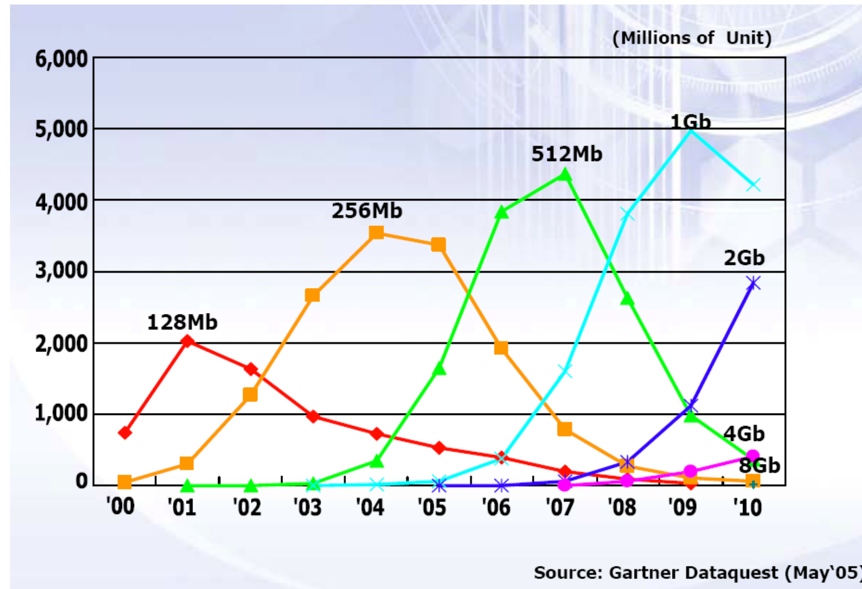


c/o ArchMemory.com

DRAM Trends



c/o Samsung

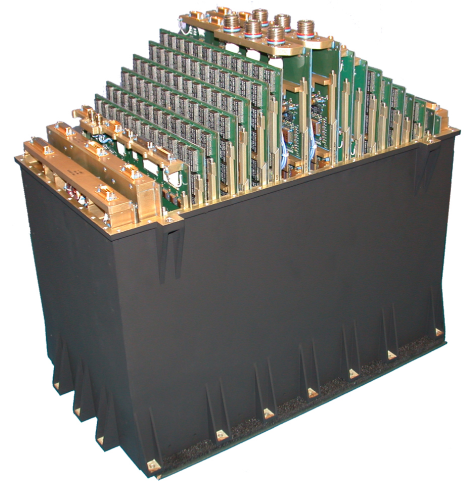


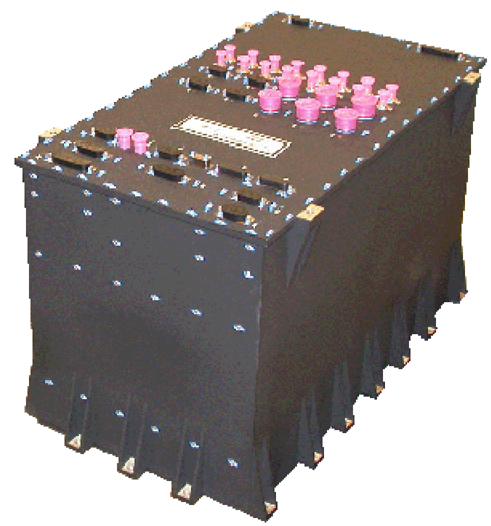
c/o Samsung

- Technology trends continue to provide higher density components
- Processing node scaling tends to improve TID but worsen SEE
- Obsolesce a key concern for aerospace systems
- Die revision changes within each family of devices another concern

Commercial DRAM in Space

- Commercial densities, performance and cost far outpacing rad-hard technologies and are being leveraged to produce increasingly capable systems
- For example, SDRAM used on SEAKR SSR with 2Tb capacity for a commercial imaging space system due to capture, compress and downlink data at rates up to 4Gbps
  - No other memory option could meet requirements
- Radiation effects such as TID and SEE need to be characterized and mitigated in systems using COTS memory for space
  - Telling that efforts to mitigate these effects more cost-effective than rad-hard for these missions





DRAM On-orbit Analysis

- While densities above 2Gb are now available in commercial components, lower density parts have been in orbit long enough to gather statistically significant data
- Recent study examined 64Mb, 128Mb, and 256Mb DRAM upset rates and compares them to predictions made using CREME96 (using actual space weather)
- On-orbit data collected from commercial DRAM parts used in SSRs designed and built by SEAKR Engineering was included in the study
- Study results presented at IEEE Aerospace Conference in March of 2009 [4]

DRAM Devices Studied

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- **Samsung 64Mb KM44V16004 FPM CMOS DRAM**
  - Fast Page Mode (FPM) offers high speed random access of memory cells within the same row
  - Revisions A, B, and D of this part used in the analyzed systems
  - Rev. A has a 0.32 μm minimum feature size
  - Rev. B & D have a 0.28 μm minimum feature size
- **Samsung 128Mb KM44S32030 SDRAM**
  - Four die per package with a bit width of four
  - Rev. B has a 0.20 μm minimum feature size
- **Hitachi 256Mb HM5225405B SDRAM**
  - Four die per package with a bit width of four
  - This component has a 0.16 μm minimum feature size

On-orbit DRAM Data

Density	Parts	Bits	Device hours
64 Mb	1155	74 Gb	4.9E7
128 Mb	1978	253 Gb	1.1E8
256 Mb	720	180 Gb	2.0E7
Totals	**3853**	**507 Gb**	**1.8E8**

- Due to the large number of parts and distribution of varieties, this study believed to compile the most comprehensive on-orbit datasets of high density DRAM available

SSR Mission Descriptions

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Memory Size	Manufacturer	Description	Program
64Mb	Samsung	16Mx4, 60nS, rev A	II,III,IV
64Mb	Samsung	16Mx4, 60nS, rev B	IV
64Mb	Samsung	16Mx4, 60nS, rev D	I
128Mb	Samsung	32Mx4, Synchronous, rev B	IV
256 Mb	Hitachi	64Mx4, Synchronous, 75ns	MRO

- Missions I, II and III were various LEO orbits
- Mission IV was in the ISS orbit
- Data from the NASA's Mars Reconnaissance Orbiter (MRO) included as well

Mission I Orbit

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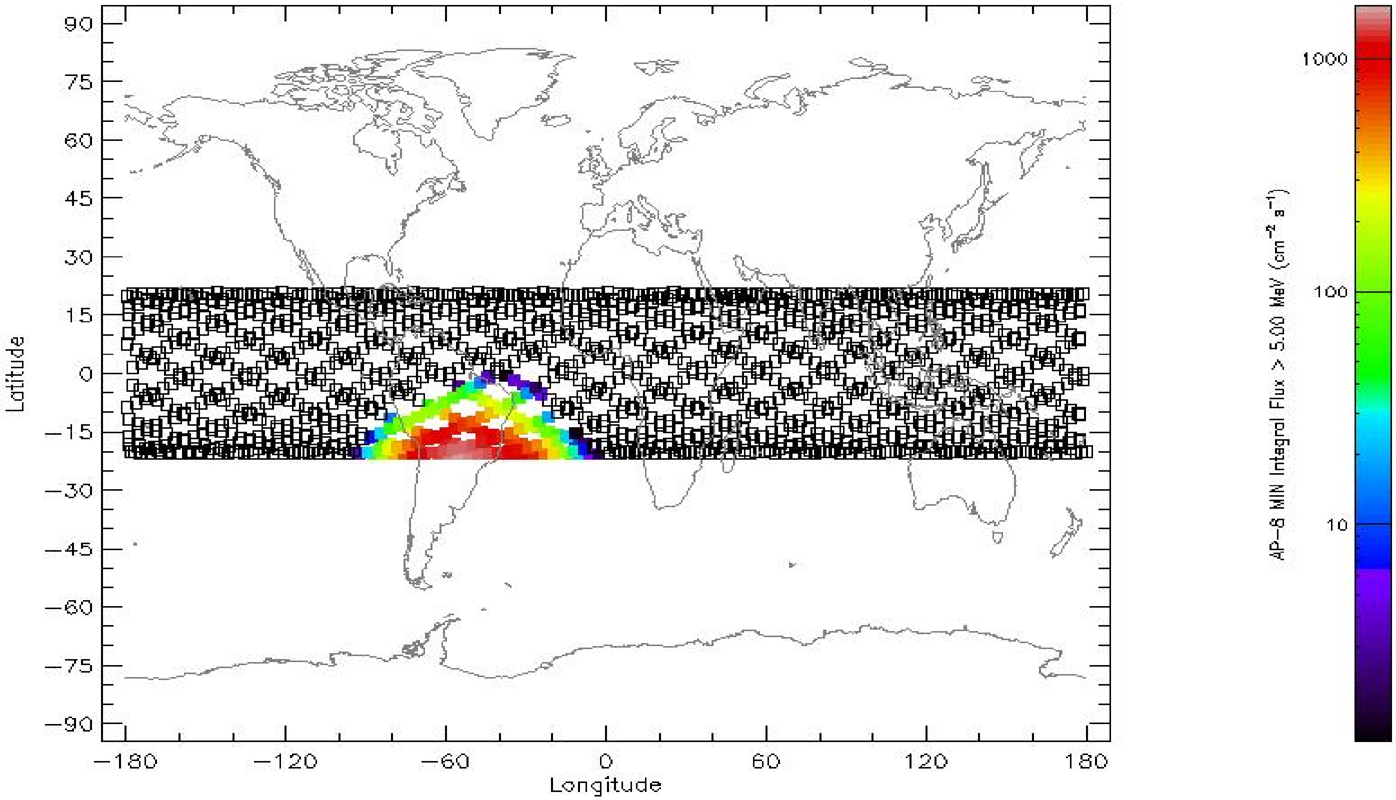

- Trapped protons along the orbit of Mission I showing multiple transits through the SAA
- Plot generated with SPENVIS

Mission II Results

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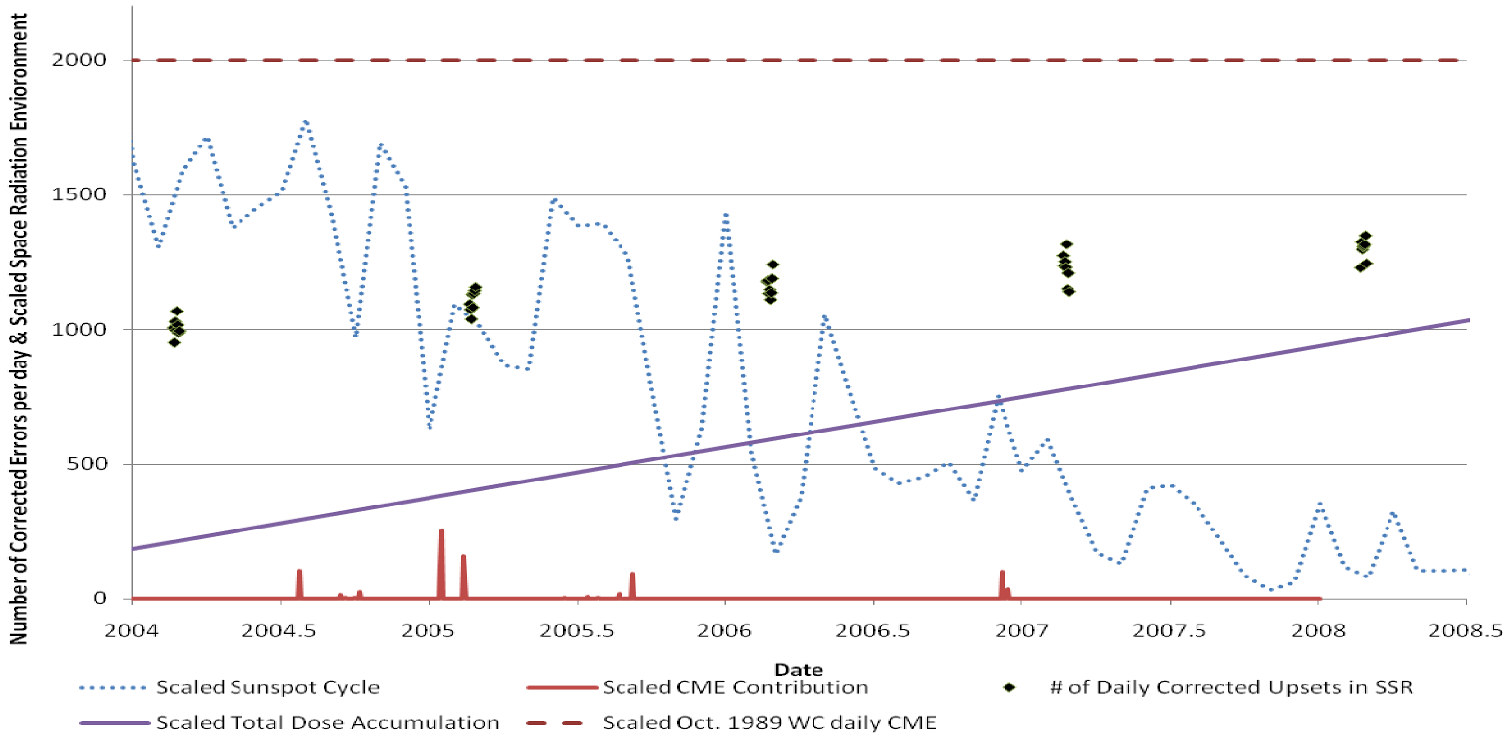
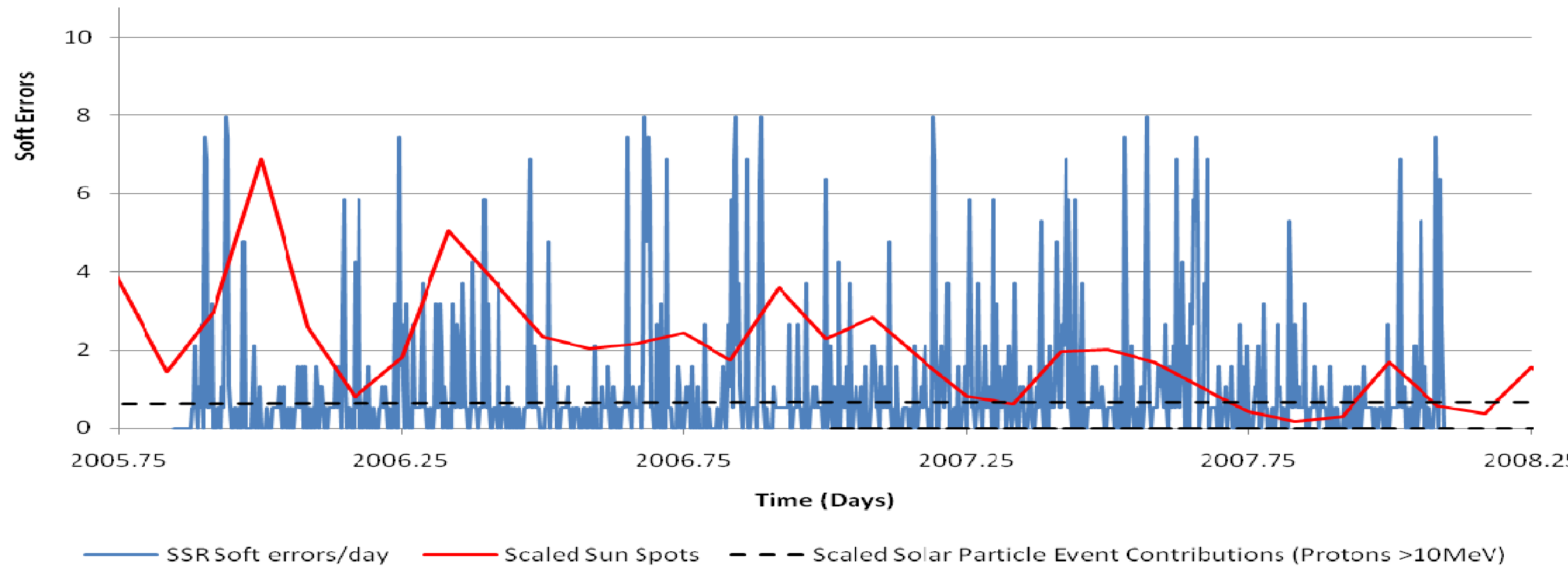


- Plot of several annual samples of daily upset data
- Scaled version of the sunspot cycle, relevant CMEs, and scaled accumulated TID overlaid
- Potential contributions to the linearly increasing number of upsets (all corrected by EDAC)

MRO Analysis Results



- **SSR errors (all corrected by EDAC) have been plotted against the scaled sun spot data and CME data**
  - **No notable CME contributions and no substantial correlation between sunspots and errors**
  - **Errors occasionally correspond to periods of increased sunspot activity but no direct correlation**

Tool Assumptions

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Program	Memory	GCR HI	GCR P	SEP HI	SEP P	AVG. TRP P
I	Samsung 64Mb	99.98%	99.98%	0.02%	0.02%	100.00%
II	Samsung 64Mb	99.91%	99.91%	0.09%	0.09%	100.00%
III	Samsung 64Mb	99.99%	99.99%	0.01%	0.01%	100.00%
IV	Samsung 128Mb	99.94%	99.94%	0.06%	0.06%	100.00%
V	Hitachi 256Mb	99.99%	99.99%	0.01%	0.01%	0.00%

Percentage of actual space environment contribution to upset rate in CREME96

Study Results

Program	Memory Type	On Orbit Upsets (Correctable Errors) per bit-day	Predicted CREME96 Upset Rate per bit-day	Ratio of Predicted CREME96 to On Orbit Upsets	Shielding Assumption (mils Al)	Orbit
I	Samsung 64 Mb	1.55E-9	1.58E-8	10.20	150	LEO
II	Samsung 64 Mb	4.44E-8	5.60E-8	1.26	150	LEO
III	Samsung 64 Mb	2.93-8	3.15E-8	1.08	125	LEO
IV	Samsung 128 Mb	2.15E-10	1.23E-9	5.72	150	ISS
MRO	Hitachi 256 Mb	1.02E-11	6.29E-11	6.16	150	Mars

- Historical data for space weather which occurred during the missions used for the comparison
- Analysis assumed sensitive volume depth of 0.5µm

Tool Conservatism

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Mils Aluminum	Program I	Program II	Program III
150	10.20	1.26	1.05
200	9.85	1.20	1.01
300	9.37	1.13	0.95

- **Ratio of CREME96 predicted to actual upsets as a function of shielding thickness explored**
  - **Other thicknesses explored ranging from 150 mils to 300 mils**
  - **Less than a 17% change was observed in the predicted upset rate**
  - **Increased shielding leads to rates slightly closer to on-orbit rates**
- **Sensitive volume (SV) assumptions also explored**
  - **SV effects for Earth-orbiting spacecraft at LEO negligible compared to the trapped proton contributions**
- **Minor difference between observed and predicted upsets indicates models relatively accurate in predictions**
- **Ongoing research to explore additional possibilities**
- **No one size fits all for guessing tool conservatism**

Summary of Characteristics

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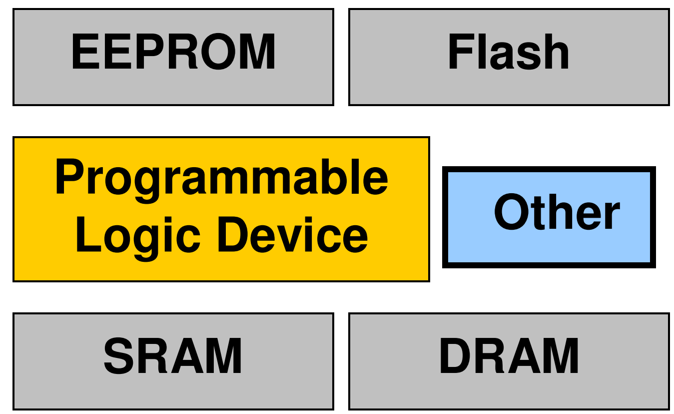
Type	Volatile	Read Latency	Write Latency	Lifespan	Power Usage	Capacity	TID
EEPROM	NV	~200ns	~3ms	~1e6	Low	Low	High
Flash	NV	~70ns	~500ms	~1e5	Low	High	Low
SRAM	V	~10ns	~10ns	Infinite	Medium	Low	High
DRAM	V	~50ns	~50ns	Infinite	High	Medium	Medium

- Volatile memory provides advantages of reduced access latency and extended device life spans but at the cost of power and data volatility
- Non-volatile memory has opposite characteristics
- Flash and DRAM principally from commercial market

Other Memory Types

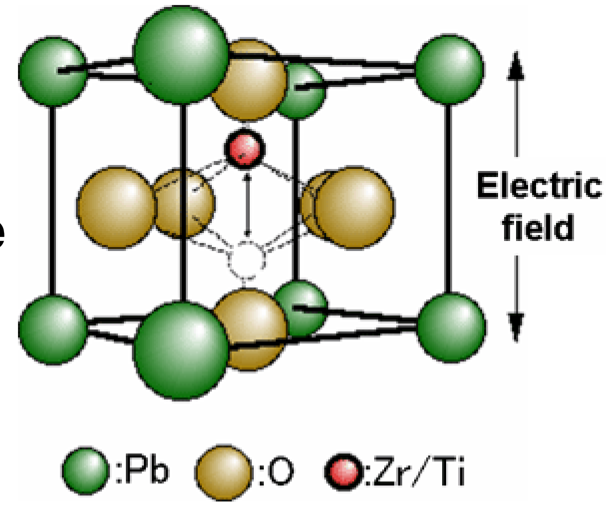
- Efforts underway to develop an alternative means of storage than the tried and true electrons and charge
- Developers seeking to create a “universal memory”
  - Non volatile with good density and fast access
- Promising options include
  - Ferroelectric RAM
  - Magnetoresistive RAM
  - Chalcogenide RAM



- Memory with other types of applications are also being explored for space systems

FRAM Structure

- Ferroelectric Random Access Memory
  - Ferroelectric film (capacitor) for storing data
  - Electric polarization of atom determines value
  - Low power required to change value
    - No charge pump required
  - No charge required to maintain persistence



c/o Fujitsu

- Characteristics
  - Non-volatile memory with high endurance
  - High-speed access, low power consumption
  - Characteristics split the difference between RAM and ROM
  - Marketed for smart cards and hand-held devices
- Options: Fujitsu, Ramtron (under development)

MRAM Structure

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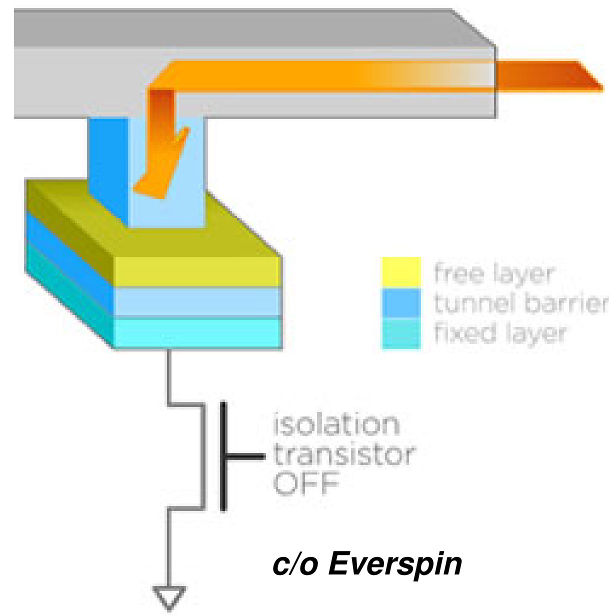
- **Magnetoresistive Random Access Memory**
  - **Magnetic Tunnel Junction (MTJ) stores data**
  - **Magnetic polarization determines electric resistance which is sensed to read value**
  - **Low power required to change value**
    - **No charge pump required**
  - **No charge required to maintain persistence**



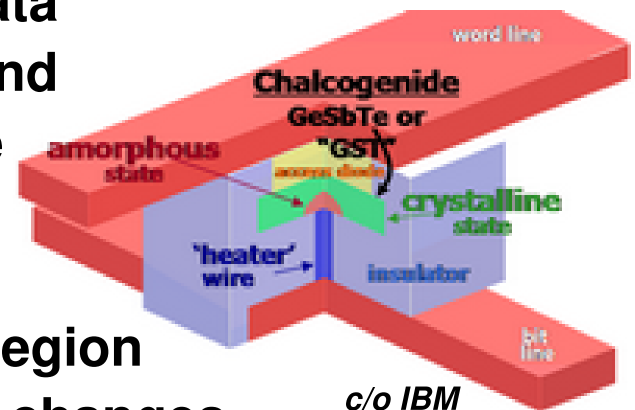
c/o Everspin

- **Characteristics**
  - **Non-volatile memory with high endurance**
  - **High-speed access, low power consumption**
  - **Characteristics split the difference between RAM and ROM**
  - **Strong commercial support to create the "universal memory"**
- **Options: Everspin, Hitachi, IBM, NEC, Toshiba**

C-RAM Structure

❑ Chalcogenide Random Access Memory

- Heat applied to Chalcogenide glass stores data
- Crystalline and amorphous states possible and resistance change is sensed to read value
  - Optical properties of material used in CD/DVDs
- No charge required to maintain persistence
- High programming current density in active region
- Temperature sensitivity may require process changes
- Also known as Phase-change memory



c/o IBM

❑ Characteristics

- Non-volatile memory with high endurance
- High-speed access, low power consumption
- Characteristics split the difference between RAM and ROM

❑ Options: BAE, Hitachi, IBM, Intel, Samsung, etc.

- BAE: 4Mb, TID to 1 Mrad with 70ns read and 500ns write latency

Conclusions

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- Four standard memory types examined and contrasted
- DRAM study of on-orbit SEAKR SSRs outlined
  - On-orbit upset data from 3853 COTS DRAM components
  - Included 64, 128, and 256Mb densities
  - Representing ~180 million on-orbit device hours
  - CREME96 predictions, using observed space weather, shown to be up to 10 times more conservative than observed upsets
  - No single attribution is clear in the analysis at present
- Alternative memory options examined
- Commercial devices currently provide improved performance per cost for space systems, even including radiation testing and mitigation
- Hopefully commercial trends continue in our favor

References

- [1] Gregory R. Allen, "Compendium of Test Results of Single Event Effects Conducted by the Jet Propulsion Laboratory," *Proc. IEEE Nuclear and Space Radiation Effects Conference (NSREC) Radiation Effects Data Workshop*, Tucson, AZ, July 14-18, 2008.
- [2] Toshiba, Inc., "NAND vs. NOR Flash Memory Technology Overview," Company Whitepaper, Irvine, CA, April 5, 2006.
- [3] T. Oldham, M. Suhail, M. Friendlich, et al., "TID and SEE Response of Advanced 4G NAND Flash Memories," *Proc. IEEE Nuclear and Space Radiation Effects Conference (NSREC) Radiation Effects Data Workshop*, Honolulu, HI, July 23-27, 2007.
- [4] Ian Troxel, Chris Miller, Russ Owen, et al., "Trends in Radiation Susceptibility of Commercial DRAMs for Space Systems," *Proc. IEEE Aerospace Conference*, Big Sky, MT, March 9-13, 2009.
- … and numerous vendor web sites

Contact Information

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