Hardware Implementation of a New Methodology for Reducing Sensor and Readout Electronic Circuitry Noise in Digital Domain

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Definition of Problem / Proposal

- Heritage methods of noise reduction using reference pixels, such as subtraction of global statistics, overlook fast-varying noise components present in the data.
- An improved method using the HHT-DPS tool, which breaks down vector functions into their data-derived basis functions, can help identify and eliminate this fast-varying noise using an algorithm based on the propagation of heat in a thermal model
- Programs were written in Matlab, testing the improved noise-reduction proposition on both simulated and actual sensor data.

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Definition of Problem / Proposal

- To achieve higher performance and bandwidth, we propose a hardware implementation of the algorithm.
- Comparison of DSP and FPGA implementation is looked at
- Design flow of an FPGA solution will be presented.

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Comparison Between DSP & FPGA Solution

DSP	FPGA
limited by fixed hardware architecture such as bus performance bottlenecks, a fixed number of multiply accumulate (MAC) blocks, fixed memory, fixed hardware accelerator blocks, and fixed data widths	DSP systems implemented in FPGAs can have customized architecture, customized bus structure, customized memory, customized hardware accelerator blocks, and a variable number of MAC blocks
Fixed performance based on clock frequency supported.	Performance could be much higher by configuring the number of DSP resources such as multiplier bandwidth
Performed well for algorithm that requires lots of branch on conditional statement.	With PSOC, embedded processor could be utilized to perform sophisticated branch on conditional statement

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Comparison Between DSP & FPGA Solution

DSP	FPGA
To increase performance, processor needs to run at higher frequency.	Algorithm can be profiled to determine the bottleneck and hardware implementation of the routine can be implemented to achieve higher performance
use external memory devices to manage large amounts of data processing	Embedded memory in FPGA eliminates the need for external memory devices in certain cases.
Have predefined hardware accelerator blocks	Configurable hardware accelerators for each application by using parameterized IP functions or from scratch using HDL.

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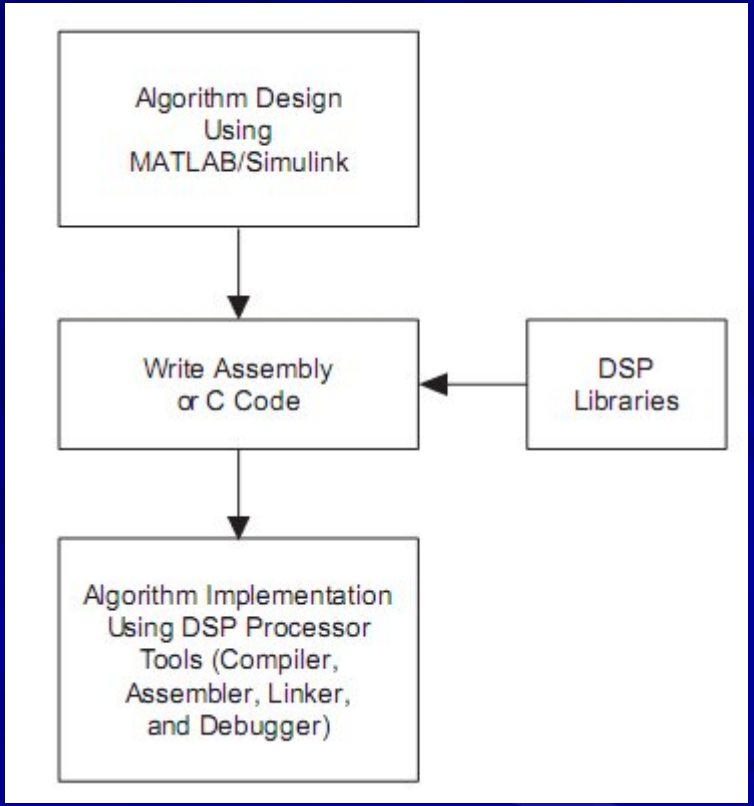
Comparison Between DSP & FPGA Solution

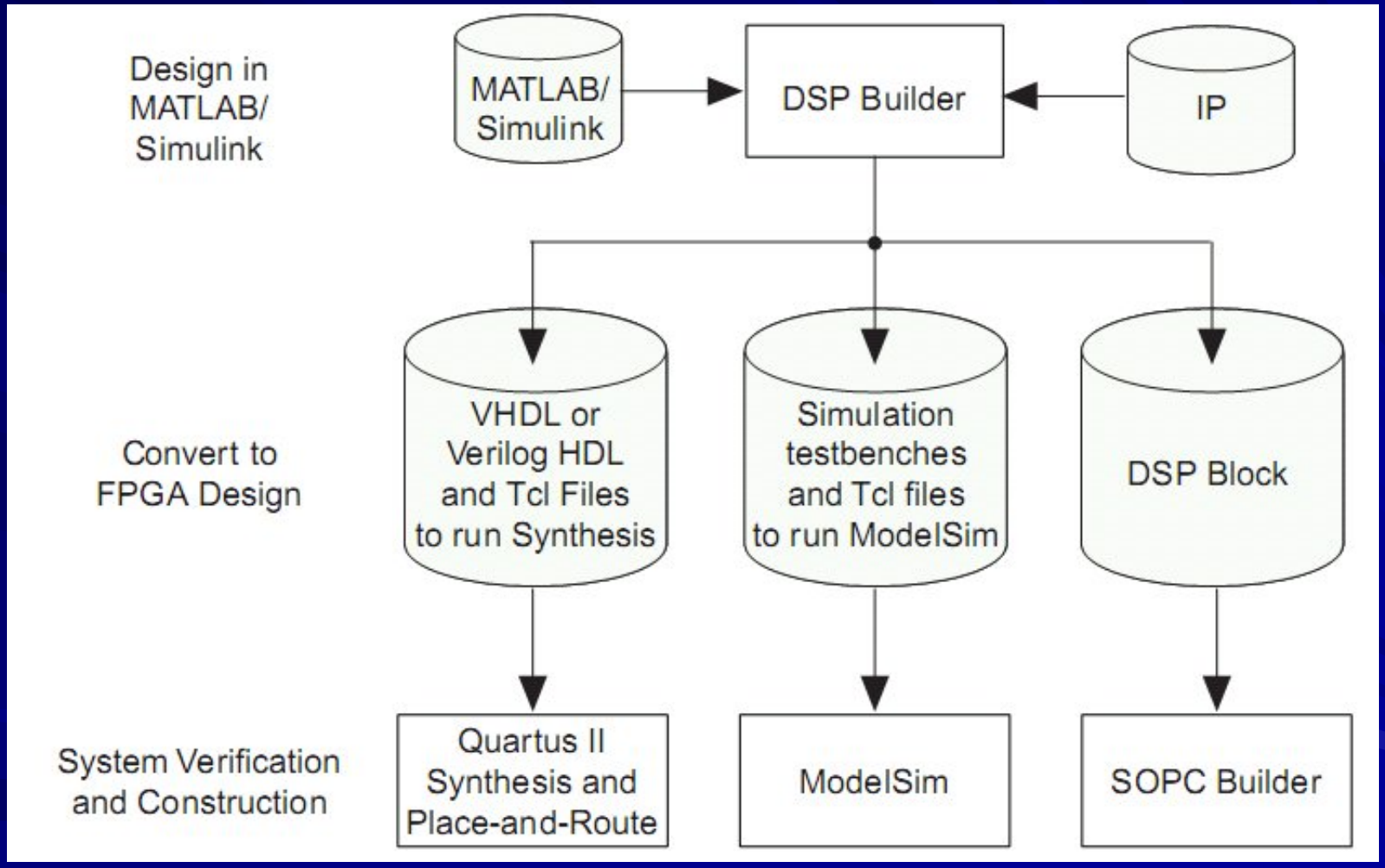
DSP	FPGA
Availability of development board with tool chain	Availability of development board with design tools set
DSP processors are programmable through software, their hardware architecture is not flexible	Provide overall system integration and flexibility while partitioning the system between hardware and software. You can implement the system's software components in the embedded processors and implement the hardware components in the FPGA's general logic resources.

DSP Design Flow

- Algorithm development tools such as MATLAB are often used to optimize DSP algorithms
- Simulink used for system-level modeling.
- The algorithms and the system-level models are then implemented in C/C++ or Assembly code using an integrated development environment, that provides design, simulation, debug, and real-time verification tools.

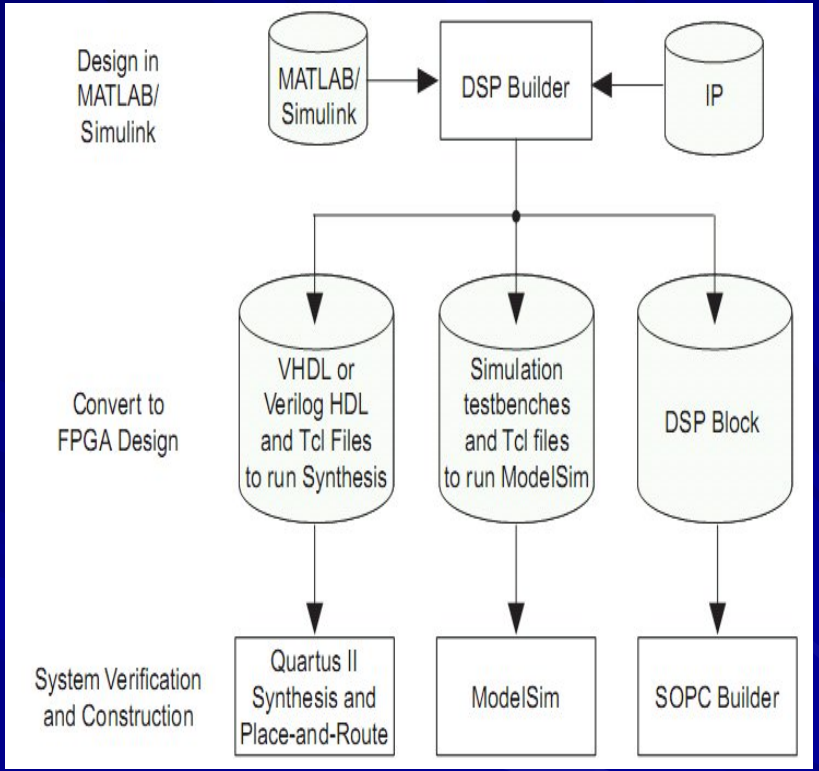


FPGA Design Flow



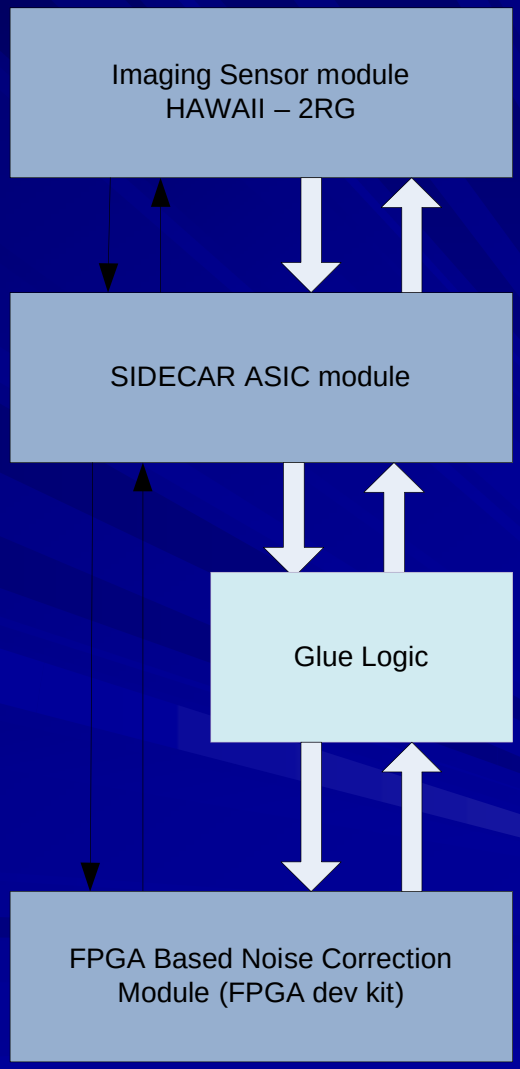
FPGA Design Flow

- DSP Builder tool provides an interface from Simulink directly to the FPGA hardware
- Able to incorporate the designs created by DSP Builder into a SOPC Builder system for a complete DSP system implementation.



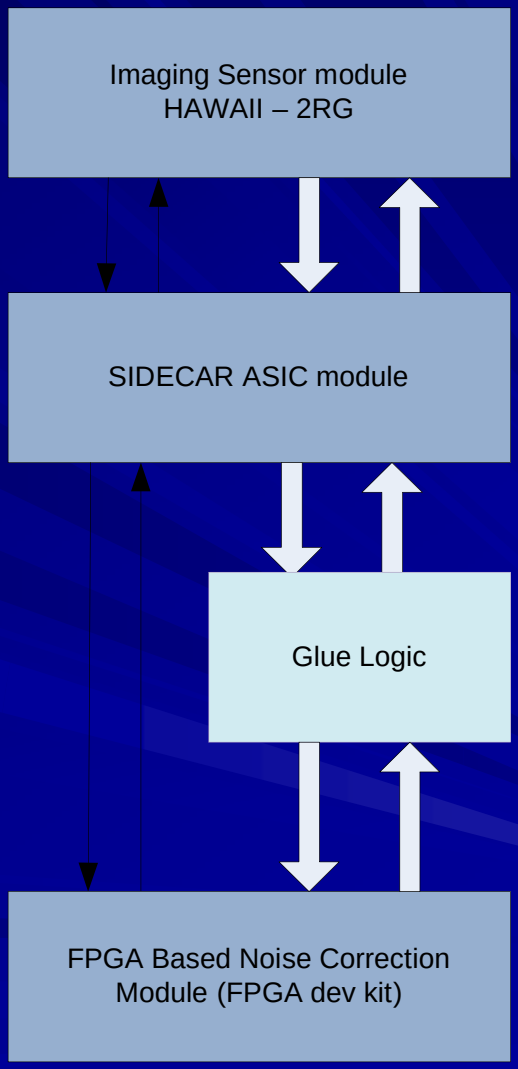
Hardware implementation options

- Using COTS FPGA development board to interface to the SIDECAR module
- Glue logic module might be required depending on the FPGA development board chosen and any voltage or timing incompatibility between the SIDECAR module and the FPGA development board



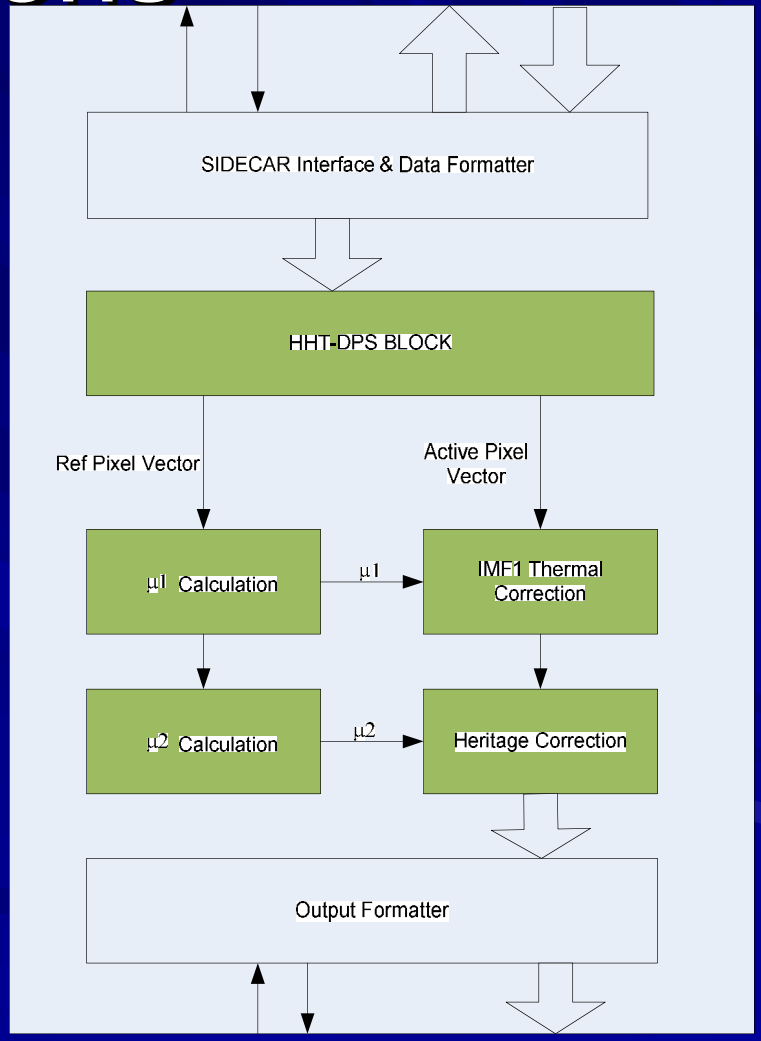
Hardware implementation options

- No custom development hardware
- Developement board typically comes with multiple output interfaces
- Maximize dev effort in testing the algorithm as well as providing us with cost saving from having to design any custom board



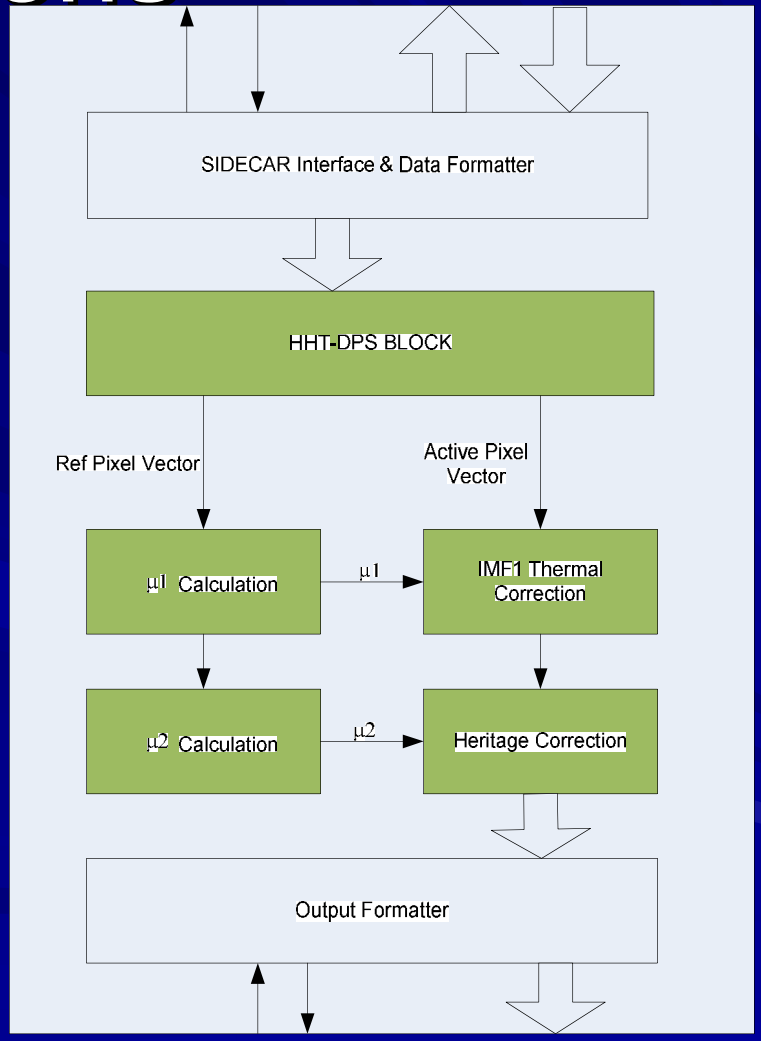
Hardware implementation options

- Potential block of major FPGA function.
- SIDECAR interface would format input data into form that is consumable by the μ1 and IMF1 thermal correction blocks



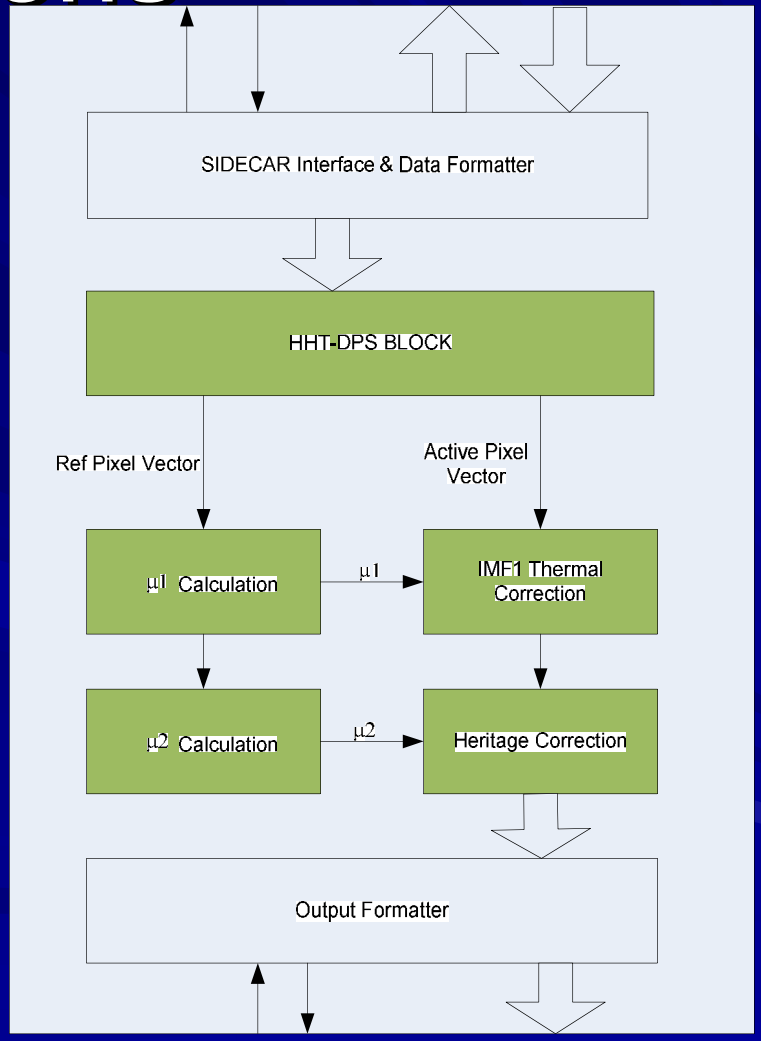
Hardware implementation options

- HHT-DPS, μ1 Calculation, μ2 Calculation, IMF1 Thermal Correction and Heritage Correction Block are synthesized from Matlab modules.
- These blocks use both, the HHT-DPS/thermal model correction for fast varying noise components algorithm and the heritage statistical parameter subtraction method for low varying noise components.

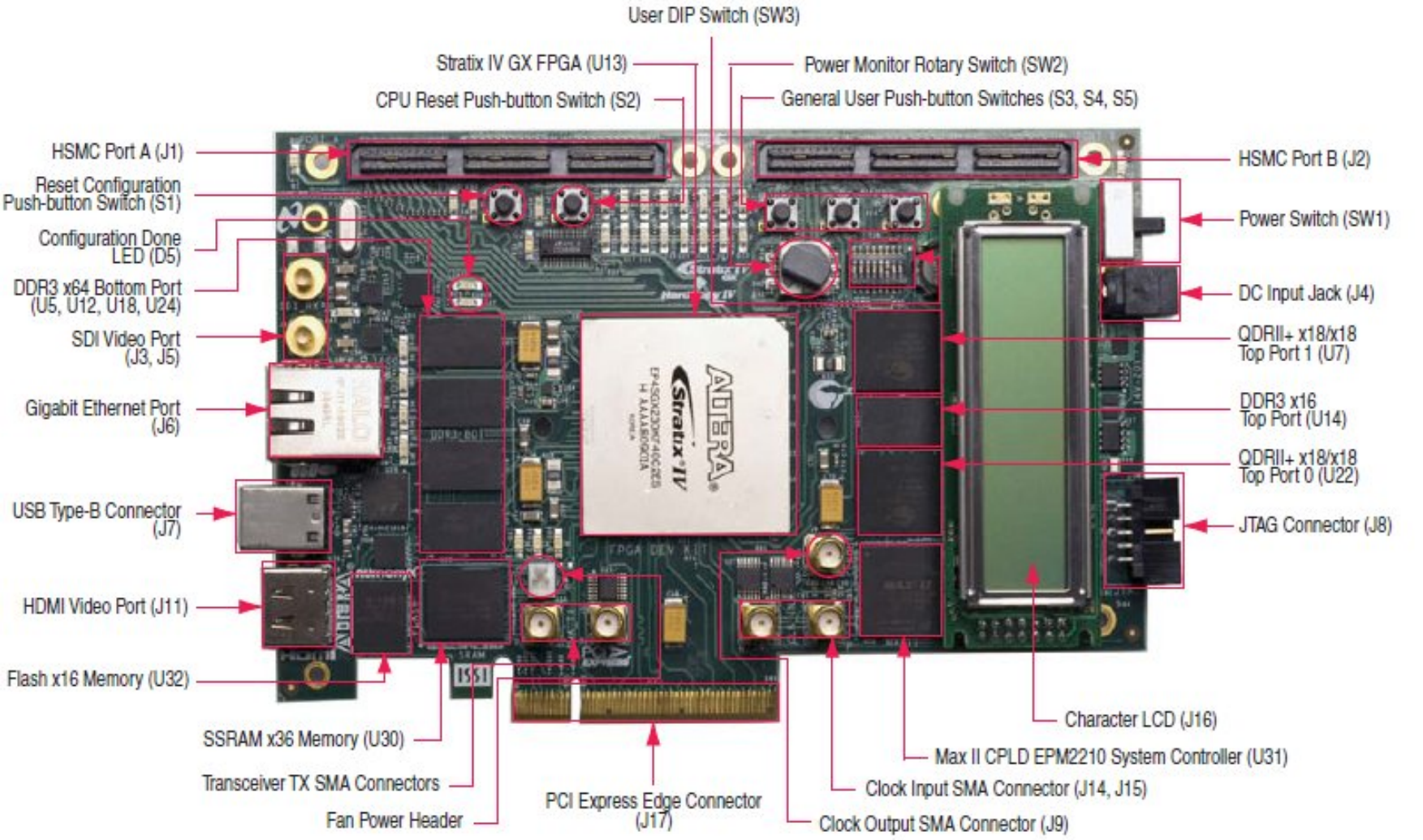


Hardware implementation options

- The thermal model will reduce the fast-varying noise (HHT-DPS first IMF), while the Heritage method which statistically average the remaining IMFs and subtract average from all hot pixels.
- As the algorithm changes, these modules will be re synthesized using FPGA vendor tool set which takes the Mathlab code as input.

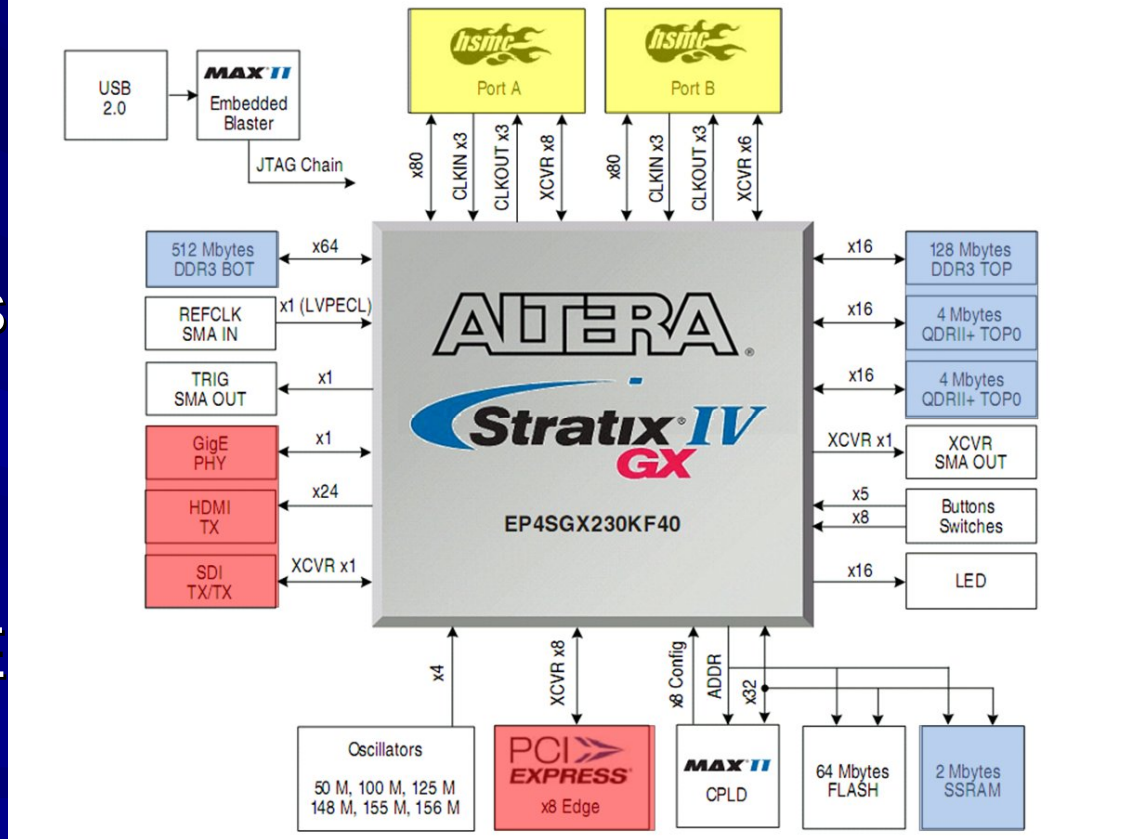


Stratix IV GX FPGA Development Board



Altera Stratix IV GX Dev Board

- Provides 168 CMOS input lines
- Provides GigE , HDMI, PCI Express, SDI output interfaces
- External memory in addition to embedded memory
- Contains 228,000 LE and 91,200 adaptive logic modules (ALMs)



Summary

- In order to process larger data set over longer time domain, a flexible hardware solution is needed.
- We have suggested FPGA based solution for the following reasons.
  - FPGA vendors have incorporated a host of features that enable high-performance digital signal processing (DSP) such as embedded memory blocks, multipliers, processors, high-speed I/Os and external memory interfaces.
  - The flexible architecture together with robust I/O interface that supports high bandwidth transfer makes this an optimal hardware platform.
  - In order to take advantage of the special DSP functional block and to provide user friendly interface, the FPGA vendor offers tool that interface to the Simulink directly and generate a synthesizable Hardware Description Language to be incorporated into the design. This would avoid any need for manual translation which tends to be error prone.
- Using FPGA development board saves us time and cost of doing a custom design and yet offers ample flexibility in term of interfaces and architectures.