Non Hermetic Ceramic Flip Chip Package Construction and Reliability

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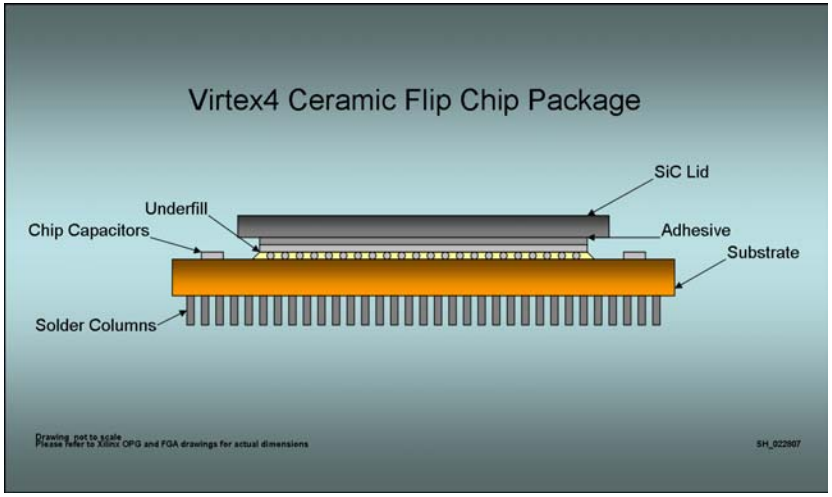
Non Hermetic Ceramic Flip Chip Package Construction and Reliability

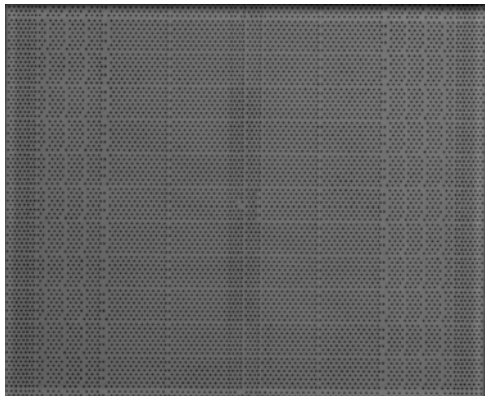
- Agenda:
  - Section 1: Package Construction Overview
  - Section 2: Why Flip Chip, Why Non Hermetic
  - Section 3: Reliability Review

Ceramic Flip Chip CGA (CF) Package Construction

- The CF package substrate is ceramic and the columns are 90%Pb/10%Sn solid solder columns.
- All Xilinx Ceramic Flip Chip package (CF) die are Flip Chip and are bumped with High Lead bumping (95%Pb/5%Sn).
- The bumped die is flipped and reflowed to the ceramic substrate at assembly. A moisture resistant epoxy underfill encapsulates the bumps.



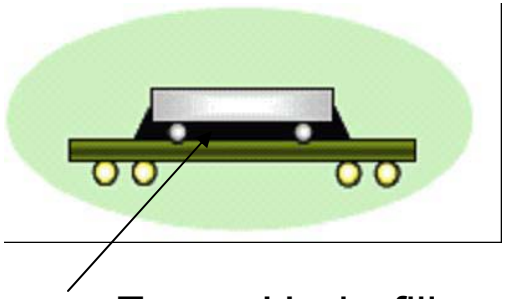
Xilinx CF Package Construction



V4 Bumped Die

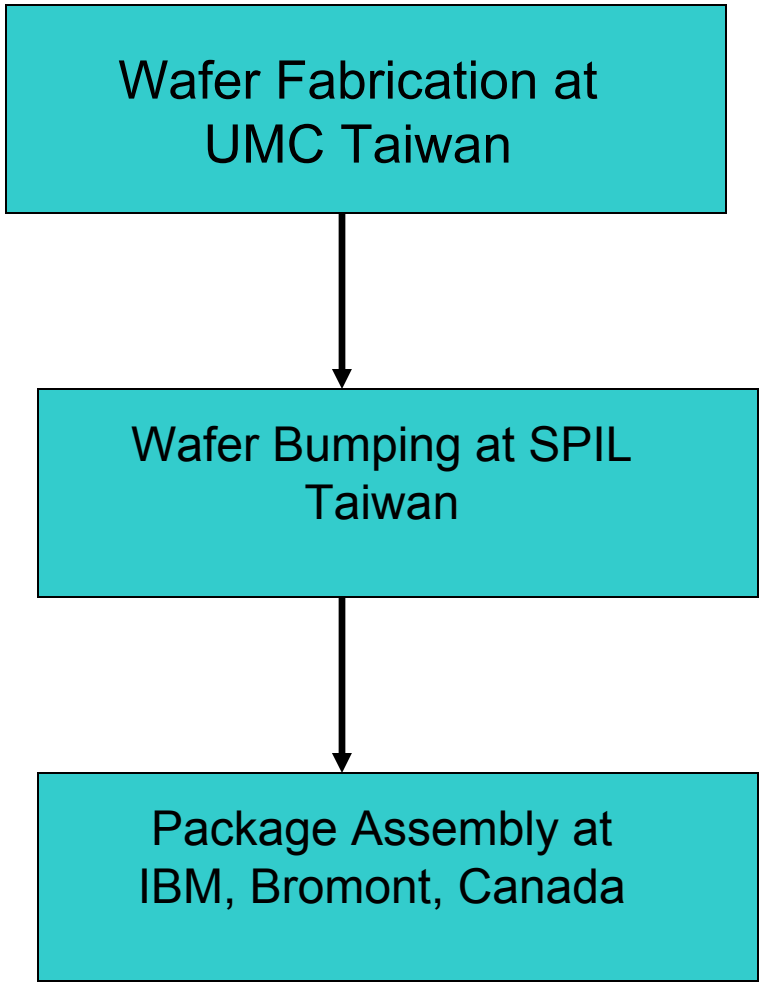
-Minimum Bump Pitch: 190 microns

-# of Bumps: 3896-8248



Epoxy Underfill encases bumps

CF Package Manufacturing Flow



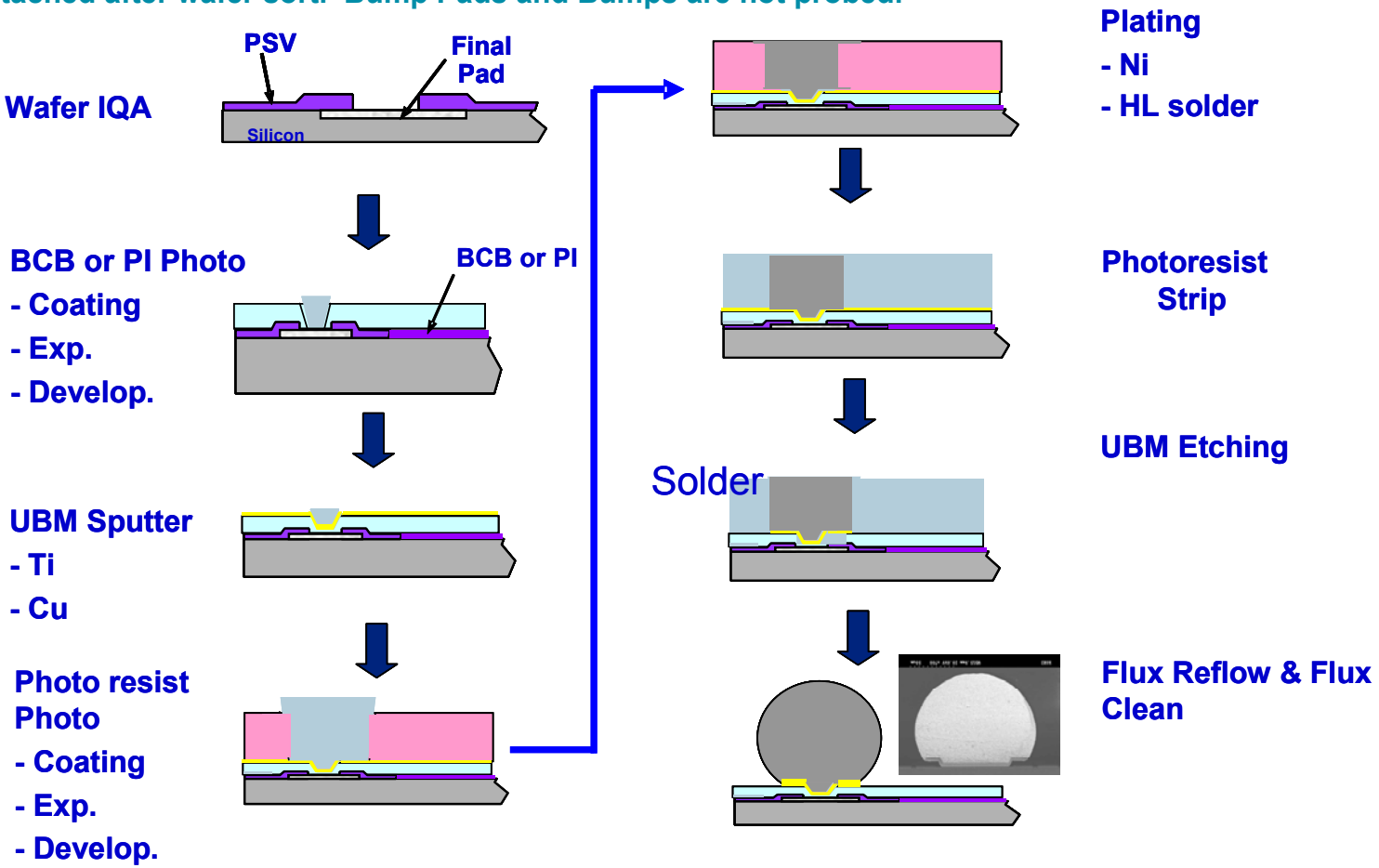
- UMC has been certified by Xilinx/DSCC
- UMC has been Xilinx's fab partner for over 20 years

- SPIL bumping has been certified by Xilinx/DSCC
- SPIL has been Xilinx's flip chip bump partner for over 10 years

- IBM has been audited by Xilinx/Aerospace Corp.
- IBM has been Xilinx's flip chip assembly partner for over 5 years

CF Package Bumping

- All CF package die are flip chip and are bumped with High Lead Bumping. (95% Pb/5% Sn)
- Bump Pads are arranged across the top surface of the die. Bump pads consist of power, ground and I/O pads.
- Bumps are attached after wafer sort. Bump Pads and Bumps are not probed.



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CF Package Assembly Flow

Wafer saw, sort & pick (300 mm (12 in) wafers)

Chip Capacitor and Chip Attach/ Cleaning

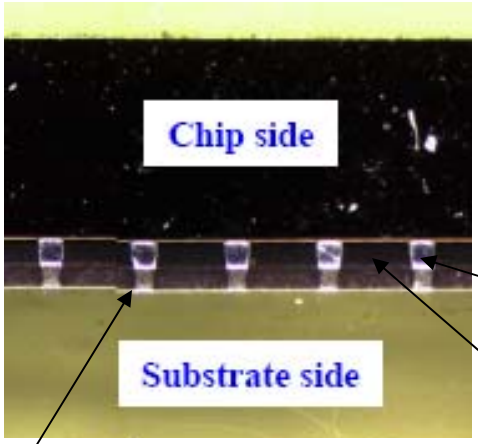
Underfill

DLA

Marking

Go for testing to XILINX

Column attach



High Lead Bumps

Underfill

Substrrate Via

CF Package Assembly Process

- **CF package is assembled at IBM using IBM's qualified material set/process flow**
- **Xilinx and Aerospace Corp. have audited IBM and have added the following additional assembly process monitors to Xilinx's Class V flow to closely match Class S military screening requirements:**

Assembly Monitor	Sample Size	Xilinx Specification
Die Visual Inspection	100%	MAC0123
Die Adhesion Test (Pad Wettability Test)	Package Substrate Lot Acceptance, 1% per substrate lot	MFC0087
Die Bump Shear and Die Bump Pull Monitor	Lot Acceptance, 3 units per assembly lot	MAC0117
Underfill Coverage Monitor (CSAM)	100% of lot	MAC0120
Lid Shear Test	Lot Acceptance, 8 units per assembly lot	MAC0118
Temperature Cycle	100% of lot, 50 cycles, Condition C (-65 to 150 C)	MFC0087

Why Flip Chip, Why Non Hermetic

- All Xilinx V4/V5 devices are only offered in Flip Chip for both commercial & military markets.
- Flip Chip gives the best electrical performance. Eliminating wire bond wires improves the inductance and capacitance of the electrical connections.
- Flip Chip connections uses the whole area of the die (compared to the peripheral for wire bond) thus allowing more I/O, Power & Ground signals.
- Non Hermetic Ceramic Flip Design allows Xilinx to assemble at IBM. IBM has been assembling Non Hermetic Ceramic Flip Chip for over 30 years, so the package has a proven excellent reliability record.

Ceramic Flip Chip Reliability

- **CF Package has proven excellent Reliability:**

Reliability Characteristic	Detail
MSL 1: Package is rated as a Moisture Superior MSL 1 (Package has passed 168 hrs 85/85 followed by 4000 TCB testing)	2 Passivations (BCB & SiN) cover the top surface of the die. Epoxy underfill protects the bumps from moisture.
CTE Matching: CTE of the ceramic package (7) closely matches the die CTE (3)	CTE matching eliminates thermal expansion stresses and so there is little risk for bump or die cracks with ceramic flip chip.
Excellent Bump Quality	Automoated bumping fabrication process provdes strong bumps. Bumps are not probed and are 100% visualed before assembly.
Strong Bump to Package Interconnection	Bumps form strong solder joint connections with the package. No marginal connections (like low wire pull on wire bond packages) are seen.
Multiple 100% Open/Short Electrical Testing	All package connections go through multiple 100% Open/Short testings in the screening flow as part of Final Test.

Virtex-4, XQR CF Package V Grade Qualification Summary

- **Virtex-4, XQR-CF product has completed and passed qualification to the requirements of MIL-PRF-38535 & MIL-STD-883.**
- **Product qualified are:**

Family	Device/Package
V4	XQR4VLX200-10CF1509V
V4	XQR4VSX55-10CF1140V
V4	XQR4VFX60-10CF1144V
V4	XQR4VFX140-10CF1509V

- **Product has passed the following qualification tests:**

Qualification Test	Test Method	Sample Size	Device	Results
Group A testing	Mil Std 883, TM5005	100%	All 4 V4 XQR CF's	Pass
Modified* Group B Testing	Mil Std 883	per Mil Std 883	All 4 V4 XQR CF's	Pass, see Section 1
Group C testing	Mil Std 883, TM1005	15 units per device	XQR4VFX60, XQR4VLX200 & XQR4VSX55	Pass, see Section 2
Group D testing	Mil Std 883	per Mil Std 883	XQR4VLX200 & XQR4VSX55	Pass, see Section 1
Group E testing	Mil Std 883	per Mil Std 883	All 4 V4 XQR CF's	Pass
BLR Temperature Cycle Testing	IPC 9701	per IPC 9701	XQR4VLX200-CF1509	Pass, see Section 3
MLS 1 testing + CSAM	JEDEC Std 020A	15 units	XQR4VLX200-CF1509	Pass, see Section 4
Package Temperature Cycle Condition B Testing + CSAM	JEDEC & Xilinx Std	14 units	XQR4VLX200-CF1509	Pass, see Section 4
Outgassing Testing	ASTM E-595	3 units	CF Underfill and Lid Adhesive	Pass, see Section 5
Wear Out Tests	Xilinx Std	Xilinx Std	V4	Pass, see Section 6
Mask Qualification (Latch Up and ESD)	Xilinx Std	Xilinx Std	All 4 V4 XQR CF's	Pass, see Section 6

* Some tests do not apply to ceramic flip chip

Appendix: Virtex-4, XQR CF Package Group B & D Qualification Results

- **Group B and D Test Results:**
  - **Group B Test Results:**

Subgroup	Test	Method	Sample Size	Results
1	Physical Dimensions	2016	2	Pass
	Internal Water Vapor	1018	N/A	Parts are not hermetically sealed
2	Resistance to Solvents	2015	N/A	Parts are laser marked
	Internal Visual and Mechanical	2013	2	Pass
	Die Pull (Bond Strength/Die Shear)	IBM Std	3	Pass
3	Solderability	IBM Std	1% per substrate lot	Pass
N/A	CSAM	IBM Std	100% of lot	Pass
N/A	Lid Shear	IBM Std	8 units per lot	Pass

  - **Group D Test Results: D3 & D4 units passed -55, 25 and 125 °C electrical testing before and af**

Subgroup	MIL-STD-883			Sample Size	Results	Ref #
	Test	Method	Condition			
1	Physical Dimensions	2016		2	0 fail	N/A(1)
3	a. Thermal Shock	1011	B, 15 cycles	15	0 fail	STS139014
	b. Temperature Cycle	1010	C, 100 cycles	15	0 fail	
	c. Moisture Resistance	1004		15	0 fail	
	e. Visual Inspection	1004 &1010		15	0 fail	
	f. End-Point Electrical Test			15	0 fail	
4	a. Mechanical Shock	2002	B	15	0 fail	STS139015
	b. Vibration	2007	A	15	0 fail	
	c. Constant Acceleration	2001	E, Y1 only	15	0 fail	
	e. Visual Inspection	1010		15	0 fail	
	f. End-Point Electrical Test			15	0 fail	
5(2)	a. Salt Atmosphere	1009	A	15	0 fail	STS137031
	c. Visual Inspection	1009		15	0 fail	

Appendix: Virtex-4, XQR CF Package Group C, Steady State Life Test Qualification Results

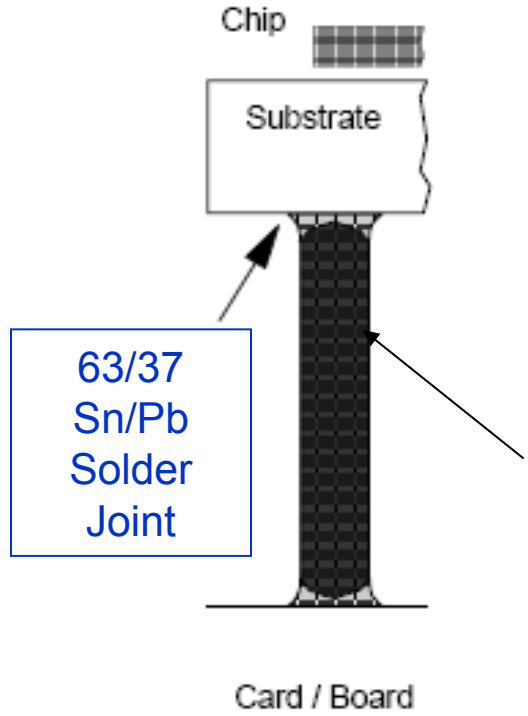
- **Virtex 4, XQR4VFX60, XQR4 VLX200 & XQR4VSX55 V Grade CF product have successfully passed qualification with each device passing 2000 hours of steady state life.**
- **Steady State Life Conditions are per Mil Std 883, Method 1005 as follows:**
  - Static Burn In, Temperature = 125°C -0/+8°C
  - VCC CORE: 1.26v
  - VCC AUX: 2.625v
  - VCC IO: 3.45v
  - -55, 25 and 125 °C Electrical Testing at each readpoint

Appendix: Virtex-4, XQR CF1509 Package - Board Level Reliability (BLR) Temperature Cycle Summary

- **Background:**
  - Daisy Chain CF parts were assembled and columns were attached following the Xilinx production approved IBM V flow.
  - Parts were then attached to 8-layer thick FR4 boards and put through Temperature Cycling Condition J (0°C to 100°C)
  - Daisy Chain nets were continuously electrically monitored for resistance change.
  - Failure criteria is when the resistance of a net exceeds the threshold resistance (300 ohms)
- **BLR testing successfully completed using XQR4VLX200-CF1509 IBM columns**
  - Results very good with first failure not seen until 3892 cycles.
- **IBM column is used on all Xilinx CF products.**

Appendix: Virtex-4, XQR CF1509 Package - Board Level Reliability (BLR) Temperature Cycle Summary

- **90 Pb/10 Sn IBM Column:**
  - After Final Test screening, CF packages are column attached at IBM with 90 Pb/10 Sn columns using IBM's proprietary CLASP process.
  - Columns are non Wire solid solder.
  - IBM's column attach CLASP process is fully automated with no manual handling.



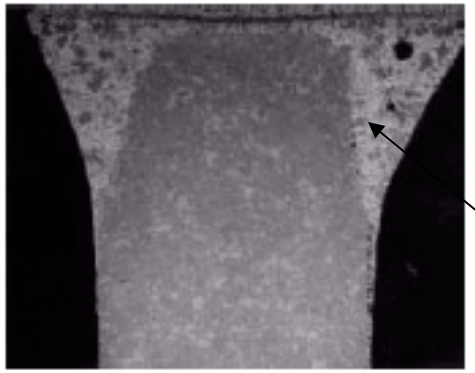
63/37 Sn/Pb Solder Joint

90 Pb/10 Sn Column

2.35 mm max height

.56 mm (22 mil) max diameter

• Column is attached to the CF package substrate using Eutectic solder and additional dopant. Intermetallics form at the column to package interface which add strength to the solder joint and causes the joint to not melt during board attach.



Intermetallic

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Appendix: Virtex-4, XQR CF1509 Package - Board Level Reliability (BLR) Temperature Cycle Summary

- Test Board
  - 8 Layer FR4 Board: Signal/GND/Signal/Power/Signal/GND/Signal/Power
  - 0.70mm NSMD Pad, 0.85mm Solder Mask Opening, HASL Finish
  - Size: 220x140x2.36 mm
- Package
  - Substrate Thickness: 2.97 mm.
  - Package size: 40 x 40 mm
  - Die size: 23.8 x 20.4 mm, XQR4VLX200
  - Column: 0.56mm diameter with 1.0mm pitch
  - Pad size: 0.80mm
- Test Condition
  - Temperature Cycle, 0^0C to 100^0C
  - 30 min/cycle (10min. Dwell and 5min. Ramp)
- Test Results
  - 24 out of 27 units failed until 5305 cycles

Package	Cycles Completed	# Tested	# Failed	1st. Failure (Cycles)	Characteristic Life (Cycles)
CF1509	5305	27	44	3892	4707

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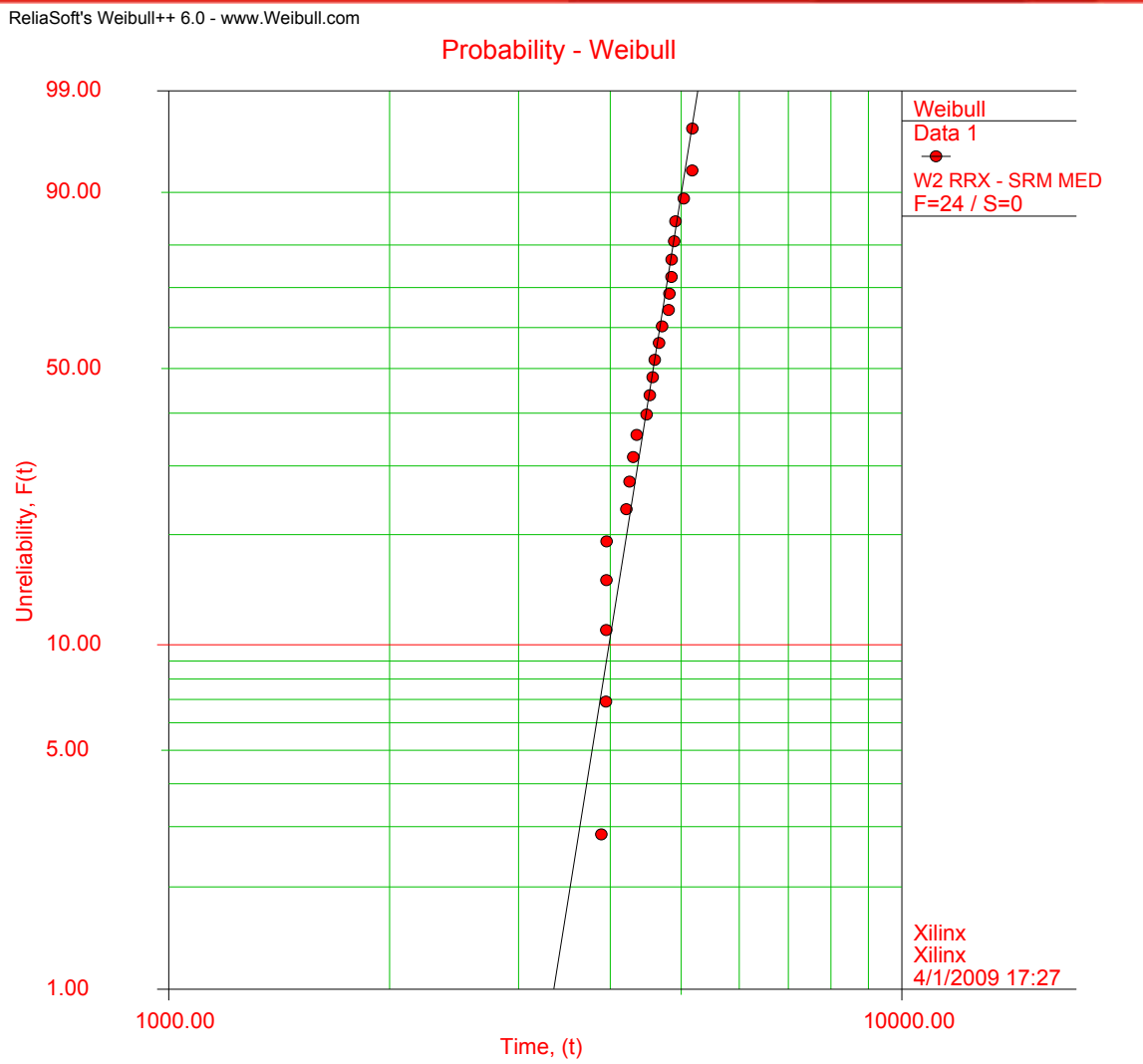
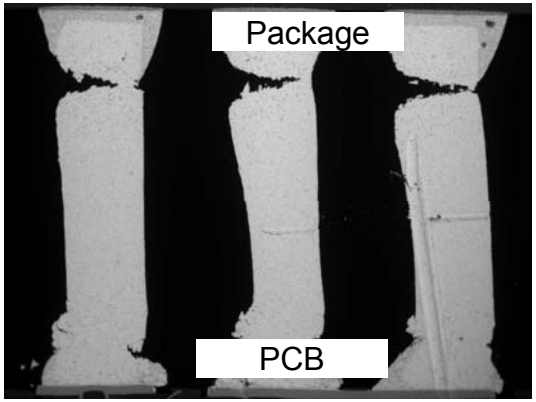
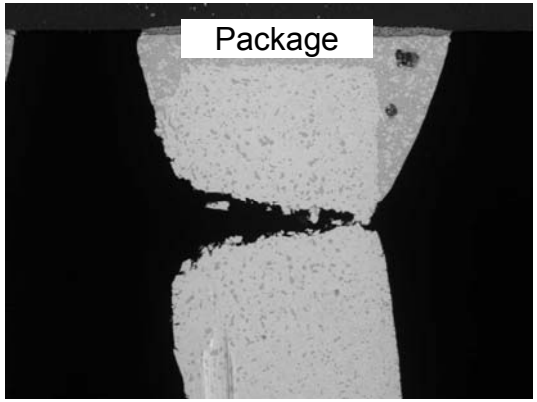


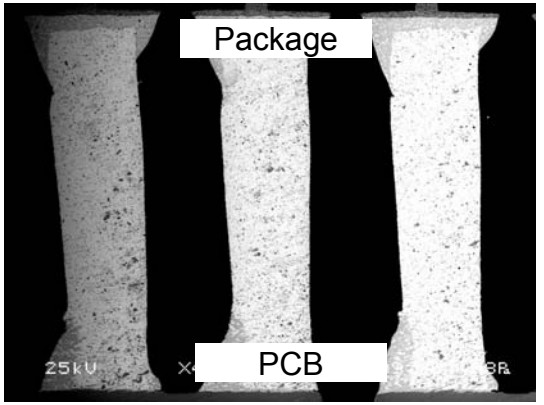
Appendix: Virtex-4, XQR CF1509 Package - Board Level Reliability (BLR) Temperature Cycle Summary

- **Failure Analysis**
  - Cross section of the failing chain showed that the failure occurred at the columns on the package side.





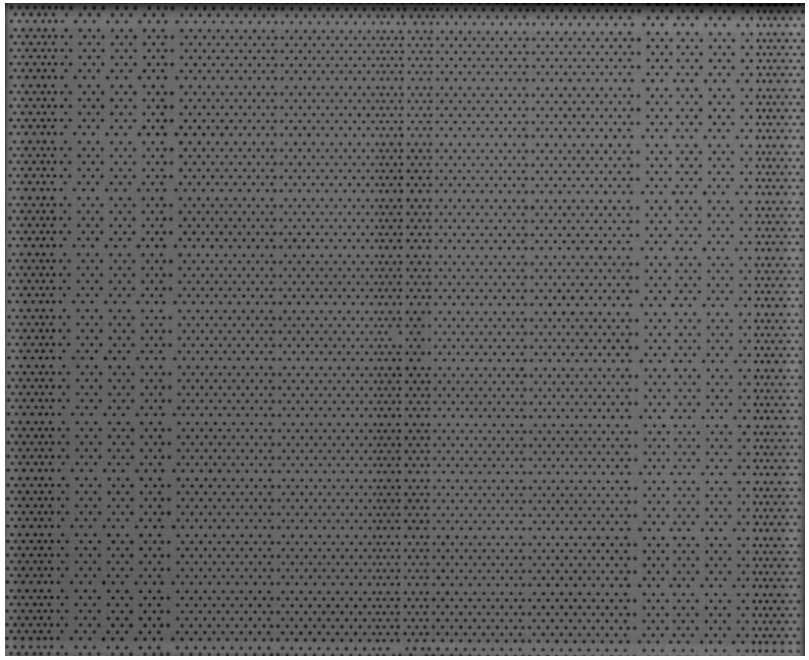
SEM photo of crack columns of First Fail Unit – SN112



SEM photo of good columns

Appendix: XQR4VLX200-CF1509 Moisture PreConditioning Qualification Results

- XQR4VLX200-CF1509 has been put through MSL 1 Preconditioning (168 hrs. 85°C/85% RH) followed by 25°C Electrical Test & CSAM. Results are as follows:
- - 15/15 units pass Electrical testing after Preconditioning.
- - 1/1 units pass CSAM inspection. See below.



Appendix: XQR4VLX200-CF1509 Package Temperature Cycling Qualification Results

- Temperature Cycling Test Conditions:
  - Condition B (-55 to 125° C) followed by 25°C Electrical Test on fully electrically functional die.
- Results:
  - 14/14 units pass Electrical testing at 1000, 1500 & 2000 3000 & 4000 cycle readpoints.

Appendix: XQR CF Package Outgassing Results

- CF Package Material Set passes outgassing criteria per ASTM E-595 testing and criteria.
- Key Outgassing Parameters:
  - TML (Total Mass Loss)
  - CVCM (Collected Volatile Condensable Materials)
- Specification:
  - TML < 1%
  - CVCM < 0.1%
- CF Package Outgassing Data is as follows:

	Underfill (LP2)	Lid Adhesive (ATI)
TML %:	0.21%	0.36%
CVCM %:	0.01%	0.01%

Appendix: XQR CF Package Wear Out Test and Latch Up and ESD Test Summary

Wear Out Test Summary for M-Grade and V-Grade Products

Table 4: Wear-out Test Summary

Mechanism	Sample Size	Condition s of Stress Test	Conditions of Quoted results	Failure Criterion	Comments	Product Life Time at Tj of	
						100°C	125°C
Hot Carrier Injection	20 per condition	3 voltages 25°C	≥1.05Vcc 125°C for com, -55°C for IO	Δ Idsat > 10%	Worst at cold for IO NMOS & hot for others	53 years	50 years
Vt stability	10 per condition	3 voltages/3 temps., 100 to 160°C	1.05 Vcc, 125°C	100mV for core/mid oxide; 110mV for 2.5V device; 200mV for 3.3V device	Verified by product HTOL	42 years	12 years
Gate oxide TDDB	20 per condition	3 voltages/3 temp., 300°C to 160°C	1.05 Vcc	Ign/Ign - 1>1.2 for core NMOS/mid oxide & 2 for core PMOS, >10 for IO CDF = 0.1%	Equivalent to 11 FITs after 10 years	157 years for LX200	27 years for LX200
Electromi-gration	20-24 per condition	250°C to 350°C	design rule I_{max} at 100°C	Δ R/R >20% CDF = 100 PPM	Equivalent to 1 FIT after 10 years	34 years	6 years
VRDB	total test areas >0.2cm^2 for area; > 1E3cm for STI edge; > 1E4cm for poly edge	Voltage ramp @ 25°C	DD	Ign/Ign - 1>1.2 for core & mid oxide, >10 for IO	B mode 1.1Vcc<VBD <2.3 Vcc	pass	Pass

Table 4: Wear-out Test Summary (Continued)

Mechanism	Sample Size	Condition s of Stress Test	Conditions of Quoted results	Failure Criterion	Comments	Product Life Time at Tj of	
						100°C	125°C
SM	20-30 per condition	3 tempera-tures 1000 hours	pass or fail	Δ R/R >20% of EDR for single via; Δ R/R > 2.5% for via chains	No sample stress fail allowed	pass	Pass
BEOL TDDB	16-20 per condition	125°C-200°C	1.1 Vcc, 100°C	line to line leakage > 1 µA CDF=0.01 %	Equivalent to 1 FIT after 10 years	646 years	214 years

The Latch-Up, HBM and CDM tests are performed according to the following industry standard specifications:

- Latch-Up: JESD-78, ±200mA and 1.5 x V_{DD} *
- HBM: JESD-22-A114, ESDA STM5.1
- CDM: JESD-22-A115, ESDA STM5.3.1

Table 5: Mask Qualification Summary

Device	Latch-Up	HBM Passing Voltage	CDM Passing Voltage
XQ4VLX60	pass	2000V	400V
XQR4VLX200	pass	2000V	350V
XQR4VSX55	pass	2000V	400V
XQR4VFX60	pass	2000V	500V

*Latch up performed at 125°C

Reference: Xilinx RPT102 Qualification Report