FPGA Based Verification Simulation Accelerator and Assurance for FPGA/Firmware Model-Based Design

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Project Objective:

This initiative aims to dramatically reduce the time required to perform V&V for critical FPGAs for JPL Flight Projects, and ultimately improve the quality of the products.

Benefits to NASA and JPL:

- ✓ Increasing complexity and criticality of the devices required by today's missions and by future missions
  - → 32k gate devices on MER
  - → 2M gate devices on MSL
  - → 4M gate devices on future missions
- ✓ Verification of complex hardware/software systems for space missions is very time consuming
  - → Even 32k gate devices can take 3 months to verify

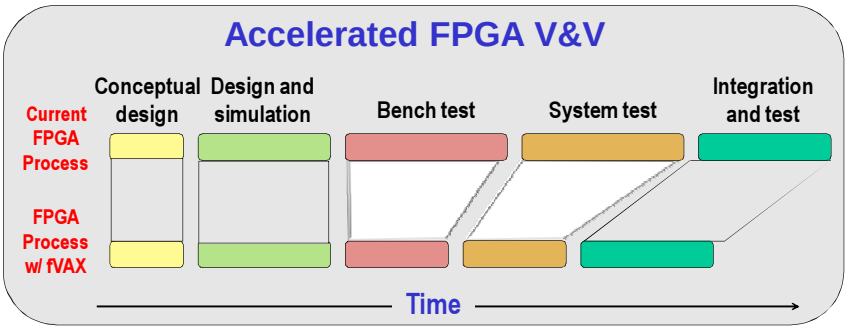
❖ **Improved system validation**

→ Perform validation in flight-like environment

❖ **Faster and more effective verification**

→ Reduce the amount of time required for verification, and reduce defect escapes

Accelerated FPGA V&V



FY08 Results:

Deliverables are:

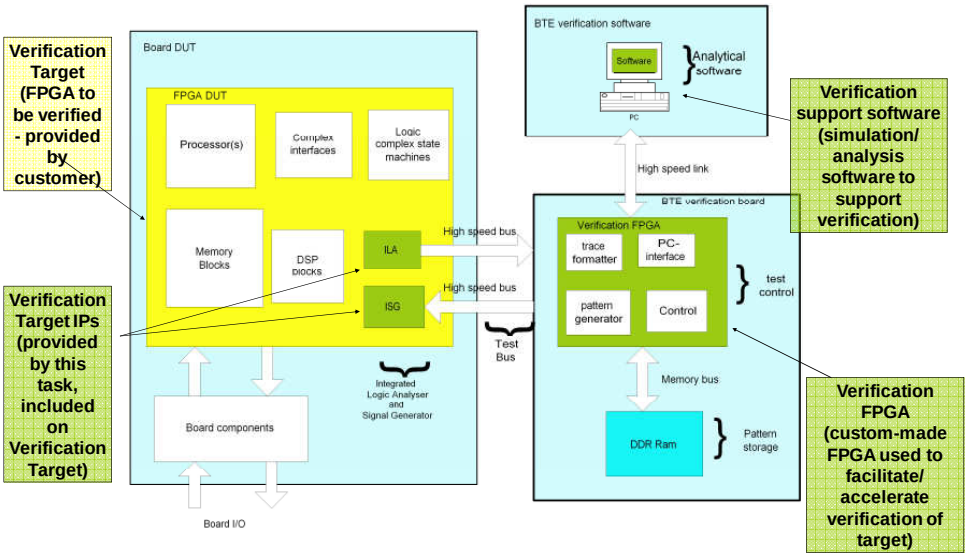
- Custom-made FPGA used to facilitate/accelerate verification of target
- Integrated Logic Analyzer (ILA) used to sample and monitor internal nodes of FPGA
- Integrated Signal Generator (ISG) used to generate data patterns to step through FPGA
- Validation Support Software used to display actual in wave forms
- Design Documentations and user's training manuals

FPGA based verification accelerator (fVAX) provided:

- High visibility of FPGA internal signals and nodes
- Method to find source of problems (e.g., runs test sequence, triggers on error, captures results in fVAX)
- Comparison of actual with model
- High speed busses connected to the verification FPGA which has a high speed link to a PC
- Automated high-speed verification tests, directed by the PC, and monitored continuously for correctness

Publication:

❑ Jane Oh and Gary Burke, "Development of FPGA-based Verification Simulation Accelerator", submitted to *Components for Military and Space Electronics Conference and Exhibition*, San Diego, CA, 2008.
❑ Jane Oh and Gary Burke, "FPGA Verification Accelerator", submitted to *Military and Aerospace Programmable Logic Devices (MAPLD) Conference*, Annapolis, MD, 2008.



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