Aeroflex Solutions for Stacked Memory Packaging

Increasing Density while Decreasing Area

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www.aeroflex.com/memories

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Abstract

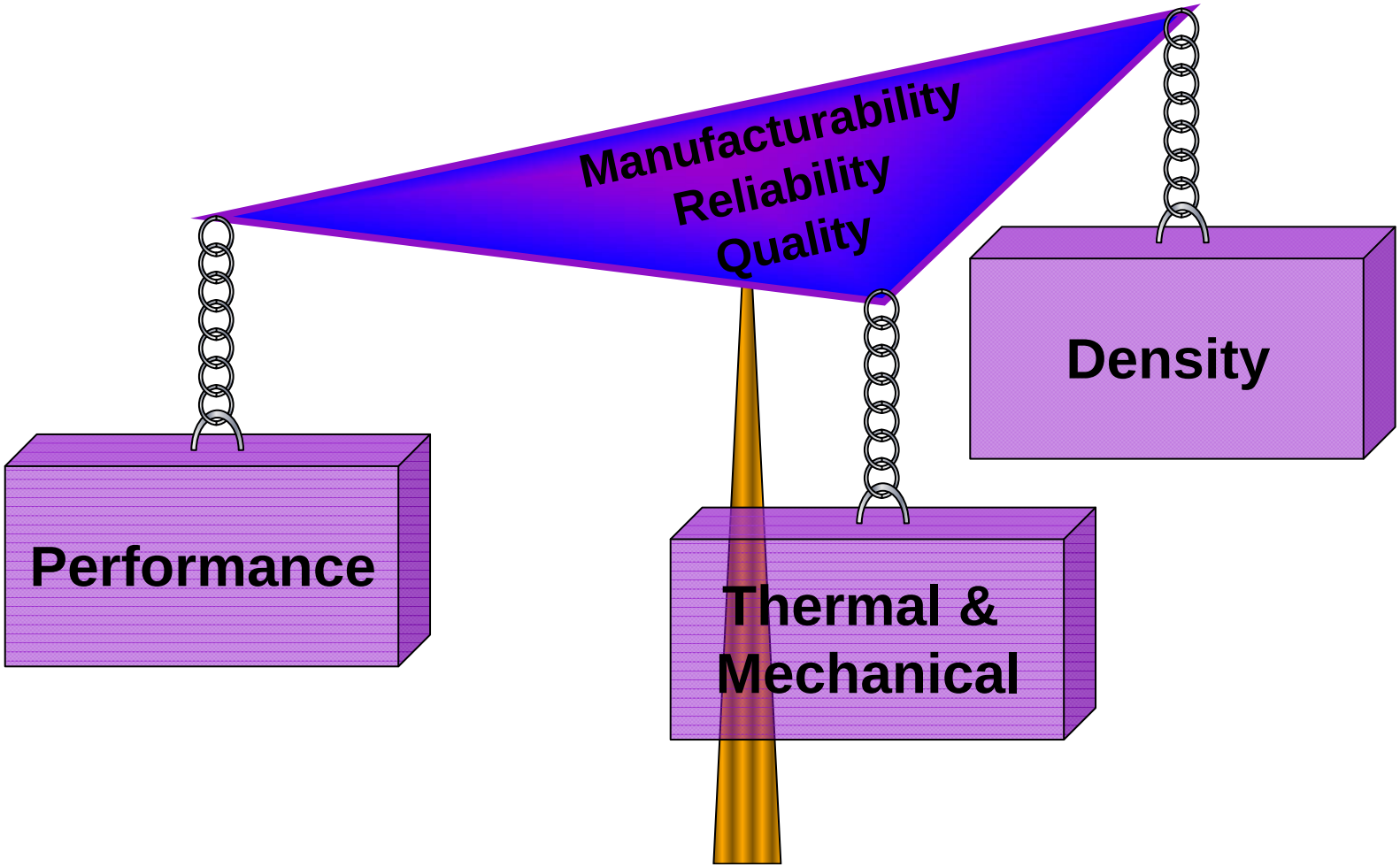
The aerospace industries continuous appetite for greater memory density in smaller footprint packages has driven Aeroflex Colorado Springs to develop new techniques for memory design and stacked die packaging. Memory requirements now exceed the device density and board area available using single die packaging, even as shrinking process geometries allow for monolithic die density of 16 – 20Mb. Stacking multiple die in a single package provides dramatic improvements in memory density per square mm of board space, while maintaining high performance. However, die stacking in multi-cavity packages introduces a whole new series of thermal and mechanical issues. In particular, due to increased thermal resistance, high junction temperatures can be created in stacked die which increases their leakage current and power dissipation while decreasing their reliable operating life.

To address these concerns, Aeroflex has modified both the electrical and mechanical procedures for the management of stacked die in Aeroflex memory products. Improvements in the attachment interfaces between die, along with package design for thermal conductivity serves to optimize the thermally conductive path from the stacked die through the package out to the ambient environment.

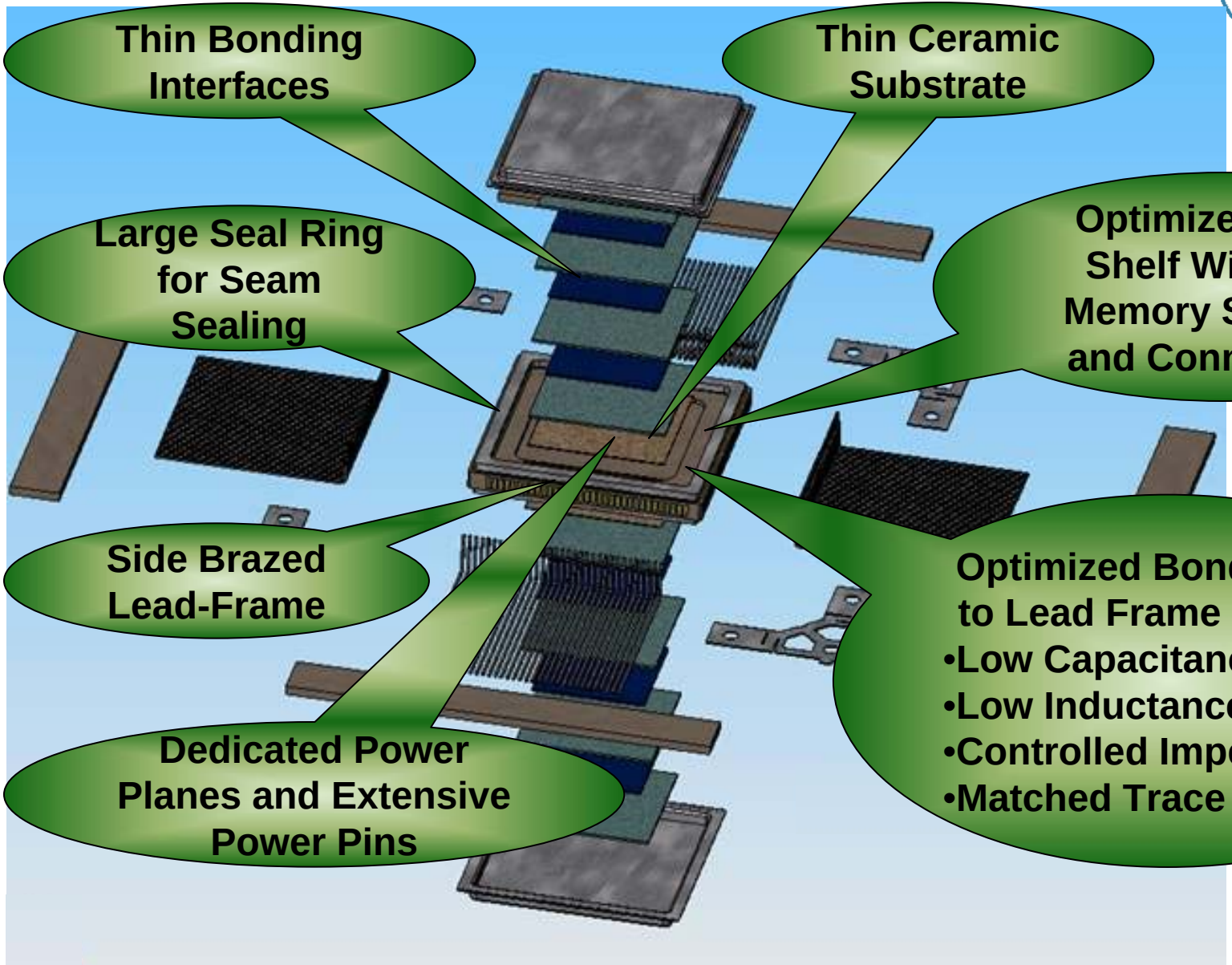
This paper will focus on the specifics of the power and thermal management techniques used by Aeroflex in the development of their stacked die memory products. Discussion will include overall package design, bonding interface materials and elimination of voids, thermal conductivity. A review of current and future Aeroflex memory products will define a roadmap from monolithic, single cavity design of 16M SRAMs up to multi-cavity, stacked die providing 160M of SRAM density.

The Packaging Challenge…

- **A successful solution balances performance, density, and thermal aspects of the product in a manufacturable process**

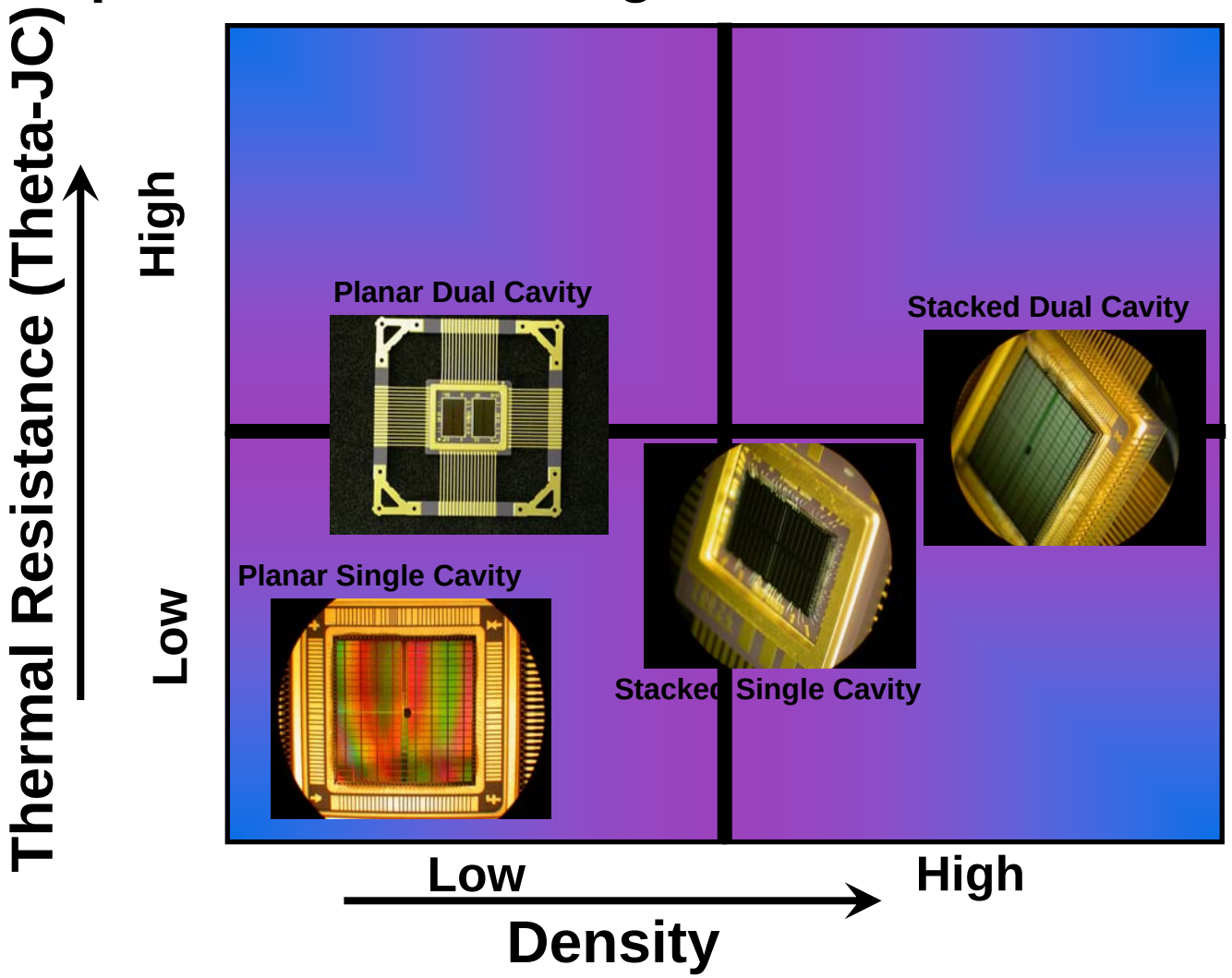


Memory Packaging for Performance

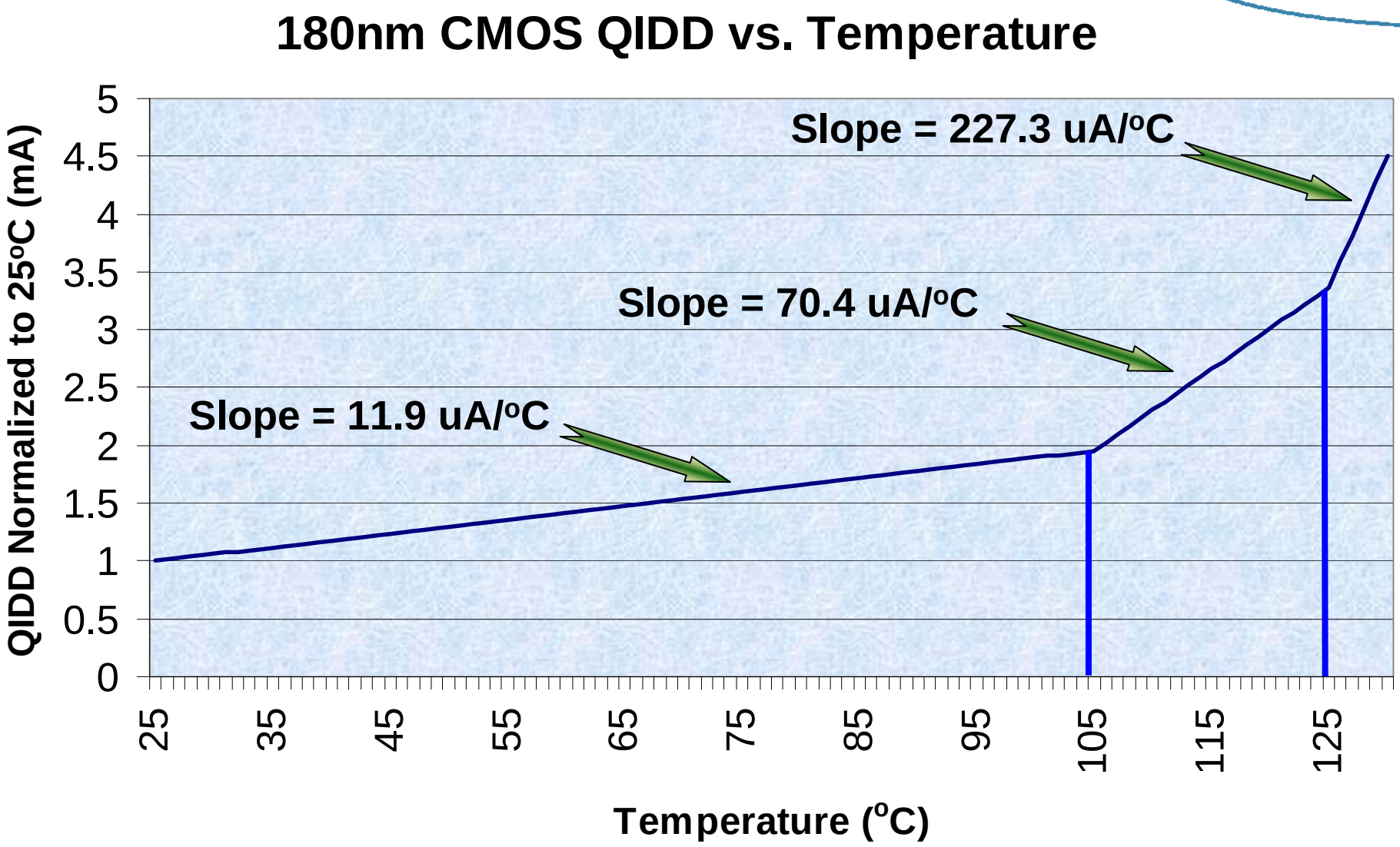


Density…

- **Stacking achieves high density in minimal board space while reducing total cost**

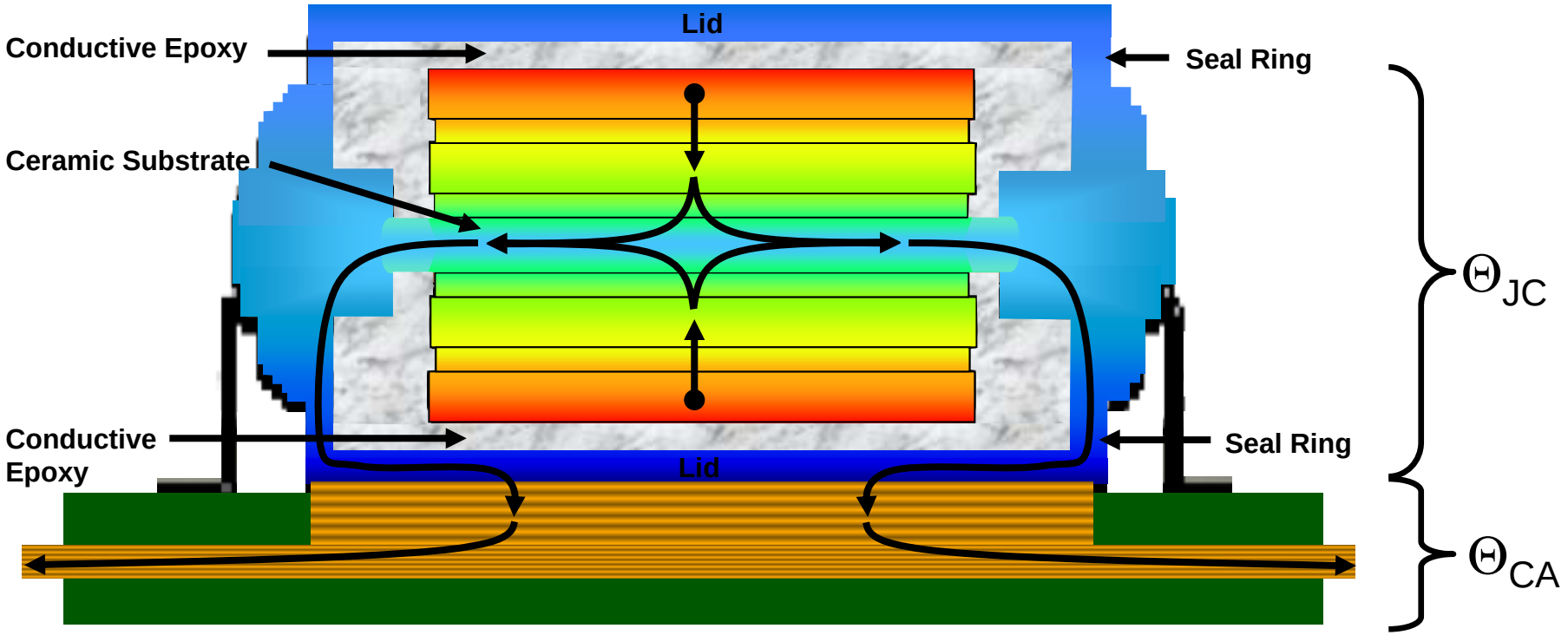


The Power of Temperature Reduction



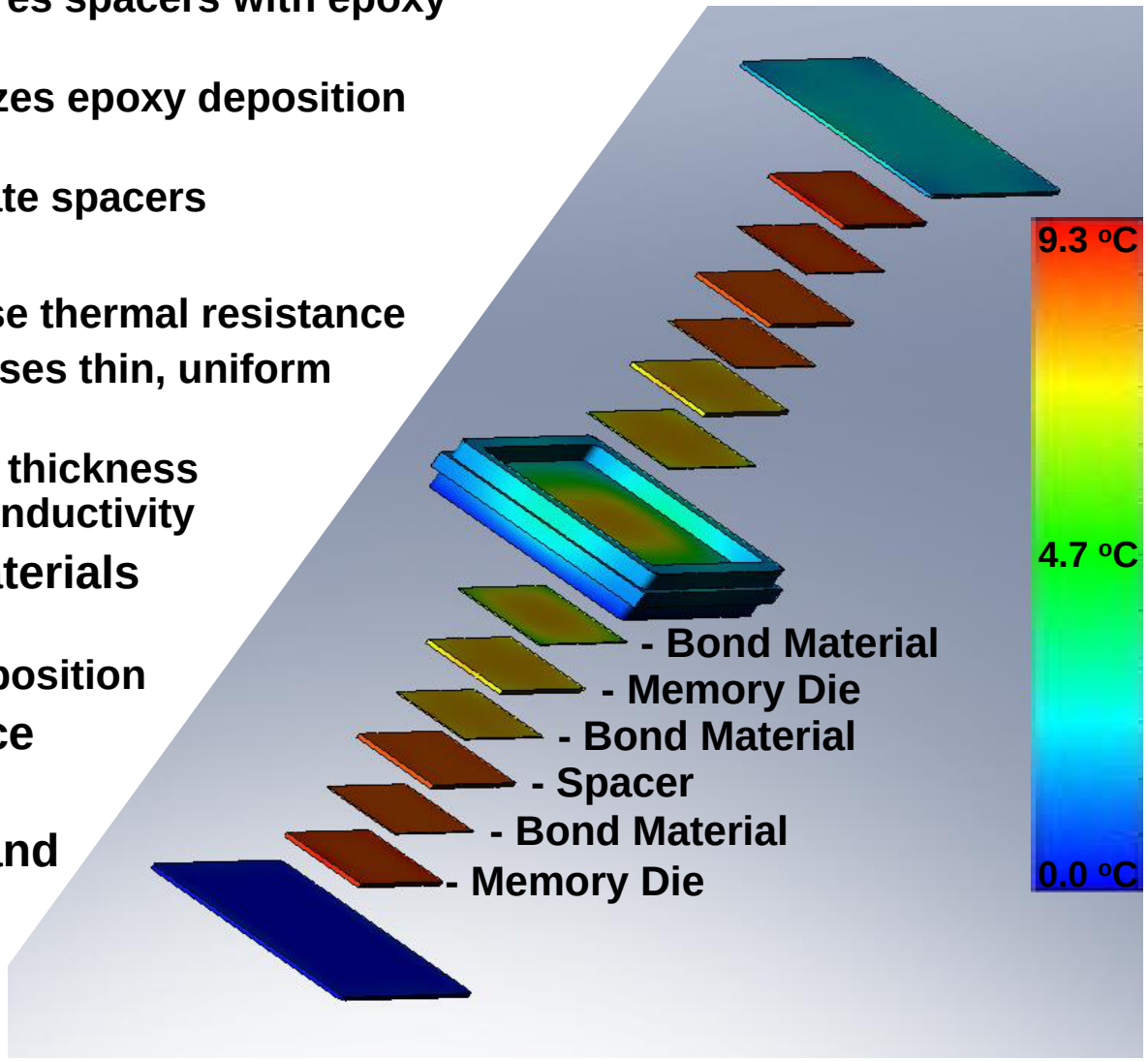
Thermal Resistance and Heat Flow

- Main heat flow is through ceramic substrate and out bottom lid through the PCB
- Conductive epoxies allow for secondary flow through top and bottom lids



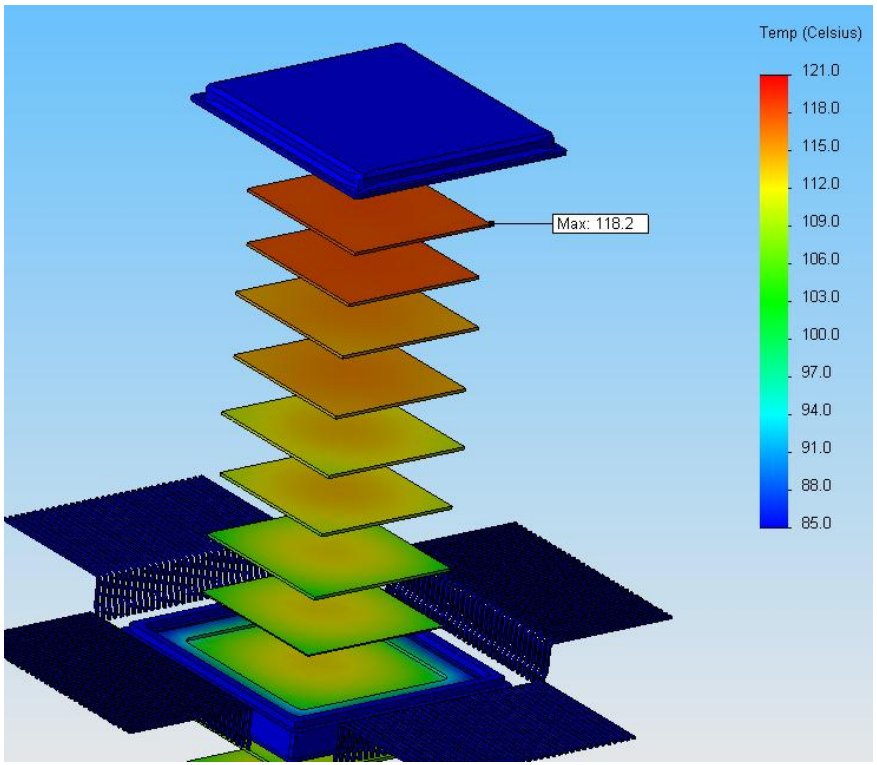
Manufacturing Process Support of Theta-JC

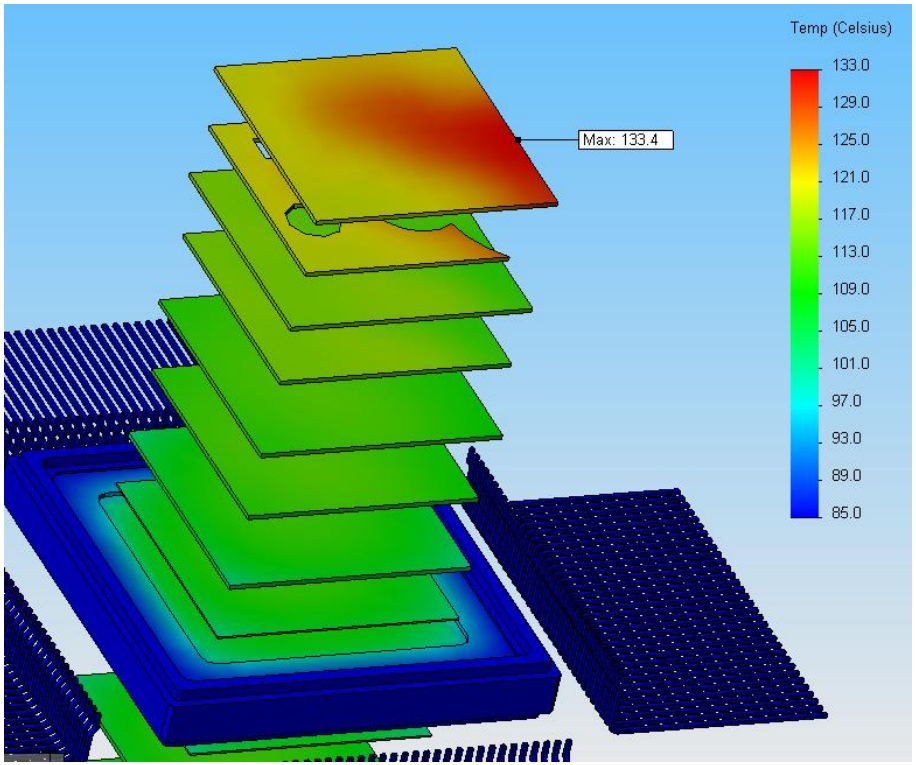
- **Interface Management Consists of:**
  - **Quantity of interfaces**
    - **Epoxy deposition requires spacers with epoxy adhered to each side**
    - **Current process optimizes epoxy deposition and curing flow**
    - **Epoxy preforms eliminate spacers**
  - **Quality of interfaces**
    - **Thick interfaces increase thermal resistance**
    - **Current process dispenses thin, uniform expoxy**
    - **Epoxy preforms reduce thickness and improve thermal conductivity**
  - **Selection of interface materials**
    - **Epoxy preform vs epoxy/silicon/epoxy deposition**
  - **Area coverage of interface**
    - **Elimination of Voids**
  - **Environmental screens and testing used to eliminate substandard device**



The Impact of Interface Voids

- 160 Mb (Dual Cavity MCM, 4-Die Stacked per Cavity)
  - Power Density of 1W distributed over 0.566” x 0.566” die surface
- 50% voiding increases Θ_{JC} 160% over identical stack w/ 0% voiding

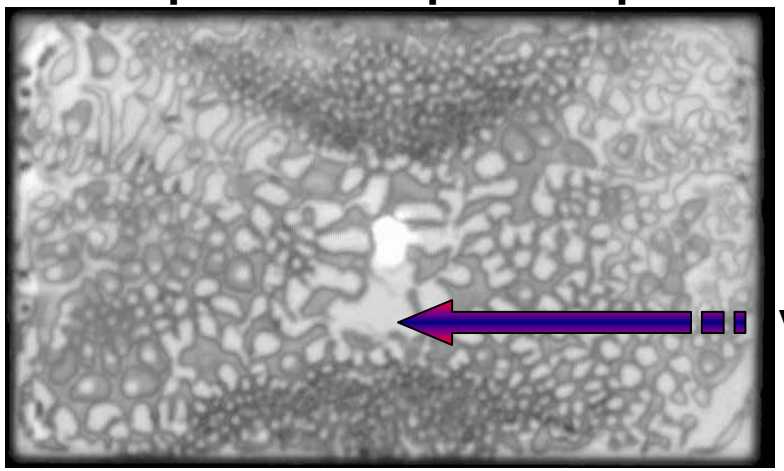




- Theta-JC with 0% voiding:
  - 11.9 °C / W
- Theta-JC with 50% voiding on each bond interface (worst case = 7 I/Fs)
  - 19.3 °C / W

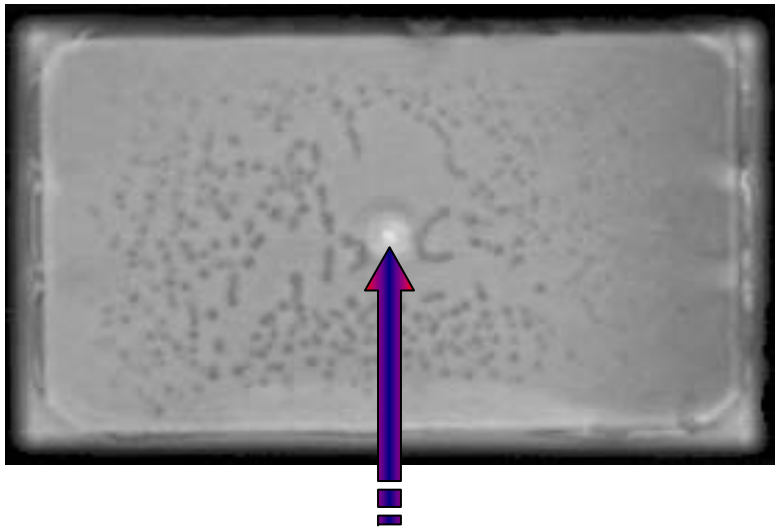
The “Cure” to “Dispensing” with Voids

- Dispense parameters and die placement are important factors in preventing voids
- A proper cure profile is critical to minimize void expansion in the die attach material
- Example of high voiding
  - Caused by improper cure profile and poor dispense



- Because of the large Theta-JC, an accelerated B/I will screen out excessive voiding

- Example of ideal bond interface



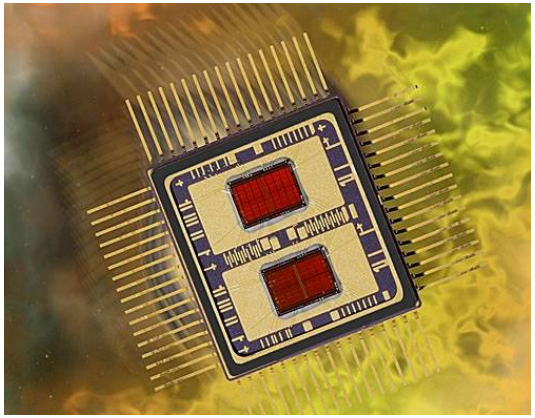
Not a void, but an artifact from the ink dot on test die

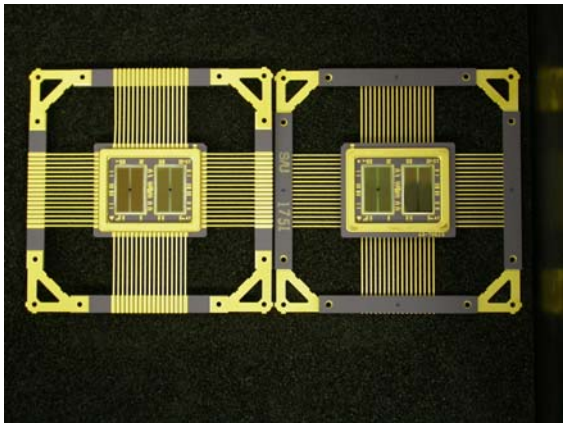
Aeroflex Qualified Memory Solutions

- Aeroflex Colorado Springs has been providing memories for over 20 years
  - Memory solutions – 50 krads(Si) to 300 krads(Si)
  - QCOTS using commercial die to 50 krad(Si)
- Offered as 4-, 8- and 16Mbit options
  - 128K x 32, 512K x 8, 512K x 32 architecture
- In development 32/64/128M and 40/80/160M MCMs
  - 1M, 2M, 4M x 32 and 1M, 2M, 4M x 39
- 3.3V I/O, 1.8V core Dual Source
- 3.3V and 5V Single Source

Aeroflex Qualified Memory Solutions

- **SRAMs**

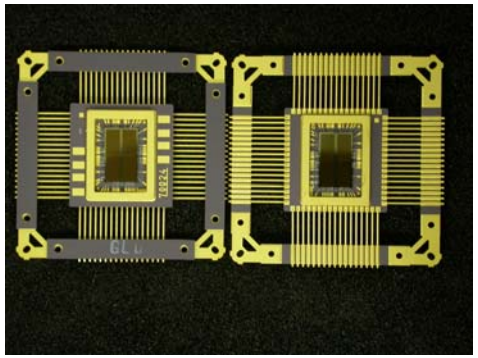


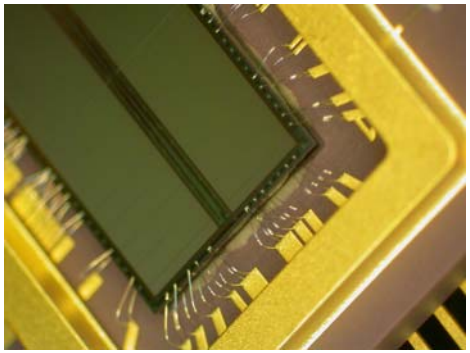


Product	Density Organization	Access Time Read/Write	Dual Supply Voltage	Max Power	Package	Total-dose	Qualification	Notes
UT8R128K32	4Meg 128K x 32	15ns	3.3V I/O 1.8V Core	205mW	68 – lead CQFP	300 krad(Si)	QML-Q, V	12T Cell
UT8R512K8	4Meg 512K x 8	15ns	3.3V I/O 1.8V Core	72mW	36 – lead CFP	300 krad(Si)	QML-Q, V	12T Cell
UT8CR512K32	16Meg 512K x 32	17ns	3.3V I/O 1.8V Core	272mW	68-lead CQFP	300 krad(Si)	QML-Q, V	MCM, 12T Cell, Dual Cavity
UT8ER512K32 (Master or Slave)	16Meg 512K x 32	20ns read 10ns write	3.3V I/O 1.8V Core	588mW	68 – lead CQFP	100 krad(Si)	QML-Q, V	On-Chip EDAC, Monolithic

Aeroflex Qualified Memory Solutions

- SRAMs

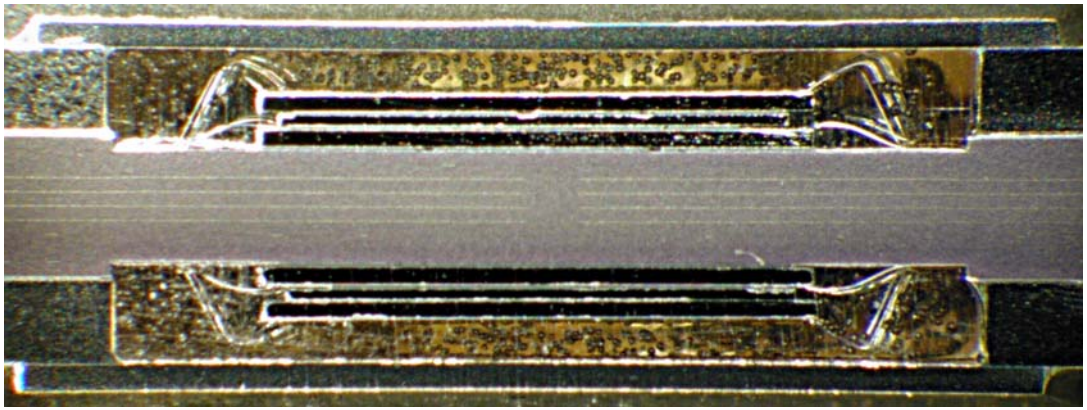


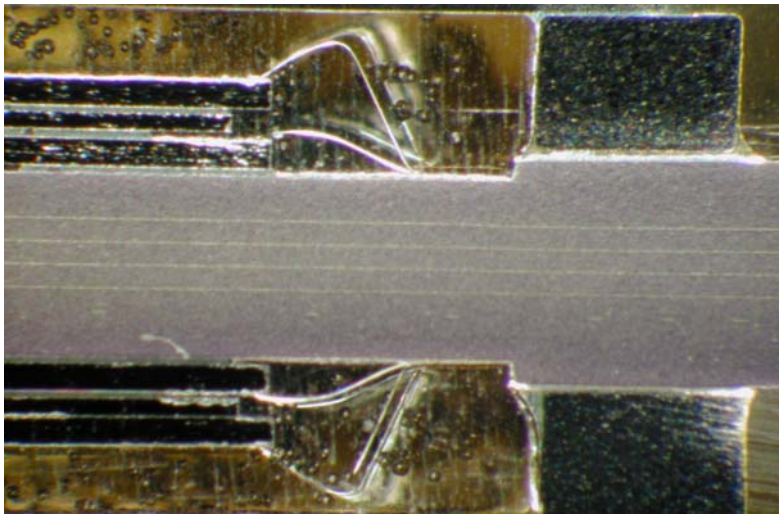


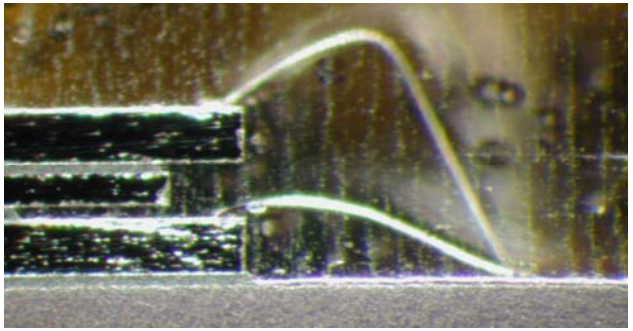
Product	Density Organization	Access Time Read/Write	Supply Voltage	Max Power	Package	Total-dose	Qualification	Notes
UT8Q512E	4Meg 512K x 8	20ns	3.3V	270mW	36 – lead CFP	50 krad(Si)	QML-Q, V	
UT8Q512K32E	16Meg 512K x 32	25ns	3.3V	252mW per byte	68 –lead CQFP	50 krad(Si)	QML-Q QML-V pending	MCM, dual cavity, 2 die stack
UT9Q512E	4Meg 512K x 8	20ns	5V	418mW	36 – lead CFP	50 krad(Si)	QML-Q, V	
UT9Q512K32E	16Meg 512K x 32	25ns	5V	385mW per byte	68 – lead CQFP	50 krad(Si)	QML-Q QML-V pending	MCM, dual cavity, 2 die stack

Stacked Die Package Development

- UT9Q512K32E dual cavity, 2 die stack
- Uses epoxy deposition with spacer
- QML-Q complete, QML-V pending







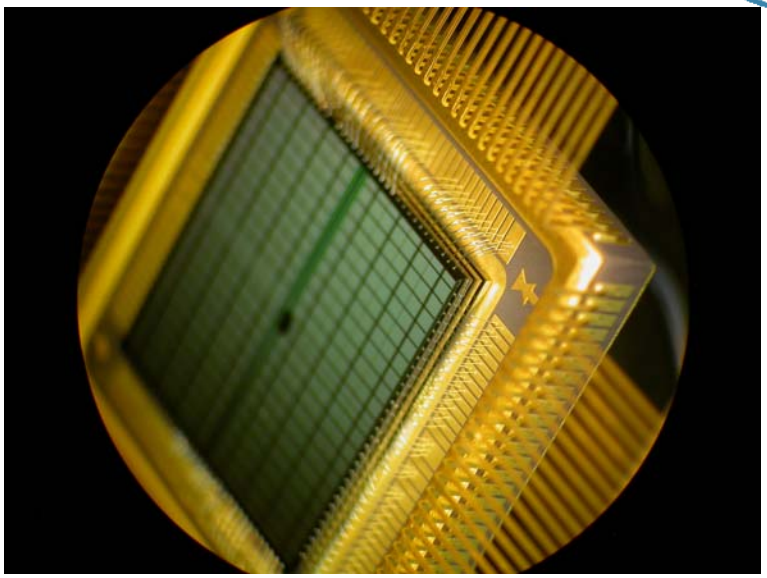
Aeroflex Qualified Memory Solutions

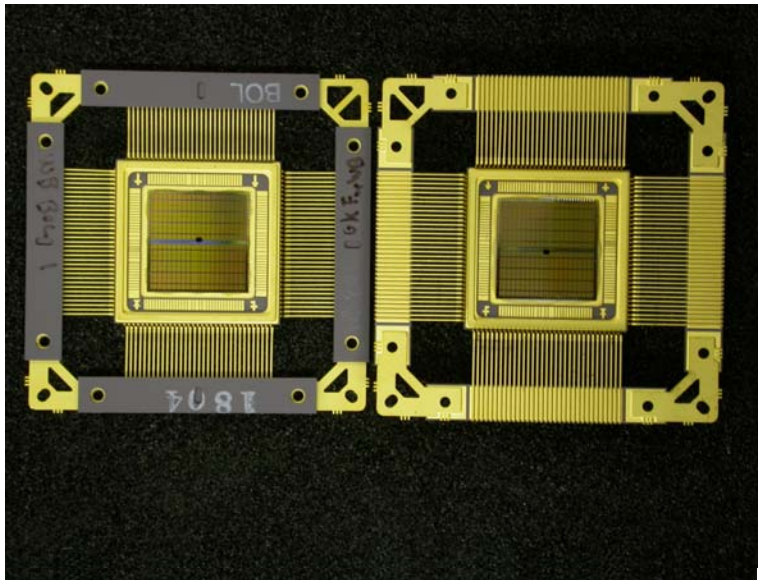
- **SRAMs** In Development

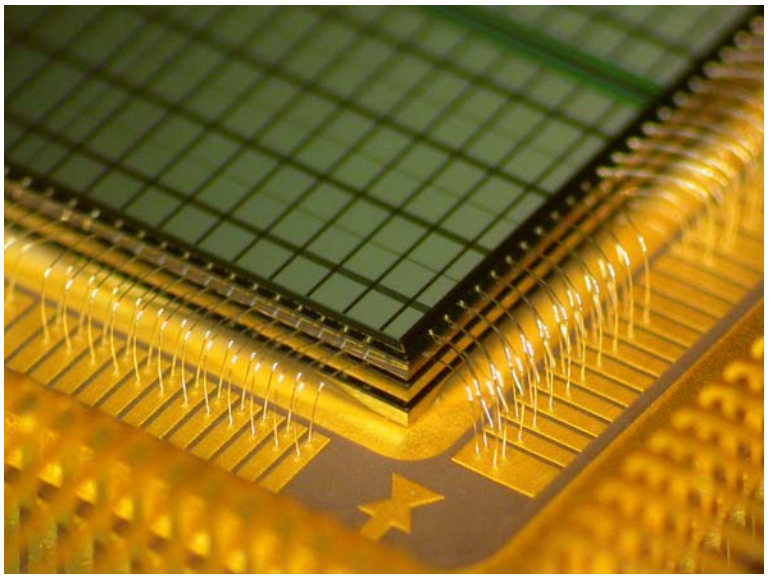
Product	Density Organization	Access Time Read/Write	Dual Supply Voltage	Max Power	Package	Total-dose	Qualification	Notes
UT8ER1M32 (Master or Slave)	32Meg 1M x 32	20ns read 10ns write	3.3V I/O 1.8V Core	540mW	132 – lead CQFP	100 krad(Si)	QML Q409	On-Chip EDAC, MCM, dual cavity
UT8ER2M32 (Master or Slave)	64Meg 2M x 32	20ns read 10ns write	3.3V I/O 1.8V Core	650mW	132 – lead CQFP	100 krad(Si)	QML Q409	On-Chip EDAC, MCM, dual cavity, 2 die stack
UT8ER4M32 (Master or Slave)	128Meg 4M x 32	20ns read 10ns write	3.3V I/O 1.8V Core	870mW	132 – lead CQFP	100 krad(Si)	QML Q409	On-Chip EDAC, MCM, dual cavity, 4 die stack
UT8R1M39	40Meg 1M x 39	20ns read 10ns write	3.3V I/O 1.8V Core	540mW	132 – lead CQFP	100 krad(Si)	QML Q409	MCM, dual cavity
UT8R2M39	80Meg 2M x 39	20ns read 10ns write	3.3V I/O 1.8V Core	650mW	132 – lead CQFP	100 krad(Si)	QML Q409	MCM, dual cavity, 2 die stack
UT8R4M39	160Meg 4M x 39	20ns read 10ns write	3.3V I/O 1.8V Core	870mW	132 – lead CQFP	100 krad(Si)	QML Q409	MCM, dual cavity, 4 die stack

Stacked Die Package Development

- UT8ER4M32 dual cavity, 4 die stack
- Current process uses epoxy deposition with spacer
- Epoxy preforms under evaluation
- QML Qualification Q409







Summary: Stacked Memory Packaging

- **Stacking memory die allows for the highest density solution while maintaining single die performance**
- **Aeroflex implemented manufacturing and assembly flows to address thermal and mechanical issues inherent with stacked die**
  - **Thin bonding interfaces**
  - **Thin ceramic substrates**
  - **Optimized bond shelf width for connectivity**
  - **Optimized bond finger routing to minimize capacitance and inductance**
  - **Dedicated power planes with extensive power pins**
- **Aeroflex minimizes Θ_{JC} for stacked die packaging**
  - **Use of multiple cavities**
  - **Quality and thickness of interfaces between die**
  - **Optimum materials and curing**
  - **Elimination of voids in the die attach process**
- **Aeroflex provides a family of stacked memory die solutions for aerospace applications**