Honeywell Microelectronics:

Functional Verification in Space Applications

Honeywell

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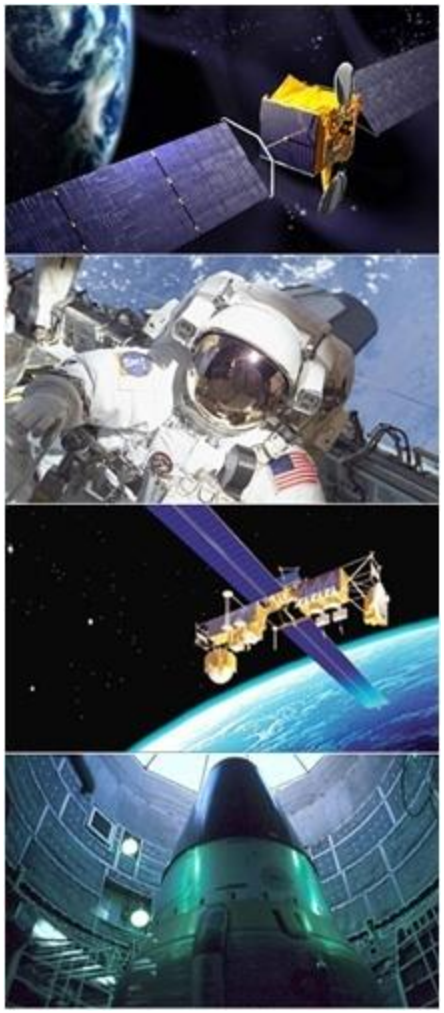
Abstract:
Honeywell Microelectronics designs and fabricates multi-million gate ASICs for Space applications. Mastering the physical implementation and timing closure for first pass success is extremely important, but equally important is first pass functional success. Both are essential to a successful program. If the ASIC correctly implements the netlist and timing, but does not function as required, it may be of little value.

This presentation will review Honeywell's adoption of the latest HDL verification methods and techniques and how they benefit the Space engineering community. Starting with a detailed requirements review, architecting the test bench and defining acceptable scoreboard coverage, the verification process for space applications is extremely rigorous. An engineering change to correct a 10 million gate ASIC can cost millions of dollars and many months of schedule delay. Devices that successfully meet all requirements, the first time, are essential to meet budget, schedule and program targets.



Verification of ASICs & FPGAs for Space

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- **Honeywell provides nanometer Radiation Hardened multi-million gate ASICs for space applications.**
- **ASIC and FPGA designs for space are critical to the overall success of the mission.**
  - **They are expensive and engineering intensive and therefore require an extremely high level of design assurance.**
- **The purpose of functional verification is to assure that the HDL design functions correctly as required by the system.**

- **Space ASICs are key components of systems costing 100's of millions of dollars.**
- **<u>The risk of a design error must be reduced as completely as possible.</u>**

What is the program impact of HDL Verification?

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- **Complex designs have a large operational state space to verify**
  - **Think exponential as size increases**
- **Complex designs can require man-years and special software to verify**
  - **Adversely affects scheduled completion.**
- **The intensive verification effort can easily exhaust in house resources.**
  - **There are high staffing and training costs.**
- **Design consultants may lack experience, availability and commitment.**
- **<u>The cost of a Space ASIC or FPGA design error in time and dollars lost must be avoided.</u>**

There are several stages of verification evolution

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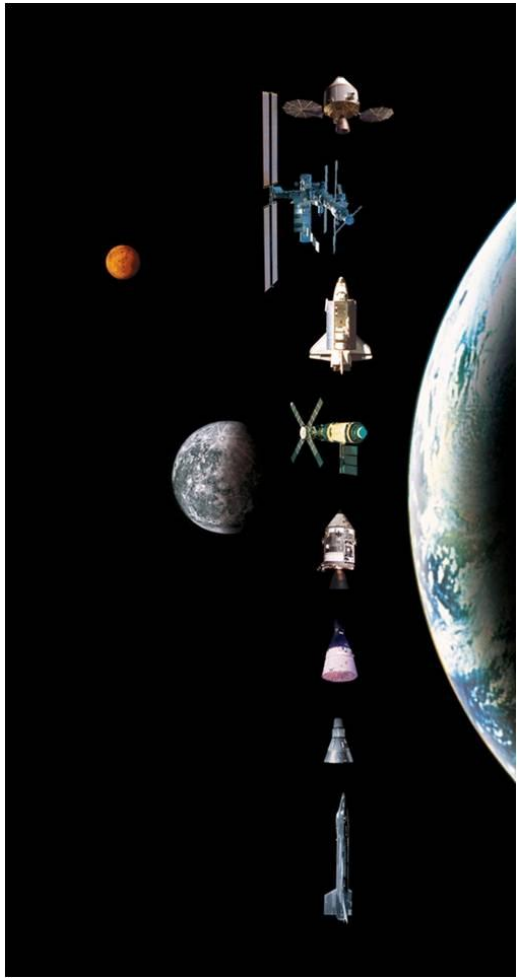
- **The Cross Your Fingers method**
  - Just code it up and throw out bit maps and programming files
- **The Force File stage**
  - You write elaborate scripts to both generate input and check the output
  - Your designs were still reasonably small, so you are able to fully verify it
- **The Bus Functional Model (BFM) stage**
  - The input files for tests become much smaller
  - The BFM is at least smart enough to check the line protocol itself
- **The Self Checking stage**
  - Your BFM's have developed some sort of pseudo-language to drive them
  - You have developed enough input to instruct the BFM on what it should be seeing and to flag errors
- **The C/FlexModel/SmartModel stage**
  - Your Pseudo language of the BFM's is now rivalling C.
  - You are lured by the power of someone having done most of the work (reuse)
  - You now focus on cranking out test after test
- **The Constrained-Random, ABV, OVM stage**
  - You realize that you are looking at a 1M+ gate design that is a verification nightmare.
  - You know that verification of the design will take thousands of tests
  - There is limited time and money in the schedule
  - You need a flexible, powerful, easy to use methodology
- **OVM Provides A Platform For Verification Infrastructure With A Common Methodology For Multi-site Projects**



How does OVM & SystemVerilog help me?

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- **Every verification task is different.**
  - **The flexibility of an advanced verification language is required**
- **Multi-Million gate designs can be verification nightmares.**
  - **The power of an advanced verification language is required**
- **You want to do everything with one language**
  - **SystemVerilog provides design and verification support.**
- **You need a complete methodology**
  - **Support software like Mentor's Questa simulator provides verification project management as well as support and execution**
  - **OVM provides access to various methods of verification beyond a single vendor.**

Why use OVM & SystemVerilog?

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- **SystemVerilog is a Hardware Description and Verification Language based on Verilog**
  - The language provides an Object-Oriented Programming Model
  - It has backwards compatibility with Plain-Old-Verilog (POV)
  - SystemVerilog has effectively utilized everything good from VHDL
- **SystemVerilog for Verification provides "Transaction" Level Modelling (TLM)**
  - Emphasis is on data being transferred and not on the implementation of the transfer
  - Data is defined as attributes of a class object
  - Objects are passed between components
  - OVM provides this functionality
- **Object-Oriented Features:**
  - Single-Inheritance (Software Interfaces)
  - Polymorphism features similar to C++ (Virtual Methods)
  - Classes can be type-parameterized (Specialization, Generics)
- **Constrained Random generation of stimulus**
- **SystemVerilog Assertions (SVA)**
- **Functional Coverage Collection**
  - Can be single, multiple and/or complex combinations of attributes
  - Very well suited to packet based designs

Honeywell's Pre-System Verilog History

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- As early as 2000, it was apparent designs had approached the point where our directed testing strategy was inadequate.
  - Verification teams were getting larger
  - Hundreds of tests were needed, involving much maintenance
- At that time the constrained random software market was dominated by Specman (E) and Vera.
  - We performed a trade-study and a selection between the two
  - An initial verification port of a "verified" design was done
  - E was chosen as our going forward language
- We attempted to use Specman (E) on a large project with mixed success.
- Working with a major design consulting company yielded communication problems and little added experience to Honeywell's HDL engineering community.

Honeywell's History (Cont.)

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- After a large design re-baseline, we had the opportunity to start over with something different.
  - At this time SystemVerilog had been ratified and was gaining support
- The Honeywell team selected the SystemVerilog language and its features
  - It is very integrated into the logic design flow
  - It is like hardware and software languages
  - Mentor's Questa platform is used for SV execution.
- We have trained every Honeywell ASIC/FPGA HDL designer using our own SV materials and instructors
  - We have taken a wide variety of classes from other sources and we were not satisfied
  - Over 150 HDL engineers trained

Honeywell's Verification Support Team

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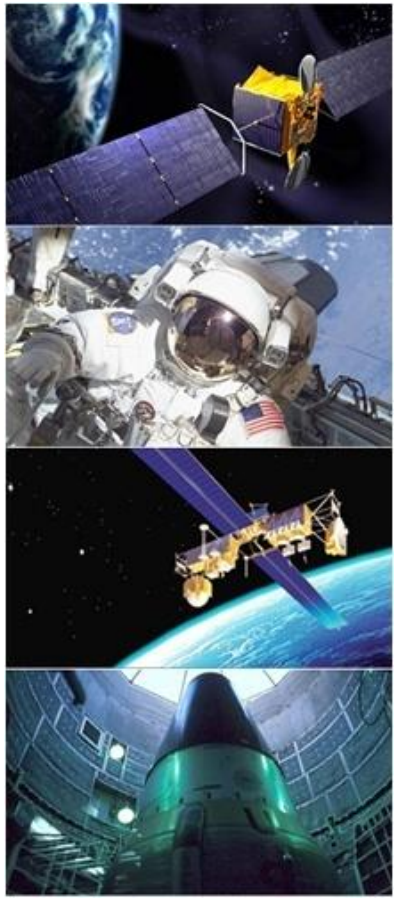
- **We have experience using SystemVerilog Verification on large designs. Examples:**
  - Currently working on multiple Million+ logic gate ASICs (with SerDes) as part a 10+ chip system
  - Have revisited previously verified designs using SV techniques and found undiscovered errors!
  - Have verified commercial established IP using SV techniques and found undiscovered errors!
- **We offer help to our customers with the verification of large HDL designs**
  - Turnkey verification from requirements
    - Test plan creation
    - Test environment creation
    - Test coverage/ scoreboard
  - Teaming with customer's engineering for schedule reduction



RTL Verification Flow with OVM

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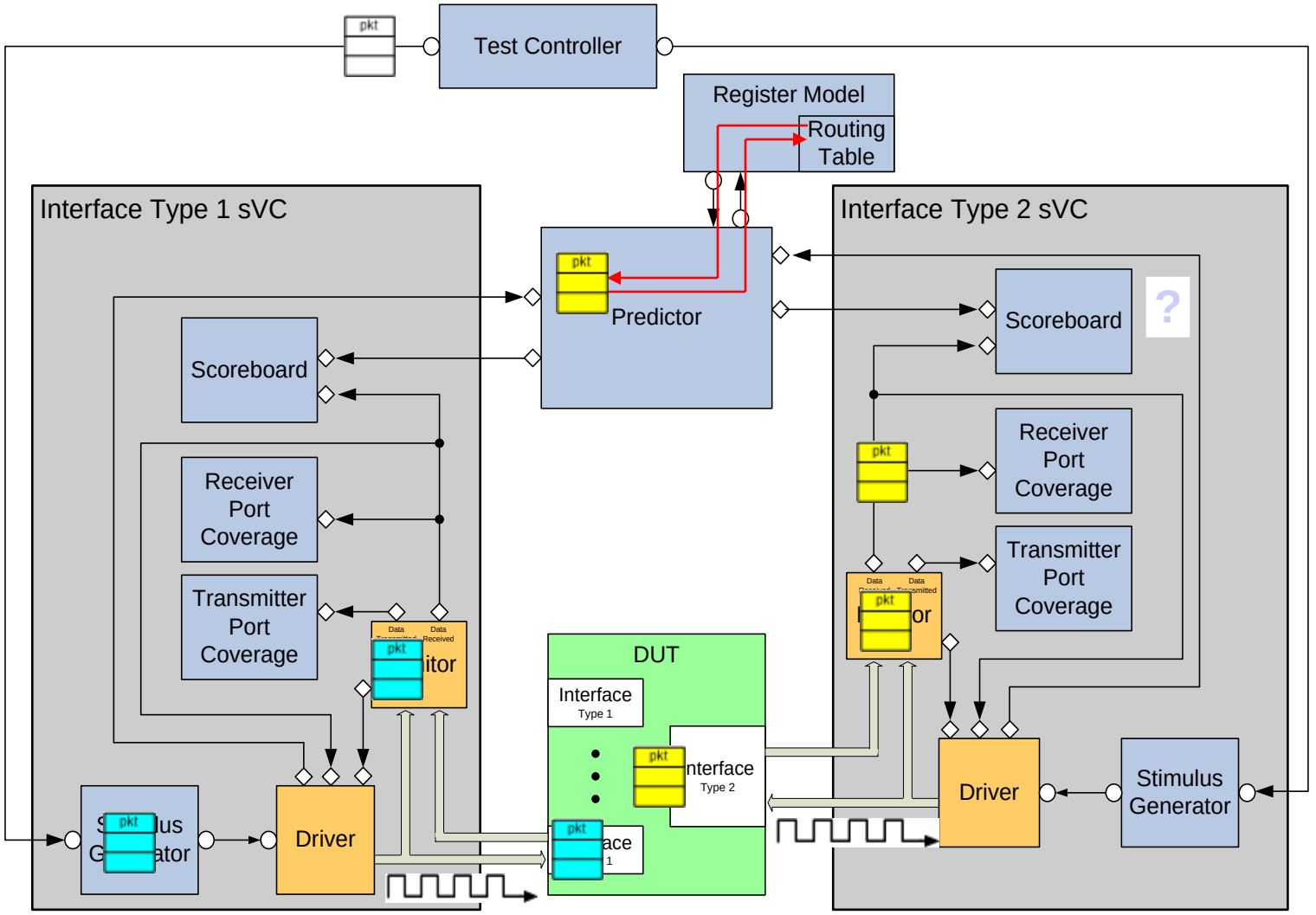

Thank You for Your Attention

For more information contact:
Gary Roosevelt
gary.roosevelt@honeywell,com
(727) 539-3195

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