Thermal Cycling Characterization of Complementary Heterostructure Field Effect Transistors (CHFETs) Test Report

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Background

Complementary heterostructure field effect transistor (CHFET) is an advanced GaAS based IC technology that offers up to 4x higher speed and 6x lower power dissipation than silicon based CMOS technology. The CHFET technology was developed by Honeywell SSEC for DOD applications and according to the manufacturer, additional features include CMOS like design flexibility with complementary N-channel and P-channel FETs), high switching speed (multi-GHz), wide operating temperature range (4°K to 400°C), and inherent radiation hardness. These features made the CHFET an attractive candidate for potential use by JPL X2000/Europa Oribter project. Honeywell SSEC provided JPL X2000 project with several wafer lots of CHFETs. In order to space qualify these CHFETs, DC/RF life testing was proposed by JPL as part of NEPP task requirements, where as GSFC was to focus on thermal cycling characterization of these devices. Several sample devices (chips in bare die form) were sent to GSFC for thermal cycling.

Test Description

The major activities that were performed as part of thermal cycling (TC) of CHFETs, with the goal of device space qualification, are listed below.

1. A litereature search was conducted to determine, what test results had previously been reported that were related to the thermal cycling of CHFETs. During the search, approximately 40 references were found through the NRL Library system, and the Honeywell CHFET web site was also reviewed. The information gathered from these references was helpful in generating the test plan for CHFET devices supplied. Although, Honeywell provided very little background information about their proprietary process, the literature search revealed that the CHFET structure had been developed with a $Al_{0.75}GaAs/In_{0.25}GaAs/GaAs$ structure, which was suitable for commercial digital integrated circuits applications.

2. CHFET chips fabricated by Honeywell for the X2000/Europa Orbiter project were electrically characterized prior to thermal cycling. These chips, contained many individual CHFETs with common gates that were all connected. Figure 1 shows a representative CHFET device from the "drain" end.

   Each bare die contained 38 columns of FETs, with 5 pairs of source and drain contact pads per column, and interconnected gate contacts at the top and bottom of each column. Two of the chips that were sent to GSFC had large die cracks, and were used for preliminary testing. A total of eight (8) individual CHFETs were electrically characterized, with at least 2 devices from each chip. One bare die was used as a control sample before and after the TC tests, throughout the TC test sequence.

3. CHFET chips that had been electrically characterized were placed in a thermal control chamber and TC performed, according to the NASA GaAs MMIC Reliability Assurance Guideline for Space Applications (JPL Publication 96-25, 15 December 1996, p. 164). The chips were cycled between –65°C and 200°C for a total of

15 cycles. One chip was held back as a control and was not temperature cycled. As stated in the guideline, packaged devices are normally used for the TC test "to detect flaws or weak point in the die attach, wire bonds, and package seals that would normally result in early failures." However, there are also thermal/mechanical stresses between the metallization and the semiconductor layers, and between the heterojunction semiconductor layers. No information was available about the intended application and/or packaging scheme for these parts. Therefore, the objective of TC was to evaluate any degradation effects at the chip level.

4. After the thermal cycling tests were completed, the pre- and post- TC electrical measurements were performed, and any changes in electrical characteristics were noted. Failure was defined as a 20% change in the drain current, gate leakage current, or threshold voltage measurements.

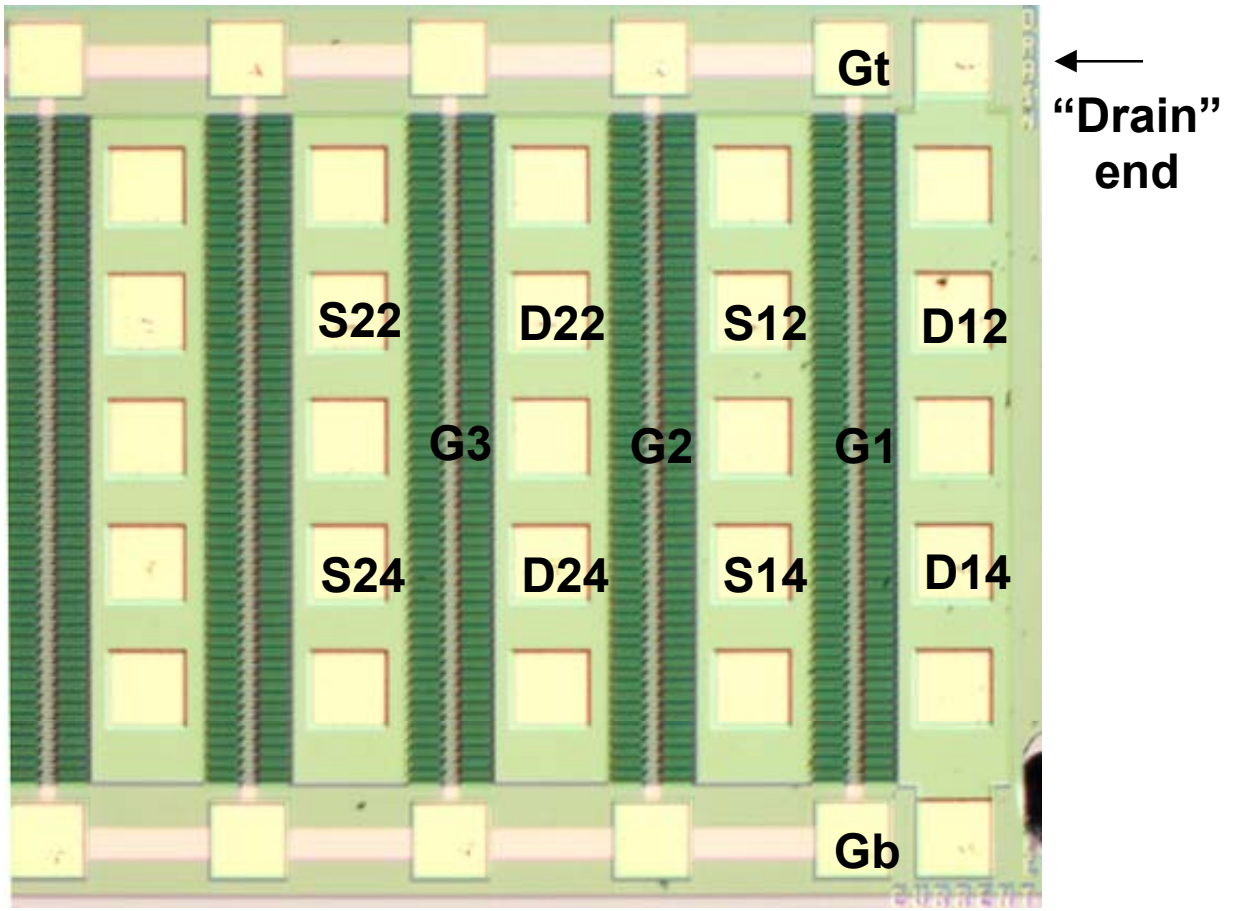

Figure 1. Drain end of a CHFET bare die at 50x magnification. D## = Drain/column #/row #; S## = Source/col.#/row#; G# = Gate column #; Gt/b = Gate top/bottom.

Test Results

Table 1 shows pre- and post- thermal cycling electrical characteristics NPN transistors for (a) Seven CHFET chips that were actually thermal cycled, and (b) One control CHFET chip. Table 2 shows pre- and post- thermal cycling electrical characteristics PNP transistors for (a) Seven CHFET chips that were actually thermal cycled, and (b) One control CHFET chip. Both tables show the test conditions and limits. The last column of the tables show drain current pre- and post- cycling (Iu – Ic) 20 % max allowable change limit and actual change (%). Figure 2 shows typical drain current characteristic curves for a NPN transistor (a) Before cycling, and (b) After cycling. Figure 3 shows typical drain current characteristic curves for a PNP transistor (a) Before cycling, and (b) After cycling.

It should be noted that for all seven devices, the change between uncycled and cycled saturated current was less than the 20% failure criteria. Therefore, all devices were considered as passing the established failure criteria limit.

		NPN Id @ Vds= 2.5V, Vgs= 0.6V (mA)			Drain Current (Iu – Ic)	
SAMPLE	**DEVICE**	**Uncycled (Iu)**	**Cycled (Ic)**	**(Iu –Ic)**	**20%max allowable change (mA)**	**Actual change (%)**
1	D1	330	285	45	66	-14
1	D20	330	330	0	66	0
2	D1	320	330	-10	64	3
2	D20	330	330	0	66	0
3	D1	315	315	0	63	0
3	D20	330	350	-20	66	6
4	D1	310	320	-10	62	3
4	D20	345	375	-30	69	9
5	D1	400	360	-40	80	-10
5	D20	425	425	0	85	0
6	D1	380	345	35	76	-9
6	D20	435	410	25	87	-6
7	D1	375	360	15	75	-4
7	D20	410	410	0	82	0

Table 1(a). Table of NPN electrical characteristics pre- and post- thermal cycling for seven CHFET chips.

	CONTROL SAMPLE 8: D12G1T			
	NPN Id @ Vds= 2.5V, Vgs= 0.6V (mA)			
Cycling Samples	**Before Cycling (Ib)**	**After Cycling (Ia)**	**Ib-Ia**	**Ib - Ia Change (%)**
Sample 1	325	325	0	0
Samples 2,3,4	325	330	-5	2
Samples 5,6,7	330	350	-20	6

Table 1(b). Table of NPN electrical characteristics for the control CHFET chip.

PNP I @ Vds= 0.8 Vgs=0.8V (mA)	Drain Current (Iu-Ic)

SAMPLE	DEVICE	Uncycled (Iu)	Cycled (Ic)	Iu -Ic	20%max allowable change (mA)	Actual change (%)
1	D1	250	*	*	50	*
1	D20	200	190	10	40	-5
2	D1	225	225	0	45	0
2	D20	230	200	30	46	-13
3	D1	200	225	-25	40	13
3	D20	150*	*	*	30	*
4	D1	215	225	-10	43	5
4	D20	150*	*	*	30	*
5	D1	210	200	10	42	-5
5	D20	205	210	-5	41	2
6	D1	230	275	-45	46	20
6	D20	245	255	-10	49	4
7	D1	220	210	10	44	-5
7	D20	230	200	20	46	-9

*Insufficient data--could not be measured accurately

Table 2(a). Table of PNP electrical characteristics pre- and post- thermal cycling for seven CHFET chips.

	CONTROL SAMPLE 8: D12G1T			
	PNP Id @ Vds= 0.8V, Vgs=0.8V (mA)			
Cycling Samples	Before Cycling (Ib)	After Cycling (Ia)	Ib-Ia	Ib - Ia Change (%)
Sample 1	200	215	-15	8
Samples 2,3,4	215	205	10	-5
Samples 5,6,7	205	230	-25	12

Table 2(b). Table of NPN electrical characteristics for the control CHFET chip.

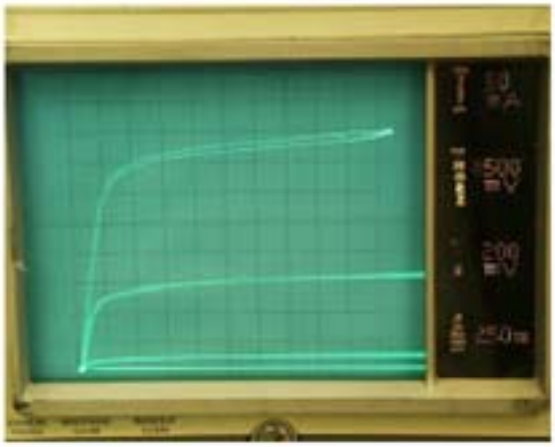

Figure 2a. Device #7 (7UD12G1T) npn characteristics before cycling.

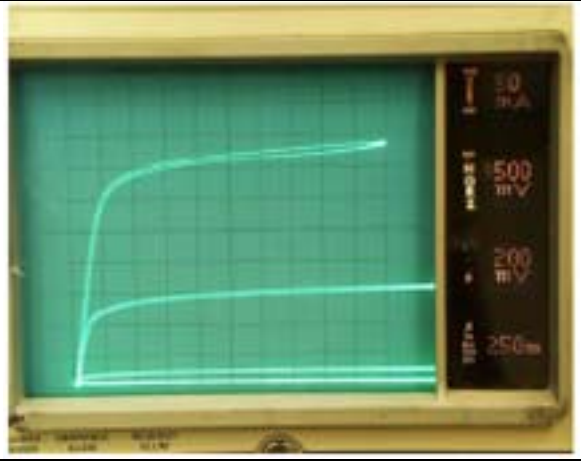

Figure 2b. Device #7 (7UD12G1T) npn characteristics after cycling.

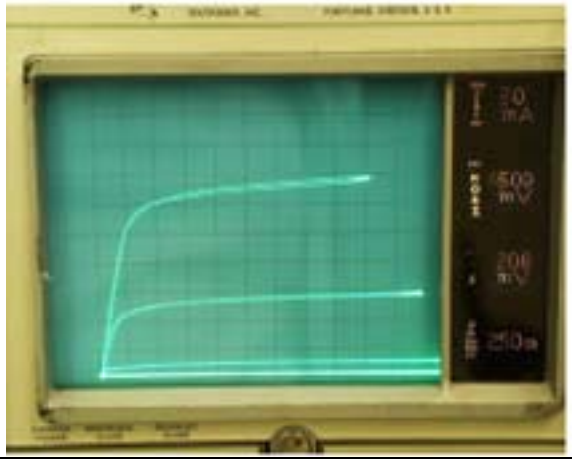

Figure 3a. Device #8 (8UD12G1T) npn characteristics before cycling of chips 5, 6, and 7

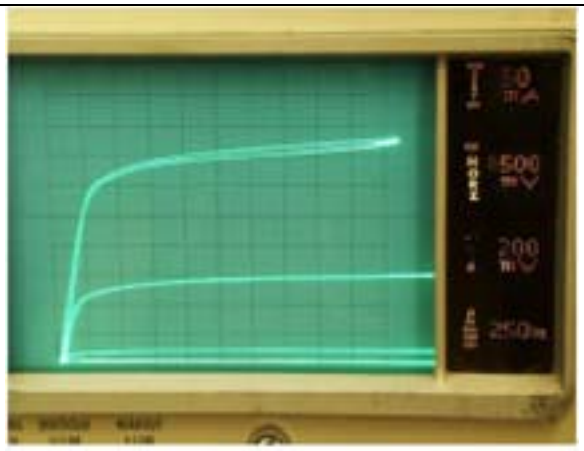

Figure 3b. Device #8 (8UD12G1T) npn characteristics after cycling of chips 5, 6, and 7

Summary

Complementary heterostructure FET (CHFET) chips manufactured by Honeywell SSEC and intended for usage in X2000/Europa Orbiter projects were supplied to GSFC for thermal cycling characterization testing. These chips contained several NPN and PNP transistors. A total of eight chips were electrically characterized with at least two devices from each chip. One bare die was used as control sample for before and after the TC testing. The devices were cycled between –65°C and 200°C for a total of 15 cycles, in accordance with NASA MIMIC Reliability Assurance Guideline for Space Applications. Failure was defined as a 20 % change in the pre- and post- TC for drain current, gate leakage current or threshold voltage. The pre- and post-thermal cycling measurements showed all test devices meeting this criteria, and were considered as passing. No signs of device degradation were observed during optical inspection after the completion of thermal cycling.

Acknowledgements

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