Total Dose and Single Event Effects Testing of the Intel Pentium III (P3) and AMD K7 Microprocessors

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***Abstract* – To understand the radiation sensitivity and radiation response, Intel Pentium III and AMD K7 microprocessors were tested for total ionizing dose and single event effects. The processors have been found to be extremely tolerant to total ionizing dose and no radiation-induced latchups have been observed with protons or heavy ions to an LET of approximately 15 MeV-cm^2/mg. Single event upset and functional interrupts have been observed with both protons and heavy ions.**

I. Introduction

Many future NASA missions will require extensive on-board computation capability. The issue that this raises is the availability, cost and capability of currently available radiation hardened or radiation tolerant microprocessor systems. Radiation hardened computers systems are often costly and are actually two or three generations behind in computational capability. Also, the feasibility of a given mission may require state-of-the-art (SOTA) capability.

To confront these issues, NASA has the Remote Exploration and Experimentation Project (REE). The goal of this project is to transfer commercial supercomputer technology into space using SOTA, low power, non-radiation-hardened, commercial-off-the-shelf (COTS) hardware and software to the maximum extent possible [1].

As part of this project, work was done to evaluate the radiation response of the Intel Pentium III (P3) and AMD K7 microprocessors and their associated bridge chips. This paper will report of the total dose response (both proton and cobalt-60) and single event effects (proton and heavy ion) observed to date.

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II. Test Hardware

A. Hardware Overview

The test hardware setup consists of two computer systems. The first computer system contains the Device Under Test (DUT) and is referred to as the DUT Computer. The second computer system is a Peripheral Component Interconnect (PCI) Extensions for Instrumentation (PXI)–based computer that is used to control the testing. It is referred to as the PXI Test Controller. A simplified block diagram of the test hardware is shown in Figure 1.

Figure 1 is divided into three regions defining the three distinct physical locations during the testing. The DUT and DUT computer reside in the beamline area with the DUT elevated using an extender card to place on the DUT in the radiation beam. The PXI Test Controller needs to reside in the vicinity of the DUT Computer but must be shielded from even scattered radiation. The final area is the User Area where the users and all the monitors and input devices reside for actual execution of the testing.

B. DUT Computer

The DUT Computer, operating the DUT processor, is entirely COTS–based. All components that make up the DUT Computer are purchased from commercial vendors and are components that can be found in any desktop computer system. The DUT, a commercial processor, modified for beam access and heat removal, resides on a motherboard designed for a desktop system. A local floppy or hard drive is used for the boot and test executive software loading.

Additional modifications are needed to assist in the testing process. First, a short processor extender board is placed in between the DUT card and the

motherboard. This improves the beam access and provides a method for sampling of the 7 currents and voltages (one is a monitor of the die temperature). Figure 2 shows the schematic of the extender card for the extraction of these values.

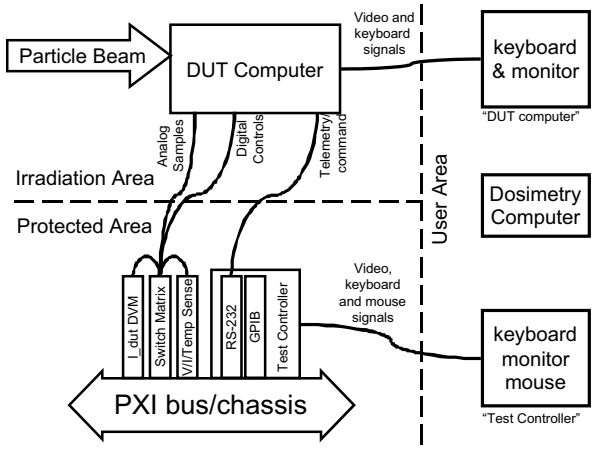

Figure 1. Block diagram showing the key features of the hardware setup for the testing.

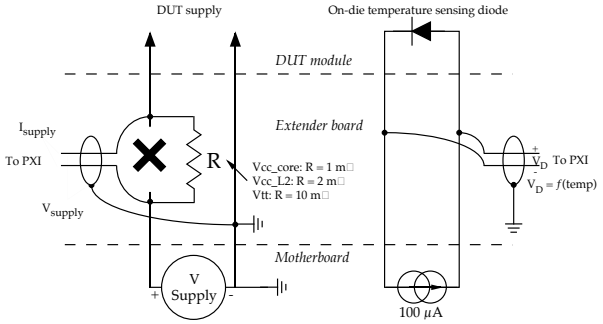

Figure 2. Simplified drawing showing the methodology used to extract the seven voltages and currents via the extender card.

Secondly, on/off and reset are configured to allow for remote control via the motherboard's front panel control connections. Similarly, the power supply is tapped into to provide an override OFF control.

Finally, the video, keyboard and RS-232 are extended to the User Area. Processor state information, (telemetry), is output to RS-232 and video, however information during boot is not available to the serial port, so video is required to observe this process.

One additional piece of hardware is used. That is a memory card that is located the DUT Computer's PCI bus. It receives the exact same telemetry sent to the RS-232 bus to give one more backup of the telemetry for increase data collection reliability. A block diagram showing this DUT Computer hardware setup is shown in Figure 3.

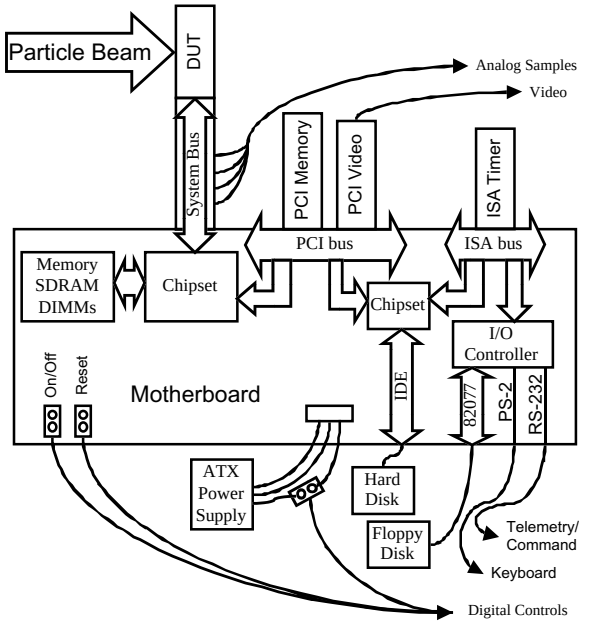

Figure 3. Block diagram showing the DUT computer hardware setup for the testing.

C. PXI Test Controller

The PXI-based Test Controller consists of a PXI chassis and its associated cabling. Within the PXI chassis resides an embedded Pentium III based controller (running Win98, Labview™ environment, and a custom Labview™ application), a signal switch matrix, and two digital multimeters (DMMs) in the voltage measurement mode. The switch matrix provides two functions: the multiplexing of analog signals to one of the DMMs and contact closures (pulling signal levels to ground). The other DMM is dedicated to monitoring one specific analog value and measuring that without regular periodic switching so that it may measure more frequently.

The cabling from the PXI subsystem to the user area includes the keyboard/monitor/mouse extension, a network connection for data file access, and power (in the case that the PXI system requires a hard power cycle). The system cabling includes cables between the PXI and the DUT Computer, cables between the PXI chassis and the user area, and intra-subsystem cables. The intra-PXI cabling includes only the cables from the switch matrix to the adjacent DMM modules.

The custom Labview™ application is a Graphical User Interface (GUI) that allows for the control of the DUT Computer, control of the PXI Controller, and data from the DUT (including display of voltage/current strip charts, raw telemetry, and processed telemetry in the form of error counters). This GUI allows for complete control of the testing from the user area, so that DUT access is only required when test hardware changes (e.g., new DUT) are needed.

III. SOFTWARE

A. Test Software

The DUT software is executed using the Pharlap Real-Time Operating System (RTOS), with pre-emptive task switching turned off. The DUT software is compiled in Microsoft Visual C++ with a Pharlap Linker add-in. The tests are written in a combination of C and assembly language. Assembly language is needed as the Pharlap RTOS was designed for an x86-based processor. Commands needed to execute Pentium III specific code must therefore be written in assembler.

There are eight tests available for testing the P3/K7 components. Each test sends a keep-alive at approximately a one hertz rate (0.1 Hz for test H) and sends error results as they occur. One test is selected for each exposure to the beam and the software repeatedly performs the test until a pre-determined dose/fluence is reached or the software stops communicating to the user (indicating a functional interrupt event). The tests are as follows:

A. *Register Test* – Test A sets five CPU registers (ebx, ecx, edx, ebp, and edi) to a baseline value of 0AAAAAAAAH then continuously checks to see if any of the register values change. If any values change, an error is reported to the user and an attempt is made to reset the register to its baseline value. The register is read again to form a new baseline value. The error report includes the register that changed, the value it changed to, the baseline before the error and the baseline after the error. The test then continues. At each keepalive the baselines are reset to 0AAAAAAAAH.

B. *Coprocessor Register Test* – Test B performs 5 math coprocessor functions checking after each to see if the results are as expected. If any results are not as expected then the function producing the result, the result and the expected result are reported to the user. This test transfers the operands before each operation.

C. *Cache and Memory Test* – Test C performs a memory test or cache test. If the cache is turned off it performs a memory test otherwise it performs a cache test. If the cache is on, the cache is temporarily turned off, the memory is loaded with an incrementing pattern and the cache is turned back on before entering the test. The entire range is loaded with a baseline of 0AAAAAAAAH. The range is 100000 words for the memory test and the L1&L2 cache test and 7500 words for the L1 only test. The memory is checked word by word. After each word is checked, its value is changed to the bitwise complement of the baseline. If the value is not as expected then an error is reported and an attempt is made to reset the value to the baseline. The error report includes the location address, the value read, the baseline and the value after attempting to reset to the baseline. If the value can not be restored to the baseline, then checking is disabled for that location until the next keepalive. After the entire range is checked, the baseline is changed to its bitwise complement and checking starts again from the beginning.

D. *Thread Test* – Test D launches seven subthreads each with a counter that is reset to zero. Each thread increments its counter if the counter is less than 11 and then passes control to the next thread. The main thread then checks after 50 milliseconds to see if all of the counters have reached 11. If not an error is reported to the user. The test repeats continuously.

E. *Instruction Cache Test* – Test E runs through 16K of instructions repeatedly. The instruction sequence is to increment the eax register from 0 to 3 checking in between each increment to see if the value is as expected, then to decrement the eax register 3 times and check to make sure it returns to zero. Any errors are reported to the user and the cache is invalidated.

F. *Coprocessor Logic Test* – Test F continuously performs the following math coprocessor operations:

cos(cos(cos(sin(sin(sin(sqrt(sqrt(sqrt(sqrt(sqrt(a*b))))))))))))

where a=0.123456789 and b=0.987654321

The result is checked and any errors are reported to the user with the actual and expected results. This test copies the two operands for the multiply operation but does not perform any other data transfers before a result is obtained.

G. *MMX Unit Test* – Test G continuously performs four MMX functions (pxor, por, pmul and pmulh) and four Streaming SIMD functions (padds, addps, divps and mulps) checking after each to see if the result is as expected. Any errors are reported to the user with the result and the expected result.

H. *Timer Card Test* – Test H measures the passage of time in CPU cycles against the ISA bus clock of 8.33MHZ. A timer board has been set up to provide an interrupt every 16383 cycles of the ISA bus clock. Five thousand samples of the number of CPU cycles between interrupts are recorded and sent to the user after the test is complete in about 9.8 seconds. Then another test is started. This test is used in full functional testing and TID testing.

B. Analysis Software

The data sets that are generated from Single Event Testing, due to the large test matrix, contain enormous amounts of data. It became necessary to generate software to deal with these large data sets to analyze the data under all the test conditions. A database form was chosen as the best form for this analysis. The database initially reads all of the test conditions, then allows to user to scan through the telemetry files (both serial and memory card). The user marks locations within the telemetry files with error annotations that are then stored in the database with those associated test conditions. An example of the errors that can be reported for Test A are shown in Table I. A similar table exists for all tests described above and for errors that are independent of the test software.

After each telemetry file has been annotated, the database can be queried via Structured Query Language (SQL) commands to extract only those conditions wishing to be analyzed. Depending on the detail of the SQL commands, either the event rate (or cross section) can be calculated directly or the selected data from the database can be exported in tabular format for other software to continue the analysis.

TABLE I
PENTIUM TEST ERROR INTERPRETATION TABLE

Test	Error Reported	Possible Causes
A Register Test	Miscompare with data different	Specified register bits flipped
		Alias/Scratch register bits flipped
		Arithmetic unit bits flipped
		Data cache bits flipped
	Miscompare with data the same	Instruction cache bits flipped
		Arithmetic unit bits flipped
		Instruction pool (ROB)/Centralized Scheduler bits flipped

IV. TEST METHODOLOGY

With the extremely complex nature of these microprocessors, an understanding of the test methodologies used is required. This section describes those methods for both the TID and the SEE testing that has been done. A discussion on the thermal considerations needed for these high power processors and a discussion on the die penetration issue for heavy ion testing is also included in this section.

1) TID Test Process

To completely characterize the P3/K7 DUT for TID effects requires numerous parametric measurements, too numerous to measure without test equipment beyond the scope of this project. This level of characterization is not necessary for the needs of this project. To this end, it is sufficient to monitor the voltages and currents to the microprocessor, the instruction timing (to monitor the processor for timing critical operations), and microprocessor functionality.

This total ionizing dose response included exposure to protons and to Cobalt-60. Proton testing was carried out at the Indiana University Cyclotron Facility (IUCF) using 198 MeV protons incident on test structure with fluxes ranging from 10^6 to 10^9 protons/cm^2/sec. This proton TID testing was done in conjunction with the proton SEE testing. Cobalt-60 testing was done at the GSFC Radiation Effects Facility (REF) with dose rates ranging from 3 to 10 krads(Si)/day.

To accomplish the measurements mentioned above, the same test hardware that is used for SEE testing. For biased testing, the entire motherboard assembly is placed in the Cobalt chamber with all but the DUT heavily shielded. For unbiased testing, the DUT is placed in a test jig with grounded pins and removed from the chamber periodically into the full test setup for data collection.

Data collection consists firstly of the seven voltages and currents available through the extender card. Secondly, the DUT is fully exercised utilizing all the tests described in the software section. Finally timing is monitored using a measurement of the access time of a data line and through the use of the Timer Card hardware and software.

2) Single Event Effects Test Process

The SEE test process includes methods to test for all aspects of single event effects (latchup, functional interrupts, upsets, etc.). As a number of these effects are sensitive to the software being run and may be sensitive to numerous other conditions, detailed control of the Device Under Test is required. To this end, an extensive operating system would serve no purpose. Therefore, testing is done with a minimal operating system and a test executive. This is to allow for low-level testing of sections of the processor.

Testing uses various software routines to isolate sections of the microprocessor (e.g., registers, cache memory, floating–point and MMX units). Additionally, numerous processor speeds are tested in an attempt to investigate frequency dependent events. This is done using processors of various rated clock speeds and running these processors at a lower than rated Front Side Bus (FSB) frequency.

The main part of the test flow is placing the DUT in a known operating state, waiting for something to happen and then dealing with it. Figure 4 shows a flowchart of the methodology used once an event happens. The flowchart shows that five event types are expected: end of test fluence, single event functional interrupt (SEFI), system resets (radiation induced),

single event latchup (SEL), and non-fatal errors (some error is produced but it does not immediately induce a functional interrupt or system reset). Once one of these conditions is seen and identified, the test process is to gain information about what exactly happened and to recover the DUT to a known state.

It is important to understand what the definition of a functional interrupt is used here. The main routine of the test executive software was written to handle all the exceptions that the processor could throw. So, in addition to looking for errors produced in the specific test being run, the test software handles any other generic exception. In general, if the exception can be handled (after the exception is recorded the process restarts correctly) it is classified as a non-fatal error (NFE). It should be noted that if these exception-handling routines were not present these events would result in the test software being halted. So, within this work, a SEFI is an event that causes the processor to lock up, reset, have continuous exceptions, or go into some unknown, unrecognizable state.

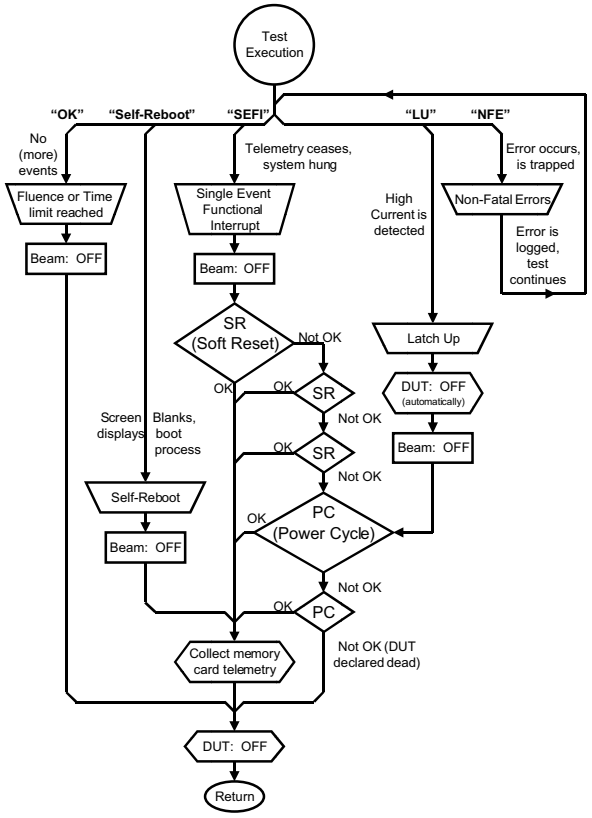

Figure 4. SEE Testing flowchart showing the expected possible outcomes from a Single Event and the methodology used in dealing with these events.

The SEE testing was conducted at the Texas A&M University (TAMU) Cyclotron facility utilizing beams of 55.1 MeV/amu Oxygen and Argon ions (giving energies of 882 and 2204 MeV, respectively). Unlike the proton testing, all materials in the beamline must be considered. Therefore, these materials and the depth into the silicon die must be taken into account to properly determine the LET in the ions in the sensitive regions of the device.

The material conditions used in the TAMU testing were 25.4 microns of aramica (output window of the cyclotron), 60 millimeters of air (testing was done in air for thermal considerations), 10 mils of Aluminum (water-cooled jacket) and 900 micron of silicon (P3 die thickness). The first two of these were stationary, whereas the latter two would rotate with the device (for getting effective LETs). Figure 5 shows a plot of the LET in silicon as a function of the depth in silicon (the aramica and air degradations have been accounted for as well as a normal incident ion through the Aluminum).

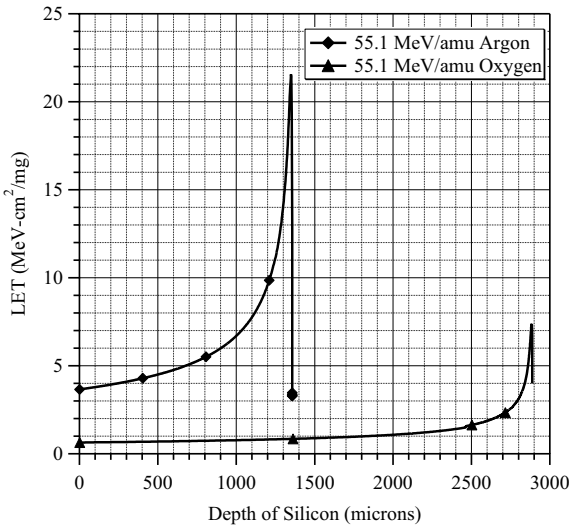

Figure 5. Plot showing the two ions used at TAMU for heavy ion testing. The zero point on the x-axis represents the Silicon surface on the backside of the die.

As can be seen from Figure 5, at the 800-micron depth into the die, the LET curve for the Oxygen ion is relatively flat but the Argon curve is heading towards the Bragg peak. Therefore, for the Argon ion, the LET will not be constant over the sensitive regions. That, combined with not knowing exactly where the sensitive regions begin, makes the determination of the LET in the sensitive regions problematic. For the remainder of this paper, it has arbitrarily been chosen to take the 800-micron depth point as the defining depth for LET. It should be noted that this value should have associated error bars based on this depth and location on the Bragg curve. It would be best, though to utilize experimental information for a more accurate

determination. This can be done using the roll off in cross sections curves with increasing LETs and possibly through the use of charge collection spectroscopy [2] that is currently under investigation.

Therefore, for the Oxygen beam effective LETs of 0.7 and 2 were used. For the Argon beam, effective LETs of approximately 5, 10, 15.7, 19.8, 24.7, and 27.7 were used.

3) Thermal Considerations

The Pentium III, when operating under normal conditions with all caches enabled, will draw in excess of 20 watts of power. If left in that state with no cooling, the processor will not even boot.

Also, The Pentium III and AMD K7 die, as procured as a COTS parts, are flip chip solder bubble bonded die to the DUT daughter cards. Since the beam must hit the die directly, the packaged heat sink and cooling fan must be removed. In its place a water-cooled jacket, which is thinned to 10 mils over the die, is used.

The large thermal source is also the reason that the die cannot be thinned, as has been done with other flip chip parts. The thick substrate is the main thermal path for removal of heat from the junctions. Thinning this would place excessive thermal stresses on the die and most likely lead to structural failures.

4) Die Thickness Issue

As pointed out above, these parts are flip chip solder bubble bonded die. This places the sensitive regions of the processor approximately 900 microns deep in the silicon die with respect to the heavy ion incidence point (See Figure 6). Thermal issues compound this by requiring cooling material in the beam line, as well. Therefore, only high energy and high Z beams are capable of penetrating and giving higher Linear Energy Transfer (LET) values in the sensitive regions.

V. Test Results

Table II shows a listing of all the DUTs that were tested and the testing that they underwent. This section will summarize the TID and SEE testing results that have been observed to date.

A. Total Dose

Intel P3 and AMD K7 parts were exposed to the total dose environment at the IUCF proton facility and the GSFC Radiation Effects Facility (Cobalt-60). The results of this testing are summarized in Table III. It should be noted that the one DUT rated at 550 MHz is 0.25 µm technology, while all other DUTs tested are 0.18 µm technology.

The parts tested at IUCF were exposed to protons in unbiased and biased states and exposed to proton doses ranging to approximately 100 krads(Si) with various increments. After each dose point, the all parts passed all functional tests and the monitored voltages and currents did not change. No parametric timing measurements were done in these tests. These parametric tests are expected to be the most sensitive to dose. The parts, however, did not degrade in timing sufficiently to fail any of the functional tests that were performed.

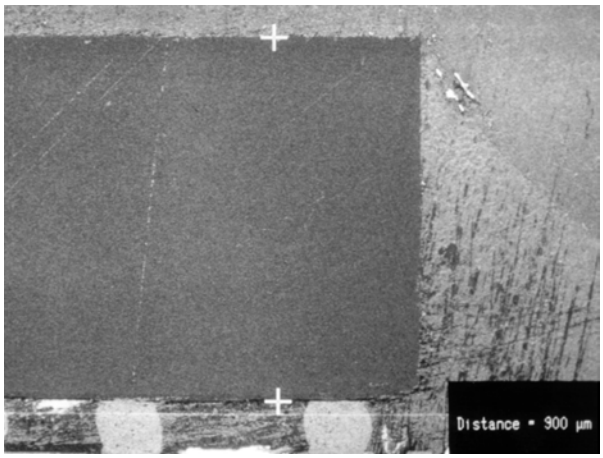

Figure 6. Photograph showing a close up cross section of the P3 die. Depicted here is the die thickness (900 microns) between the backside of the die and the front edge where the solder bubbles are clearly visible.

Total dose testing using the Cobalt-60 source at GSFC is still continuing. Several P3 devices, in an unbiased condition, have been exposed to various doses, one in excess of 1600 krads(Si). They have shown little sign, if any, of degradation in either supply currents or timing and functionality testing. Biased testing of one Pentium III DUT is still ongoing and to date has been exposed to in excess of 400 krads(Si).

There were plans to expose the AMD K7 processors, both biased and unbiased, to Cobalt-60. However, after the poor showing the parts made at the heavy ion facility (see next section), it was determined to remove the AMD K7 parts from this study.

This proton total dose testing seems to indicate that these generations of AMD K7 processors are TID hard to greater than 100 krad(Si), based on minimal test data. However, based on substantial data collected via proton and Cobalt-60 exposure, the Intel Pentium III processors are extremely tolerant to total dose, with unbiased parts surviving in excess of 1.6 Grads(Si) and biased parts surviving in excess of 400 krads(Si).

TABLE II
DEVICE UNDER TEST (DUT) TABLE

Device	Vendor	Rated Speed	Operating Speed	Source	Test Type	Package Markings
Pentium III	Intel	550 MHz	550 MHz	Protons	SEE	550/256/100/1.65V S1 90050493-0099 MALAY imc '99 SL3V5
Pentium III	Intel	550 MHz	Unbiased	Co-60	TID	550/256/100/1.65V S1 90050493-0307 MALAY imc '99 SL3V5
Pentium III	Intel	650 MHz	650 MHz	Protons	SEE	650/256/100/1.65V S1 10100418-0293 PHILIPPINES imc '99 SL3KV
Pentium III	Intel	650 MHz	Unbiased	Protons	TID	650/256/100/1.65V S1 10100418-0176 PHILIPPINES imc '99 SL3KV
Pentium III	Intel	650 MHz	650MHz	Protons	TID	650/256/100/1.65V S1 10100418-0161 PHILIPPINES imc '99 SL3KV
Pentium III	Intel	650 MHz	Unbiased	Co-60	TID	650/256/100/1.65V S1 10160248-0411 PHILIPPINES imc '99 SL452
Pentium III	Intel	650 MHz	Unbiased	Co-60	TID	650/256/100/1.65V S1 10160260-0075 PHILIPPINES imc '99 SL452
Pentium III	Intel	700 MHz	700 MHz	Protons	SEE	700/256/100/1.65V S1 90160187-0108 MALAY imc '99 SL454
Pentium III	Intel	700 MHz	700 MHz	Protons	SEE	700/256/100/1.65V S1 90160187-0055 MALAY mc '99 SL454
Pentium III	Intel	700 MHz	700 MHz	Protons	TID	700/256/100/1.65V S1 90160187-0057 MALAY imc '99 SL454
Pentium III	Intel	700 MHz	Unbiased	Co-60	TID	700/256/100/1.65V S1 90160187-0060 MALAY imc '99 SL454
Pentium III	Intel	750 MHz	500, 750 MHz	Protons	SEE	750/256/100/1.65V S1 90260050-0092 MALAY imc '99 SL456
Pentium III	Intel	800 MHz	533, 800 MHz	HI	SEE	800/256/100/1.65V S1 90240221-0006 MALAY imc '99 SL457
Pentium III	Intel	800 MHz	800 MHz	Co-60	TID	800/256/100/1.65V S1 90240169-0091 MALAY imc '99 SL457
Pentium III	Intel	850 MHz	850 MHz	Protons	SEE	850/256/100/1.65V S1 10280400-0071 Philippines imc '99 SL47M
Pentium III	Intel	850 MHz	566, 850 MHz	Protons	SEE	850/256/100/1.65V S1 10280400-0293 Philippines imc '99 SL47M
Pentium III	Intel	850 MHz	Unbiased	Co-60	TID	850/256/100/1.65V S1 10280400-0262 Philippines imc '99 SL47M
Pentium III	Intel	933 MHz	466, 700, 933 MHz	Protons	SEE	933/256/133/1.7V S1 00280415-0224 COSTA RICA imc '99 SL47Q
Pentium III	Intel	933 MHz	466, 700, 933 MHz	HI	SEE	933/256/133/1.7V S1 00280415-0269 COSTA RICA imc '99 SL47Q
Pentium III	Intel	933 MHz	466, 700, 933 MHz	HI	SEE	933/256/133/1.7V S1 11040081-0098 Phillippines imc '00 SL4KK
Pentium III	Intel	933 MHz	Unbiased	Co-60	TID	933/256/133/1.7V S1 00280415-0068 COSTA RICA imc '99 SL47Q
K7	AMD	600 MHz	600 MHz	Protons	SEE	AMD-K7600MTR51B C 219949147583
K7	AMD	650 MHz	650 MHz	Protons	SEE	AMD-K7650MTR51B A 210017540094
K7	AMD	650 MHz	650 MHz	HI	SEE	AMD-K7650MTR51B A 210017540094
K7	AMD	650 MHz	Unbiased	Protons	TID	AMD-K7650MTR51B A 230015009833
K7	AMD	700 MHz	700 MHz	Protons	SEE	AMD-K7700MTR51B A 210019614073
K7	AMD	900 MHz	900 MHz	Protons	SEE	AMD-K7900MNR53B A 210036542751
K7	AMD	1 GHz	1 GHz	Protons	SEE	AMD-K7100MNR53B A 710026014044
K7	AMD	1 GHz	1 GHz	Protons	SEE	AMD-K7100MNR53B A 710026147861
K7	AMD	1 GHz	1 GHz	HI	SEE	AMD-K7100MNR53B A 710026019051

TABLE III
TID RESULTS TABLE

DUT	Rated Speed (MHz)	Operating Speed	Source	Exposure Level
P3	650	Unbiased	Protons	26 krad
P3	650	650MHz	Protons	52 krad
P3	550	Unbiased	Co-60	336 krad
P3	650	Unbiased	Co-60	336 krad
P3	650	Unbiased	Co-60	*1.59 Mrad
P3	700	700 MHz	Protons	100 krad
P3	700	Unbiased	Co-60	336 krad
P3	800	800 MHz	Co-60	*404 krad
P3	850	Unbiased	Co-60	*85 krad
P3	933	Unbiased	Co-60	*85 krad
K7	650	Unbiased	Protons	100 krad

** Exposure levels as of 6/1/01.*

A. Single Event Effects

Both P3 and K7 processors were evaluated for SEE response. This included exposure to protons at the IUCF and heavy ions at Texas A&M University (TAMU) Cyclotron.

1) Protons

Figures 7 and 8 show the Pentium III and AMD K7, respectively, SEFI cross sections as a function of the processor speed with various cache states. It is quite obvious from this figure that the cache represents the most sensitive region of the device and its operation causes the SEFI rate to increase by approximately a factor of 3 to 10 in magnitude. There is approximately a factor of three difference between the P3 and K7 SEFI cross sections, with the K7 being higher.

For the P3, different rated processor speeds are shown with different symbols. The K7 parts were not clocked down so the data points shown are for the rated processor speed. Therefore, Figures 7 and 8 also show no processor speed differences.

It should also be mentioned that some K7 processors had a high current transient on the core power supply. While these transients were very high (tens of amperes in some cases), no destructive events were ever observed. In fact, the processors for most transients continued to work through a series of transients before a reset event would occur. The other aspect of this to note is that these transients were not observed in all K7 parts, not even consistently across a processor speed family. An attempt was made to determine if this was a foundry effect, but that information was not available on the part or from AMD.

As pointed out in the Test Methodology section, another category of events is exceptions. These are events, if not handled in software, would lead to a SEFI. This data is shown in Figure 9. The cross section is similar to the SEFI cross section and again no speed dependence is observed.

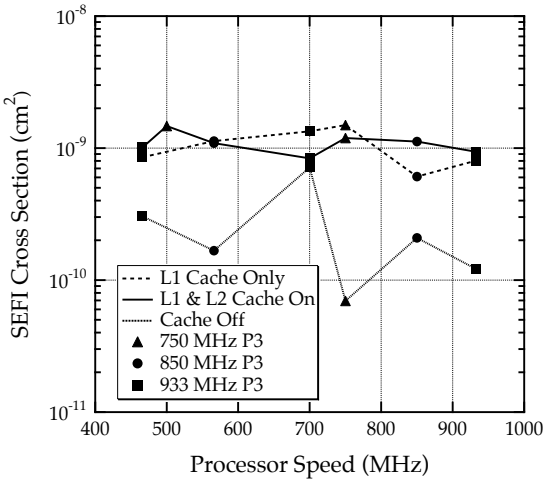

Figure 7. Plot showing the Pentium III SEFI cross section as a function of the processor speed with various cache states. Note that the symbol shape represents the three different rated processor speeds used in the testing.

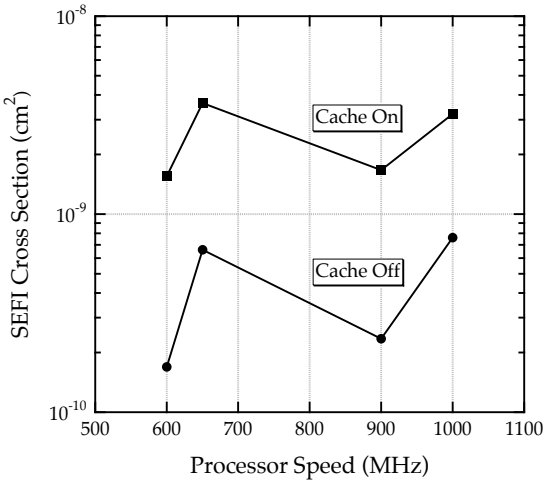

Figure 8. Plot showing the AMD K7 SEFI cross section as a function of the processor speed with On/Off cache states.

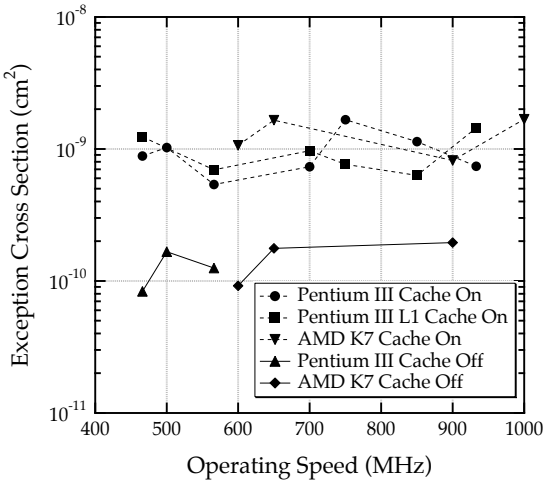

Figure 9. Plot showing the Pentium III and AMD K7 Exception cross section as a function of the processor speed with various cache states.

The final category of event is upsets. The various tests, A through G, were designed to look for upsets in the registers, caches, floating point and MMX units. The cross section data obtained from these tests for the P3 and K7 processors is shown in Table IV. The main item to note is that very few events were actually observed. Collection of this data was problematic, as the SEFI rate was sufficiently high as to impact the lengths of the runs. This data had to be collected with the Cache Off or the SEFI would have been too high to collect any significant data.

TABLE IV
PROTON SEU (CACHE OFF) RESULTS TABLE

DUT	Test	Number of Upsets	Fluence (p/cm^2)	Cross Section (cm^2)
P3	A	1	6.53×10^{10}	1.53×10^{-11}
P3	B	0	5.3×10^{10}	$< 1.89 \times 10^{-11}$
P3	C	0	4.7×10^{10}	$< 2.13 \times 10^{-11}$
P3	D	1	7.7×10^{10}	1.3×10^{-11}
P3	F	1	5.17×10^{10}	1.93×10^{-11}
P3	G	1	3.98×10^{10}	2.51×10^{-11}
K7	A	0	5.11×10^{10}	$< 1.96 \times 10^{-11}$
K7	B	0	1.4×10^{10}	$< 7.14 \times 10^{-11}$
K7	C	0	3.19×10^{10}	$< 3.13 \times 10^{-11}$
K7	D	1	$3.47x\ 10^{10}$	2.88×10^{-11}
K7	F	3	3.04×10^{10}	3.29×10^{-11}
K7	G	0	2.85×10^{10}	$< 3.51 \times 10^{-11}$

2) Heavy Ions

As with the protons, the first item to be discussed is the SEFI cross section. The data for the P3 and K7 are shown in Figure 10. The first observation to make is roll-off with LET. The K7 processor shows a significant roll-off after an LET of 15. It should be noted that the thickness was determined using a P3 part and the K7 part could have a substantially thicker substrate. The P3 parts do not show this roll-off but most likely would show a higher saturation cross section if a longer range, high LET ion were used. As for LET threshold, every ion used in this test eventually led to a SEFI event. Therefore, the SEFI LET threshold is less than 0.7 MeV-cm^2/mg.

The next observation to make is the order of magnitude difference between the K7 and the P3 processors. This difference is for the cache off condition only as the cache on condition for the K7 led to a single event induced reset as soon as the beam was turned on. This did not allow for an accurate determination of a SEFI cross section for the K7 cache on state. For even the cache off state, the rate was high enough that the time to turn the beam off was a substantial error in the actual SEFI cross section.

Finally, it should be noted that the same high current transients observed in the proton testing on the K7 processors were observed with the heavy ions. They were observed on the same parts that demonstrated them in the proton testing and not seen on the same parts that did not demonstrate them with protons. This significant part to part variation, with the very high SEFI rate, led to the decision to remove the AMD K7 parts from further consideration (i.e., no additional SEE testing or any Cobalt-60 testing).

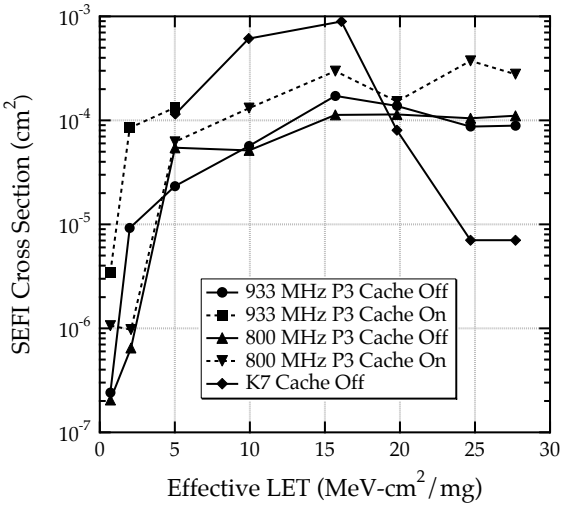

Figure 10. Plot showing the Pentium III and AMD K7 SEFI cross section as a function of the Effective LET with On/Off cache states.

With this determination in mind, the remainder of this section deals exclusively with the Pentium III processor. Also from this point forward, processor speed is not explicitly shown in the figures. As was stated for previous figures, it is true for the following figures that no speed sensitivity was observed for any of the tests.

Next to be considered is the exception cross section (i.e., those events that if not handled would lead to a SEFI). Figure 11 shows the data for the exceptions as a function of LET and cache state.

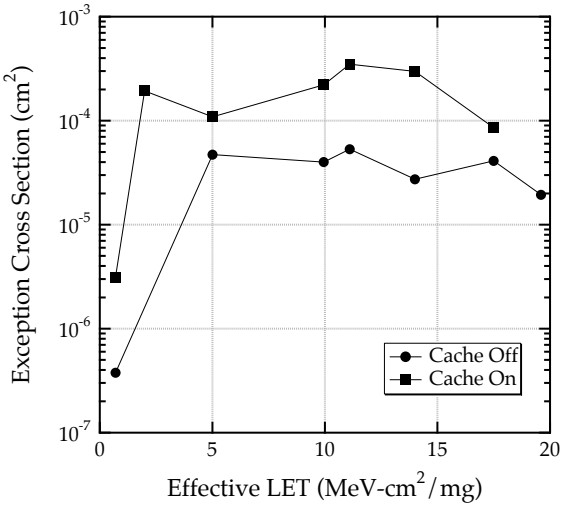

Figure 11. Plot showing the Pentium III Exception cross section as a function of the Effective LET with On/Off cache states.

As with the SEFI, the LET threshold is less than 0.7. There does appear, however, to be a more significant roll-off with LET above an LET of 10 to 15. The fact that events shown in Figures 10 and 11 are still observed at the higher LETs, indicates that as long as charge is deposited in the region between 800 and 900 microns, events can occur. It is not necessary for the ion to actually reach the sensitive region, as the LET 28 ions do not have sufficient range to reach 900 microns.

The final data to be presented is for upsets based on tests A, B, F, and G (registers, FPU, and MMX units, respectively). This data is shown in Figure 12. As with the proton testing, there were only a small number of events observed for each of the conditions, leading to the low saturation cross section. While some tests required an LET of 5 to observe events, this may be due more to the small event rate that to a higher threshold. More extensive testing is required to make this determination.

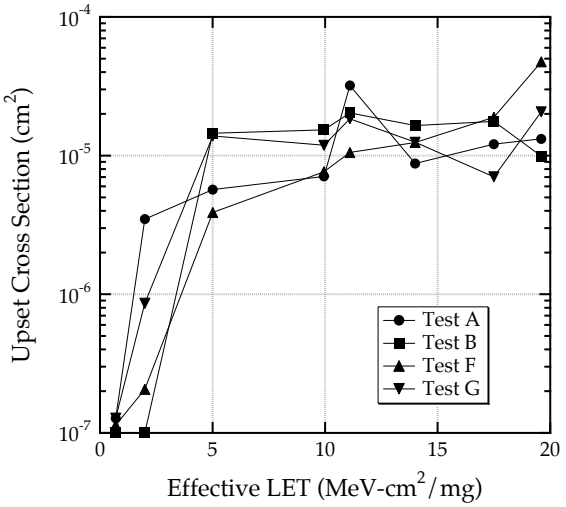

Figure 12. Plot showing the Pentium III upset cross section as a function of the Effective LET, in the cache Off state, for various test cases.

VI. Conclusions

Extensive data has been collected on the total dose and single event response of the Intel Pentium III and the AMD K7 microprocessors. The data indicates that there is a high tolerance to total dose and there is no susceptibility to latchup from protons. Single event upsets and functional interrupts are present. However, for the Pentium III, if running with the caches disabled is an option and with mitigation in place, these events may be controllable to allow for operation in the space environment. The thermal issues and the power requirements of these processors will most likely be the limiting factors in their usage in space applications.

VII. References

[1] 1. J. Beahan, L. Edmonds, R.D. Ferraro, A. Johnston, D.S. Katz, and R.R. Some, "Detailed Radiation Fault Modeling of the Remote Exploration and Experimentation (REE) First Generation Testbed Architecture", unpublished.

[2] R. Reed, Private Communication.