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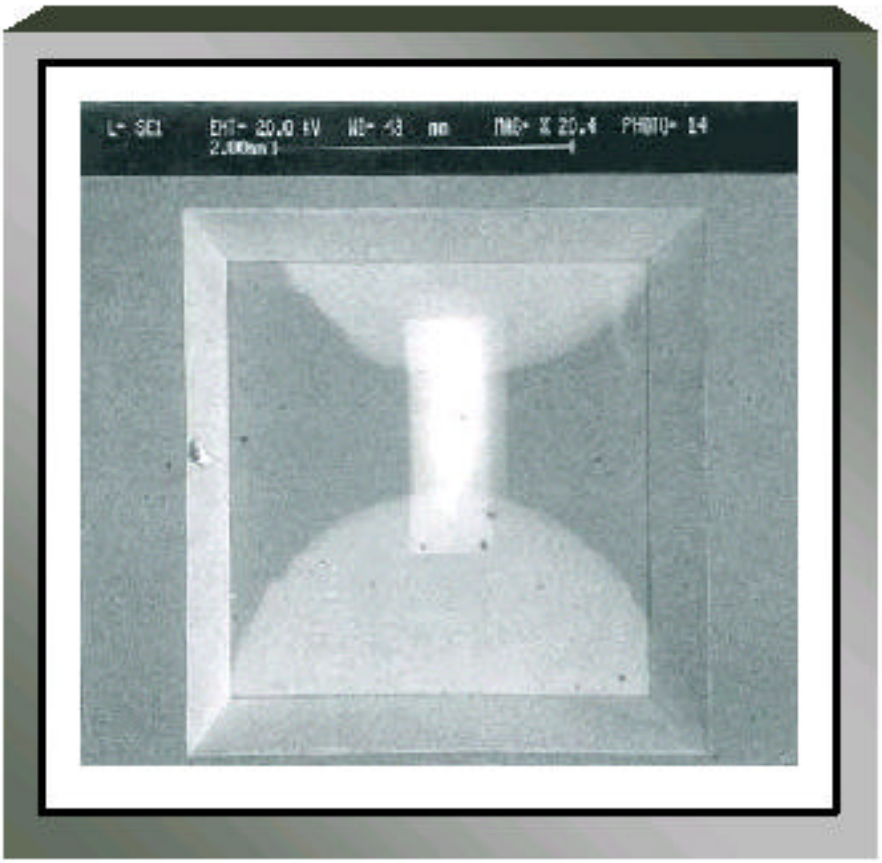

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Variables Affecting CSP Reliability

Reza Ghaffarian
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California
818-354-2059
Reza. Ghaffarian@JPL.NASA.Gov

ABSTRACT
Although the weakest link of chip scale package (CSP) assembly reliability has been often internal package failure, solder joint fatigue is still considered to be the key factor for reliability. Other key factors that affect solder joint reliability including package type, package build, board design, assembly variables, and accelerated environmental testing are also discussed. The reasons for unrealistic life projections for CSP assembly reliability by numerous modelers is also examined. It was concluded that availability of meaningful assembly reliability test results are needed to accelerate implementation of this technology. The JPL-led CSP consortia are addressing many of these issues.

CSP RELIABILITY
The CSP packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages. Although CSP was defined by "industry experts" as a package that is up to 1.2 or 1.5 times larger than the perimeter or the area of the die, many manufacturers refer to the pack-age that is a miniaturized version of the previous generation. There are many factors that affect CSP assembly reliability. These include design, package build, solder paste, assembly, underfill, and type of test for reliability evaluation. In the following a few of these
variables are discussed.

DESIGN
PWB pad design
For BGAs, discussions on use of solder mask defined vs. non-solder mask (SMD vs. NSMD) were hot subjects for a short period. There were two camps, one showing the improvement due to use of SMD– reasoning that masks over copper are needed for improved adhesion as well as the potential benefit of
cycles to failure increased due to increase in solder joint height. The other camp showed that crack initiation in solder, due to overlaying of the mask, could reduce the number of cycles to failure. NSMD is now commonly recommended. The pad size design relative to package has its own supporters. As a rule of thumb, the board pad size should be the same as the package. A slight unbalance in this relationship could result in failure at the board or package. Optimized conditions might differ for different packages depending on the ball attachment configuration.

PACKAGE VARIABLES
Die bond on interposer
There are various techniques that are used to transfer the die I/O to the interposer within the package. Each element of the package internal form has its own effect. For TAB CSP (Tape Automated Bonding), the TAB is the weakest link. For flip chip die in a flip chip CSP, the failure was observed on the C5 (board level) solder joint interconnection, when subjected to thermal cycling. This might not be the general case for the flip chip die. CSPs and BGAs with flip chip dies are more susceptible to internal package failure than their wire bond versions.
Interposer thickness
When the interposer was increased from 0.4 mm thickness to 0.6 mm, cycles to failure increased from 400 to about 800 cycles (-25/125°C). Data for a flip chip CSP, indicates that semi-rigid interposer would have 1.88 times the number of thermal cycles. Is the rigidity equivalent to thickness change or possibly because of materials change? The answer is not known. Interposer CTE also has significant affect on the board reliability.
Interposer materials
CSPs with different interposer materials showed significantly different cycles to failure– about a three times increase (Sony, IMAPS '97). In an experiment, it was found that a factor of about three times will be achieved when a low CTE interposer was used (1200 vs. 400 cycles, -25/125°C).
Die size
In one study it was shown (R. Darveaux, ECTC '98) that when die size increased from 6.4 mm to 9.5 mm, the first cycles to failure decreased from 1500 to 900 cycles in the range of -40°C to 125°C.

SOLDER BALL
Solder composition
Eutectic solder (63/37) is the most commonly used solder due to it having many desirable attributes, in-cluding low temperature melting. To improve fatigue characteristics, small amounts of silver (2%)
have been added to this composition. Additive materials have the potential of formation of brittle intermetallic phases as well as softening by precipitation formation. These metallurgical transitions are further accelerated by increases in temperature. Effect of five element alloy was shown to improve thermal cycling reliability by 1.2 to 1.5 times (Ano, SMI CSP Symposium Proceedings '97).
Ball shape attachment

For BGAs, it has been demonstrated that the DBGAs (Dimple BGA) improve reliability. This might be the case for CSPs too, but its significance is yet to be demonstrated.

ASSEMBLY VARIABLES OF RELIABILITY

Solder joint height

The effect of solder joint height on reliability has been widely discussed for BGAs. One reason for the use of an SMD pad for PBGAs, with collapsible solder, was to increase solder ball height and hence increase reliability. Height was also increased by use of columns in the ceramic column grid arrays to achieve significant reliability improvements compared to the ball grid array version. Improvement was shown for CSPs when ball heights are increased (Kosuga IMAPS 97). When solder height is doubled, cycles to failure for the board tripled– a Coffin-Manson exponential value of β=1.6.

Underfill

One key advantage of CSPs over flip chips is that ideally there is no requirement for CSPs to be underfilled. The assemblers for consumer products prefer packages with no underfill one process step is eliminated and reworkability is permitted. However, for high reliability applications where vibration and shock are key in ruggedness, use of underfill might be the only solution now known to meet the harsh requirements. For flip chips with very short cycles to failure, it has been shown that underfill will improve cycles to failure reliability an order of magnitude (5-10 at least). This is very similar to the results shown for the wafer level miniBGA packages with and without underfill.

Double Reflow

There are many concerns when double-sided boards are assembled. Reliability reduction is one. For heavy BGAs, one concern was potential part fall from the assembled side during the second reflow. Similar concerns might be true for CSPs with the small solder volume; not enough tension force to hold even the small size of CSPs. In addition, it has been shown that for two sided packages, reliability of board assembly was half of the single sided (Kosuga, IMAPS '97). Recently, similar test results were presented for another CSP package (Juso, ECTC 98). Double sided assemblies with packages on directly opposite sides of the board showed lower cycles to failure. This was improved with partial relative package offsets on the two sides.

FAILURE MECHANISMS AND CSP RELIABILITY

Solder joint interconnects were considered to be the main cause of assembly failure. Failure at the board level could also be caused by the internal failure of the package. For example, package internal TAB lead failures at heels were reported for the CTE absorbed CSP— a fatigue failure shift from the solder joint to the internal package. This new type of failure is in contrast to the traditional theoretical wisdom where the solder joint failure is generally considered to be the weak link in solder joint assemblies. This and other failure mechanisms, which are being established for CSPs, must be understood by a modeler before he/she is to predict a meaningful reliability projection. Table 1 includes four projections from different modelers and experiment test results. It is interesting to compare the theoretical values with those experiment test results for numerous CSPs. It becomes obvious that these calculations are at least 5 to 20 times higher than the test results. To date, the highest value test results reported for CSPs are in the range of 500 to 1,000 cycles. Projections of more than 20,000 cycles to failure in the range of -55 to 125°C is very unrealistic and are misleading. Misleading results could also occur when DNP (distance to neutral point) is used as indicator for cycles to failure. In the IPC report J-STD-012 (Joint Industry Standard Implementation of Flip Chip and Chip Scale Technology), assembly reliability projections were based on flip chip die being attached to the board. DNPs were used for calculation of the first failure and projection of failure with size of package. This is not valid for most CSPs, except possibly for a few wafer level CSPs without underfill. Although there is a relationship between an increase in die size and reliability, the relationship is not linear and depends on many parameters. For example, fan-out packages with small die will not follow the DNP indications.

Table 1. Misleading CSP Cycles to Failure Projections by Modeling

Package Type	I/O	Cycle Profile	Cycles to Failure Projection	Test Results
TAB CSP	46	-55/125°C	7,000	500-1,000
WAFER CSP	96	-40/125°C	3,200	200-500 8 failures
FLIP CHIP CSP	N/A	-55/125°C	20,000	N/A
LOW COST CSP	N/A	-40/125°C	21,000	N/A

LESSONS LEARNED AND RECOMMENDATIONS

Board reliability information is essential for CSP implementation for high reliability applications and to ease their use in commercial sectors. For wider application of this technology, the potential user will need design reliability data since they often do not have the resources, time, or ability to perform complex environmental characterizations. To help build the infrastructure in these areas, nearly 200 test vehicles were assembled by the JPL-led consortia to address many technical issues regarding the interplay of package types, I/O counts, PWB materials, surface finishes, and manufacturing variables for the quality and reliability of assembly packages. Results will be published as they become available.

REFERENCES

Four main sources of information for the text were from:

1. SMI '97, Proceedings of Chip Scale Packaging Symposium, SMI, Sept. 7-11, 1997
2. IMAPS '97, Proceedings of International Symposium on Microelectronics, Philadelphia, October 14-16, 1997
3. CSI '98, Proceedings of Chip Scale International, San Jose, May 6-7, 1998
4. ECTC '98, Proceedings of 48th Electronic Components & Technology Conference, Seattle, May 25-28, 1998

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