Accelerated Thermal Cycling and Failure Mechanisms For BGA and CSP Assemblies

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ABSTRACT

This paper reviews the accelerated thermal cycling test methods that are currently used by industry to characterize the interconnect reliability of commercial-off-the-shelf (COTS) ball grid array (BGA) and chip scale package (CSP) assemblies. Acceleration induced failure mechanisms varied from conventional surface mount (SM) failures for CSPs. Examples of unrealistic life projections for other CSPs are also presented.

The cumulative cycles to failure for ceramic BGA assemblies performed under different conditions, including plots of their two Weibull parameters, are presented. The results are for cycles in the range of –30°C to 100°C, –55°C to 100°C, and –55°C to 125°C. Failure mechanisms as well as cycles to failure for thermal shock and thermal cycling conditions in the range of –55°C to 125°C were compared. Projection to other temperature cycling ranges using a modified Coffin-Manson relationship is also presented.

INTRODUCTION

Reliability, irrespective of its definition, is no longer an "after-the-fact" concept; rather, it must be an integral part of development and implementation. This is specifically true for microelectronics with demands for miniaturization and system integration in a faster, better, and cheaper environment. BGAs and CSPs rapid development and introduction into the market is a good example of this trend.

The use of new materials, processes, and new applications obscure the traditional definition of quality and reliability assurance. New systems approaches are needed to assure quality and reliability as well as to manage risks. Quality should be assured by design for reliability, controls for processes, tailored testing methods for qualification, and use of unique accelerated environmental testing along with credible analytical prediction. In other words, an efficient concurrent engineering system approach must be implemented.

Environmental Testing

Among the many environmental accelerated testing methodologies for assessing reliability of electronic systems, thermal cycling is the most commonly used for the characterization of devices as well as interconnections. From the many predefined thermal cycling profiles, the military and commercial ranges represent the two extremes. Previously, NASA also had a preset specific thermal cycling requirement. Although a number of Military Standards were obsoleted, they are still used for benchmark testing. For example, within Mil-STD-883, there are three levels of accelerated cycling temperatures:

- Condition A, -55°/85°C
- Condition B, -55°/125°C
- Condition C, -65°/150°C

For acceptance/benchmark testing, devices are generally subjected to condition C and assemblies most often to condition B. The assemblies were traditionally considered qualified when they survived 1,000 cycles. A commercial cycling profile, the J-12 IPC specification, recommends a thermal cycle in the range of 0°C to 100°C. Within a temperature range, the dwell, heat and cool down rates are critical parameters and also affect cycles to failure.

The NASA thermal cycling requirements are stringent and are specified in various revisions of NASA Handbooks. For example, in a previous revision, NHB 5300.4 (3A-1), there was a well defined requirement for number of cycles and solder condition after exposure. No cracking of any solder joint was allowed after 200 NASA cycles (-55°C to 100°C with 245 minutes duration).

Performance-based Assurance Requirement

In a subsequent NHB revision, the requirements were based on meeting the specific mission condition. The build and test methodology is expected to yield confidence in reliability to satisfy the mission conditions. Mission requirements are emphasized rather than a universal cycle and a value for all missions.

Test to "establish the confidence in reliability" adopted by NASA a long-time ago is now "the reliability theme" for the commercial sector. Discussions on "Breaking Traditional Paradigms" and "Rethinking of Environmental Reliability Testing" by authors from the commercial sector are becoming hot topics with the introduction of new miniaturized CSPs. These packages have their own unique form factor not seen in SMT. Unable to meet the stringent requirements established by the previous military standards, a new "paradigm shift" is considered to be the solution.

The "shift" is further motivated by several factors including the following:

- Reduction in life expectancy for consumer electronics
- Rapid changes in electronic technology
- Obsolescence of many military specifications

Additional unique tests are now adopted to meet the specific consumer electronic products. For portable electronics, bend test, drop test, and possible "washing machine test" are suggested. The IPC 9701 specification, Qualification and Performance Test Methods for Surface Mount Solder Attachments, is aimed to include some of these requirements. It must be recognized that no accelerated tests can be truly universal. Field reliability is the ultimate test, and either substantiates or invalidates the experimental tests.

For space missions, gathering information on the root cause of field failure is almost impossible. For commercial applications, rapid changes in technology render field information almost useless for new product development. The only solution is to understand key reliability parameters and to design for reliability. Subsequent process controls, as well as effective qualification and inspection, also help assure sufficient field reliability. In other words, risk control and risk management must be practical.

Failure Mechanisms and CSP Reliability

Emerging grid CSPs, miniature versions of BGAs are competing with bare die flip chip assemblies. CSP is an important miniature electronic package technology for utilizing especially low pin counts, without the attendant handling and processing problems of low peripheral leaded packages such as thin small outline packages (TSOPs) and high I/O (input/output) quad flat packages (QFPs). Advantages include self alignment characterization during assembly reflow process and better lead (ball) rigidity.

For conventional surface mount assemblies, solder joint interconnects were considered to be the main cause of assembly failure. For CSPs, failure at the board level could also be caused by the internal failure of the package. For example, package internal tape TAB (tape automated bond) lead failures at heels were reported for the CTE (coefficient of thermal expansion) absorbed CSP— a fatigue failure shift from the solder joint to the internal package (see Figure 1).

This new type of failure is in contrast to the traditional theoretical wisdom where the solder joint failure is generally considered to be the weak link in solder joint assemblies. This and other failure mechanisms, which are being established for CSPs, must be understood by a modeler before he/she is to predict a meaningful reliability projection.

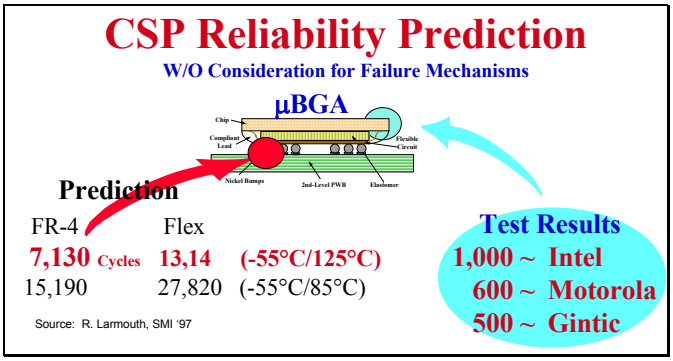

Figure 1 Fatigue failure projection based on the wrong failure mechanism assumption

Table 1 includes four projections from different modelers and experiment test results. It is interesting to compare the theoretical values with those experiment test results for numerous CSPs. It becomes obvious that these calculation are at least 5 to 20 times higher than the test results. As noted earlier, the highest value test results are in the range of 500 to 1,000 cycles. Projections of more than 20,000 cycles to failure in the range of -55 to 125°C is unrealistic.

Table 1 Unrealistic CSP cycles to failure projections by modeling

Package Type	I/O	Cycle Profile	Cycles to Failure Projection	Test Results
TAB CSP	46	-55/125°C	7,000	500-1,000
WAFER CSP	96	-40/125°C	3,200	200-500 8 failures
FLIP CHIP CSP	N/A	-55/125°C	20,000	N/A
LOW COST CSP	N/A	-40/125°C	21,000	N/A

Unrealistic results could also occur when DNP (distance to neutral point) is used as an indicator for cycles to failure. In the IPC report J-STD-012 (Joint Industry Standard Implementation of Flip Chip and Chip Scale Technology), assembly reliability projections were based on flip chip die being attached to the board. DNPs were used for calculation of the first failure and projection of failure with size of package. This is not valid for most CSPs, except possibly for a few wafer level CSPs without

underfill. Although there is a relationship between an increase in die size and reliability, the relationship is not linear and depends on many parameters. For example, fan-out packages with small die will not follow the DNP predictions.

BGA ASSEMBLY RELIABILITY

BGA is an important technology for utilizing higher pin counts, without the attendant handling and processing problems of the peripheral leaded packages. They are also robust in processing because of their higher pitch (0.050 inch typical), better lead rigidity, and self-alignment characteristics during reflow processing.

BGAs' solder joints cannot be inspected visually and reworked using conventional methods and are not well characterized for multiple double sided assembly processing methods. In high reliability SMT assembly applications, e.g. space and defense, the ability to inspect the solder joints visually has been standard and has been a key factor in providing confidence in solder joint reliability. Inspection techniques such as X-ray can be used to detect gross manufacturing defects such as solder bridging, but are not suitable for detection of other defects such as cracks.

To address many common quality and reliability issues of BGAs, JPL organized a consortium with sixteen members in early 1995 (Ghaffarian, BGA guidelines, 1998). Diverse membership including military, commercial, academia, and infrastructure sectors which permitted a concurrent engineering approach to resolving many challenging technical issues. Likewise, MicrotypeBGA and CSP consortia addressing many technical and infrastructure issues regarding miniature packages including CSPs was organized (Ghaffarian, et al, 1998).

Test Vehicles

The test vehicles in this investigation included both plastic and ceramic packages on either FR-4 or polyimide printed circuit boards (PWB) with six layers, 0.062 inch thick. Ceramic packages with 625 I/Os were one of the type of BGAs that were included in our evaluation. Solder balls for CBGAs had high melt temperature composition (90Pb/10Sn) and about 0.035 inch diameters. The high melt balls were attached to the ceramic package with eutectic solder (63Sn/37Pb). At reflow, package side eutectic solder and the PWB side eutectic paste were reflowed to provide the electro-mechanical interconnects.

The CBGA package had internal daisy chains which made a closed loop with daisy chains on the PWB, enabling the monitoring of solder joint failure through continuous electrical monitoring. Daisy chain were divided into four ring regions (See Figure 2) in order to identify failure sites with increased thermal cycles. The first failure is known to have occurred at the peripheral ring in the corner solder joints with the maximum DNPs. To improve assembly reliability, the package supplier had removed daisy chain connections among a few corner balls; excluding them from failure detection during electrical monitoring. This means that cycles to first failure data cannot be directly correlated to package diagonal dimension which usually is assumed to be equal to the maximum DNP.

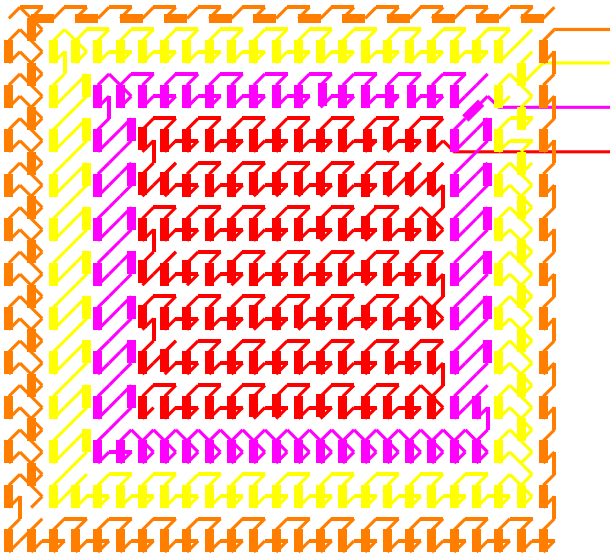

Figure 2 Daisy chain for CBGA 625 I/O

BGA- Thermal Cycling

Four different thermal cycle profiles were used. These were:

- Cycle A: The cycle A condition ranged from -30 to 100°C and had an increase/decrease heating rate of 2 to 5°C/min and dwell of about 20 minutes at the high temperature to assure near complete creeping. The duration of each cycle was 82 minutes.

- Cycle B: The Cycle B condition ranged from –55 to 100°C with long time duration. The heating and cooling rates were 2 to 5°C per minute with an oven dwell setting of 45 minutes at the two extreme temperatures. The duration of each cycle was 246 minutes.
- Cycle C: The cycle C condition ranged from –55 to 125 °C with 2-5°C/min heating/cooling rate. Dwell at extreme temperatures were at least 10 minutes with duration of 159 minutes for each cycle.
- Cycle D: The cycle D condition ranged from -55 to 125°C, the same as condition C, but with very high heating/cooling rate It could also be considered a thermal shock since it used a three region chamber: hot, ambient, and cold. Heating and cooling rates were nonlinear and varied between 10 to 15 °C/min. with

dwells at extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes.

The criteria for an open solder joint specified in IPC-SM-785, Sect. 6.0, were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, there were many additional interruptions within 10% of the cycle life. This was especially true for ceramic packages.

Figure 3 shows three data sets for cycles-to-first-interruption as well as the number of electrical interruptions detected for condition D. For these, the first interruptions were observed at 129, 205, and 267 cycles. After a slow increase after first signs of failure, the rate of interruptions (slope) became approximately constant (70 interruptions/cycle) at higher cycles indicating a complete daisy open chain.

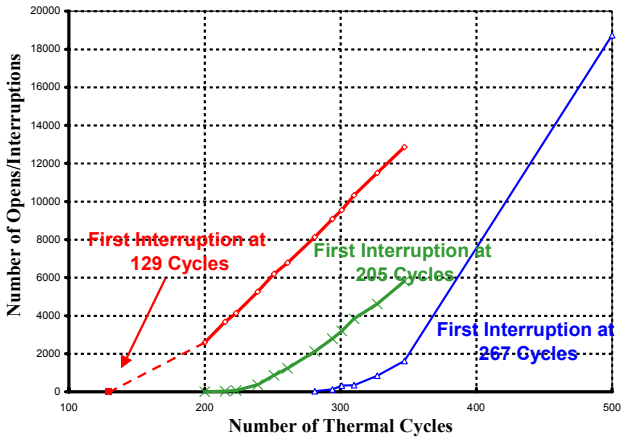

Figure 3 Electrical interruptions detected with thermal cycles for CBGA 625

BGAs- Damage Monitoring

Both board and package interface cracking was observed with increasing number of cycles. Figure 4 shows typical failures for the two cycling conditions. Failures under the A conditions were generally from the PWB and for the D conditions from the package sites. Failure mechanism differences could be explained either by global or local stress conditions.

Modeling indicates that the high stress regions shifted from the board to the package themselves when stress conditions changed from the global to local. For the A cycling, with slow heat/cooling ramping, which allowed the system to reach uniform temperature, damage could indicate a global stress condition. For the D cycle with rapid heat/cooling, damage could indicate a local stress condition.

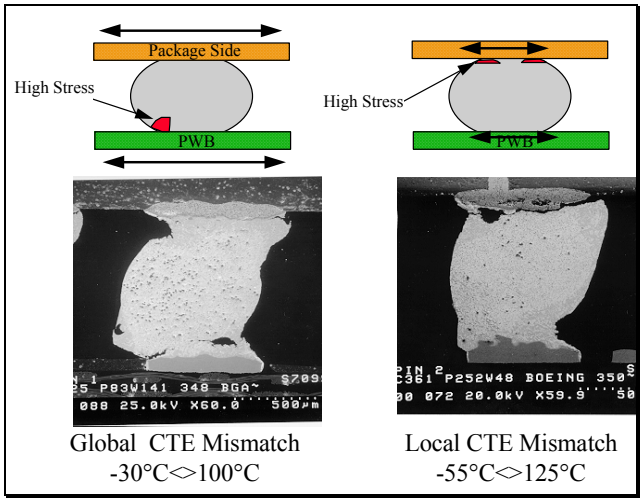

Figure 4 Cross-sections of failure sites for CBGA 625 after 350 cycles under A and D conditions

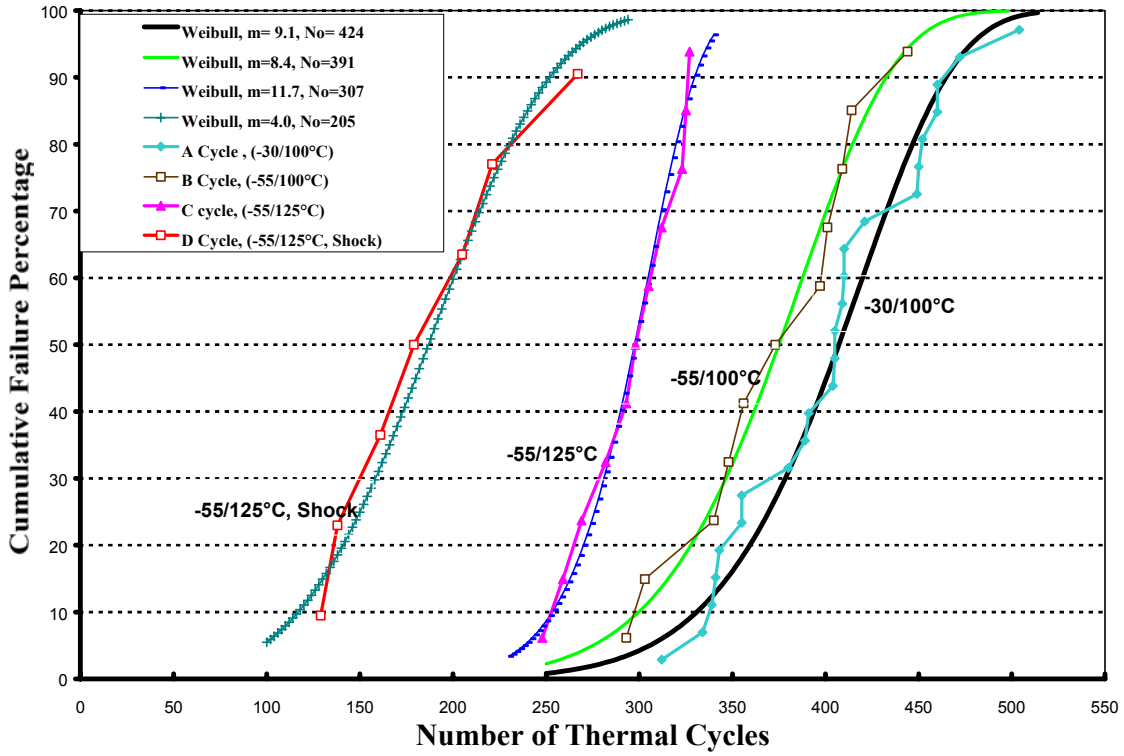

Figure 5 Cycles to failure for CBGA 625 assemblies under different cycling conditions

Table 2 Weibul parameters for CBGA 625 under different thermal cycling conditions

Cycling Condition	Weibull No (N50%)	Weibull m	Comments
A- (-30/100°C)	424 (407)	9.1	23 test vehicles (TVs), Includes FR-4, polyimide PWB, and 3 solder volumes
B- (-55/100°C)	391 (373)	8.4	11 TVs, FR-4 and polyimide
C- (-55/125°C)	307 (298)	11.7	11 TVs, different assembler
D- (-55/125°C, Shock)	205 (189)	4.0	7 TVs, 3 on FR-4, 3 on polyimide, one with high solder volume

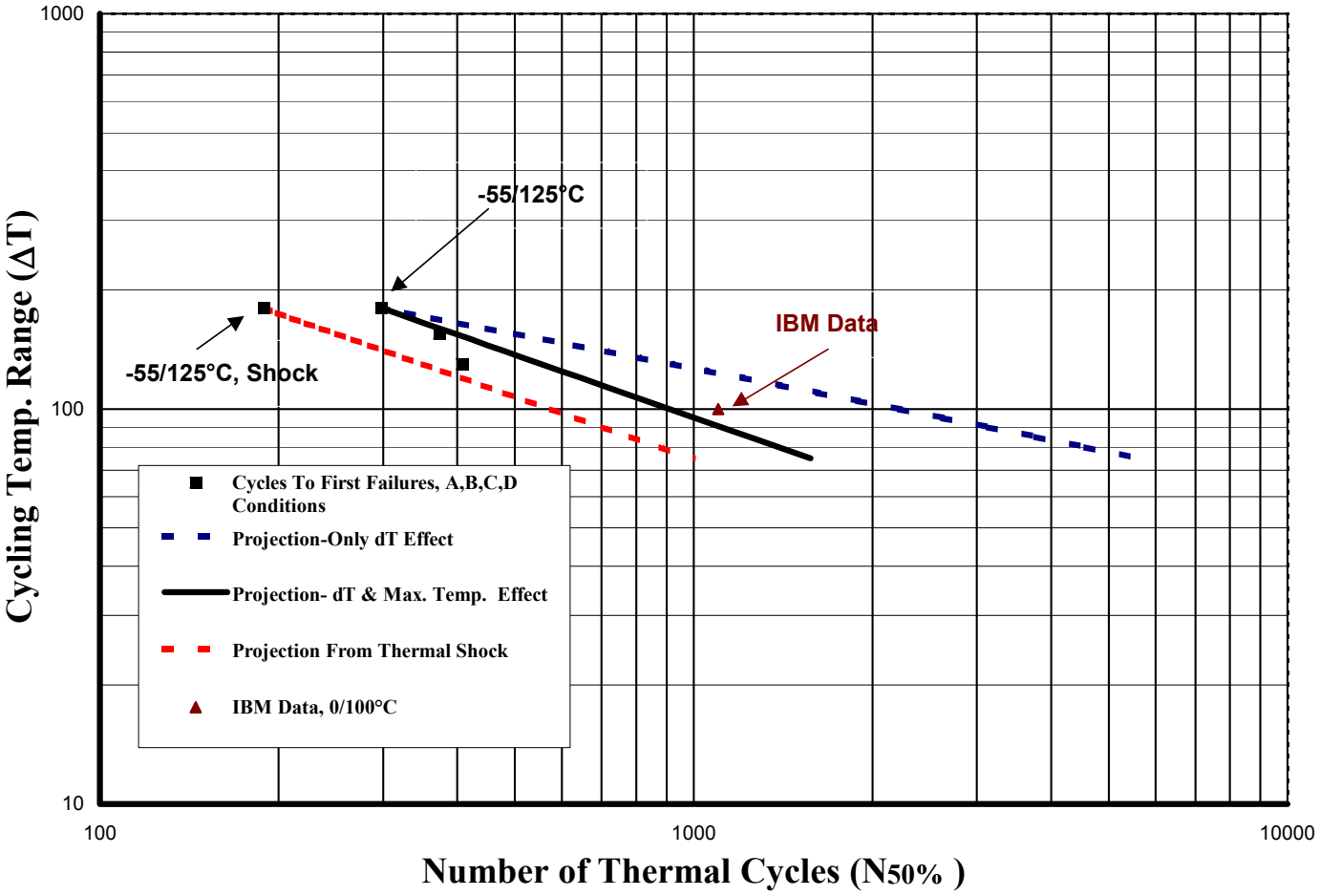

Figure 6 Effect of temperature range on fifty percentile failure cycles for CBGA 625 and projection using modified a Coffin-Manson relationship

Thermal Cycling Results

Figure 5 shows cycles to first failure for CBGA 625 under four different thermal cycling conditions. To generate plots, the cycles to failure were ranked from low to high and failure distribution percentiles were approximated using median plotting position, $F_i = (i-0.3)/(n+0.4)$ (Kapur,1977).

Often, two-parameter Weibull distributions have been used to characterize failure distribution and provide modeling for prediction in the areas of interest. The Weibull cumulative failure distribution was used to fit cycles to failure data. The equation is

$$F(N) = 1- \exp (-(N/No)^m)$$

where

F(N) is the cumulative failure distribution function
N is the number of thermal cycles
No is a scale parameter that commonly is referred to as characteristic life, and is the number of thermal cycles with 63.2% failure occurrence.
The m is the shape parameter and for a large m is approximately inversely proportional to the coefficient of variation (CV) by 1.2/CV; that is, as m increases, spread in cycles to failure decreases

This equation, in double logarithm format, results in a straight line. The slope of the line will define the Weibull shape parameter. The cycles to failure data in log-log were fitted to a straight line and the two Weibull parameters were calculated.

Weibull parameters for cycles to failure were also generated and plotted in continuous graphs in Figure 5. Weibull parameters for the four conditions are listed in Table 2. In addition to cycling conditions, it includes manufacturing and assembly variables that possibly affected the m values.

The widest spread, i.e m=4, was observed for those assemblies cycled under condition D. The other three

conditions had m values ranging from 8.4 to 11.7 with the narrowest spread, m=11.7, for condition C. Near-thermal shock with two hot and cold extreme temperatures and the use of a limited number of test samples are possible causes of low values for m under D condition. Only seven test vehicles were tested, three on polyimide, three on FR-4, and one with solder volume above the norm. Test vehicles tested under condition C were manufactured at another facility under different manufacturing conditions.

Fatigue Equation

The Coffin-Manson relationship is a simple relationship in which cycles to failure is inversely proportional to creep strain. Its modified version includes the effects of frequency as well as the maximum temperature in the form of

$$(N_1/N_2) \propto (\Delta\gamma_2/\Delta\gamma_1)^{\beta} \ (f_1/f_2)^{\kappa} \exp (1414 \ (1/T_1 - 1/T_2)$$

- N1 and N2 are cycles to failure under two plastic strain conditions. β is the fatigue exponential and is generally assumed to be equal to 1.9.
- $\Delta\gamma$ is proportional to (DNP/h) $\Delta\alpha$ ΔT, where DNP is the distance from neutral point, h is equal to the solder joint height, $\Delta\alpha$ is the difference in the coefficient of thermal expansion of package and PWB, and ΔT is the cycling temperature range.
- f_1 and f_2 are frequencies. κ is the frequency exponential varying from 0 to 1, with value 0 for no frequency effect and 1 for the maximum effect, which depends on materials and testing conditions. A value equal to 1/3 is commonly used to extrapolate the laboratory accelerated thermal cycles to failure data with short duration (high frequency) to on/off field operating cycle with long duration (low frequency), i.e. a shorter field cycles to failure projection.
- T_1 and T_2 are absolute maximum temperatures under two cycling conditions

Projections

The above relationship was used to correlate the test results for CBGA 625 generated under the above four thermal cycling conditions. Cycles to 50 percent failure data are shown in Figure 6. Projections to lower temperature ranges from two data points and a single data point using the above relationship were also plotted. Projections were compared to a test result for the same package thermal cycled in the range of 0 to 100°C (Martin, et al,1997). The following key points were considered:

- Effect of frequency– The effect of frequency was considered to be minor since frequency ranges in our study were very similar and their dwells at maximum temperatures were at least 10 minutes. Creep was assumed to be almost complete for the two maximum cycling temperatures of 100 and 125°C. These temperatures are well above the creep temperature of the eutectic Sn/Pb solder.

- Projection from C and B (–55/125°C and –55/100°C) to lower cycling ranges– The projection lines using Coffin-Manson relationship are shown in Figure 6. It includes plots from projection with and without considering the effect of maximum temperature. Projections with correction for maximum temperature better approximate the test results; the test results under conditions C and A, as well as an IBM data point.

- Projection from near-thermal shock data– Cycles to failure under thermal shock conditions were much lower than those under low heating/cooling rate cycling, therefore projection to other temperature ranges provides conservative failure cycles. Characteristic changes in solder behavior under rapid heating and cooling as well as failure mechanism changes for thermal shock conditions may not realistically represent most field applications.

- Projection from –55/100°C and –30/100°C to lower temperatures– This projection is not shown in Figure 6, but it was conservative since the slope between the two data points is much deeper than the slope connecting data sets for –55/125°C and –55/100°C cycles. This means that damage induced by fatigue due to decrease in cold temperature is not as severe as creep induced due to increase in hot temperature.

CONCLUSIONS

- A failure shift from solder joint to package may occur more often for miniaturized CSP packages. Projection based on the wrong failure mode results in the wrong forecast of cycles to failure.

- Near-thermal shock conditions induced the most damage on CBGA assemblies compared to thermal cycling. Up to 50 percent reduction in cycles to failure were observed when heating/cooling rates significantly increased for thermal cycling in the range of –55 to 125°C.

- Increase in the maximum cycling temperature from 100 to 125°C had a more damaging effect than a decrease in the minimum temperature by the same amount (–30 to –55°C) while keeping the ΔT constant. Fatigue, rather than creep, is considered to be the main damage

mechanism below one-half of the absolute melting temperature.

- Cycles to failure can be reasonably projected using a simple modified Coffin-Manson relationship and accelerated thermal cycle test results.
- Understanding the overall philosophy of testing to meet system requirements as well as detecting new failure mechanisms associated with miniaturized package assemblies including CSPs is key to collecting meaningful test results.

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