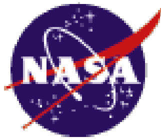

Goddard Space Flight Center
National Aeronautics and Space Administration

Pico-Technology, Inc.

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The High-Speed Potential of Multi-Chip Modules Built with Pico-Strates

An Introductory Study

1. Introduction

In as much as the signal propagation delays between chips or dice are a function of chip interconnection length, multi-chip modules have an inherent advantage over any other form of packaging. However, the full speed potential of multi-chip modules can only be realized to the degree that the electrical quality of the actual interconnects approaches the quality of ideal transmission lines, for which the signal propagation speed is equal to the speed of light. This paper will investigate the transmission line capabilities of multi-chip module substrates in general and that of present and future Pico-strates in particular. Major areas to be considered are the dielectric between the conductors, the resistivity of the conductors, and the configuration-dependant increases of the natural inductances and capacitances in the interconnect system. In parallel, it will be attempted to provide a signal propagation model so that the speed of a substrate with a particular interconnect configuration can be reasonably well predicted by simulation before it is built and tested.

2. The TEM Model

2.1 The Transmission Mode

Recognizing that at least all present Picostrates have interconnect traces riding over a ground plane, it appears natural to compare the traces with the familiar micro-strips on printed-circuit boards and to presume transversal electro-magnetic (TEM) waves. As we shall see, the actual signal propagation is unfortunately more complex, but the TEM model is still useable within carefully staked out boundaries. This is very important because of the readily available simulation tools for TEM waves. A first consideration within this context is the ground plane itself.

2.2 The Ground Plane

Ideally, the ground plane should be infinitely conductive. In that case, it would be a mirror plane for all waves, transversal or not, and it would not contribute to signal attenuation. In reality, the ground plane "thickness" is comparable to that of the traces and its sheet resistance is therefore finite and of the same order of magnitude.

If a signal return current in the ground plane were distributed as it is known for an ideal ground plane, it would flow more or less right under the trace and the impact of the ground plane resistance would be significant. Fortunately, the very same resistance and its consequential voltage drop forces the current outwardly into the plane for a more favorable current distribution. The exact current distribution in the ground plane is not known and warrants a future investigation. However, it has been determined by comparing measured results with TEM-simulated results that the impact of the ground plane resistance can be adequately approximated by a 10% surcharge on the trace resistance as long as the ground plane sheet resistance is equal to the sheet resistance of the trace layer and the pulse transition time is below 1 ns. If the ground plane sheet resistance is, for instance, doubled (layer thickness cut in half), the surcharge rises to 30%. The simple surcharge approximation may also be valid for transition times less than 1 ns, but that has not yet been proven and requires therefore future investigations.

Present Picostrates use ground planes, which have indeed the same sheet resistivity as the signal trace layers. Future parts may be designed with even higher ground plane conductivity. Proposals to replace the solid ground plane with a ground grid for cost reduction purposes must in view of the above results be met with skepticism unless speed is of no concern.

2.3 The Trace Resistance

In presently available Picostrates, the sheet resistance of the M3 layer (lower signal trace layer) is typically 16 mΩ (range 15 to 18). The effective trace width is typically 16 μ m, leading to a trace resistance of 1Ω / mm. This value is consistent with the measured D.C. resistance of the traces.

The high-frequency resistance of the traces could be higher because of the skin effect. For reference, the calculated skin depth of a semi-infinite aluminum wall is 3 μ m versus the trace height of 2 μ m. Another potential problem is that the trace resistance causes longitudinal voltage drops which are large enough to invalidate the TEM model. However, it has been determined by comparison with experimental results that a TEM simulation with the D.C. resistance used as broad band resistance gives good results for pulse transition times down to 1 ns. That this approximation is also adequate for still shorter transition times is possible but has not yet been demonstrated.

The sheet resistance of the M4 layer (upper signal trace layer) is typically 14 mΩ (range 12 to 15). With a typical effective trace width of 12 μ m, the calculated trace resistance is 1.2 Ω / mm. Again, this value is consistent with D.C. measurements and its applicability to TEM simulation has been demonstrated down to 1 ns.

The trace resistance can potentially be reduced by developing thicker metal layers and /or using copper instead of aluminum. It could also be traded against trace capacitance by making the traces wider, but that would not produce any net speed gain as will be shown below.

2.4 Pure and Effective Trace Capacitance

The static capacitance of a single trace versus the ground plane can be reasonably well calculated and also be measured with a capacitance meter at low frequencies (under 200 kHz). Typical values obtained for Picostrates are 0.21 pF/mm and 0.15 pF/mm for M3 and M4 traces, respectively. Since the dynamic current and charge distributions in the ground plane and even in the trace itself are not well known, the quasi-static or low-frequency capacitances are not necessarily useable as broad-band capacitances. However, it could again be shown by experiment that they are fortunately applicable to TEM simulation down to at least 1 ns.

The effective trace capacitance exceeds the pure trace capacitance because of the partial capacitance between the trace and its parallel neighbors in the same plane and because of the partial capacitance between the trace and the orthogonal traces crossing it in the other plane.

In present Pico-strates, the first addition is negligible but the second is substantial. The crossover coupling capacitance between two traces is small, 8 fF without and 16 fF with an antifuse, but the large number of them make them significant. The impact of a crossover is smaller for an M4 trace than for an M3 trace because the "normal" dielectric flux between the M4 trace and ground is reduced by the interposed M3 trace.

A secondary difference between the layers is that an M3 trace sees slightly fewer crossovers per length than an M4 trace, this time favoring the M3 trace.

For a TEM simulation of a trace, the coupling capacitances to the orthogonal traces can be considered as being returned to ground because the ratio of a single coupling capacitance versus the input impedance of the crossing line at the coupling point is very small. Furthermore, the density of crossovers along the trace can be approximated as being constant because the period of the actual density variations is small (0.3 mm).

The effective capacitance, which is the sum of the "normal" capacitance of an isolated trace plus the effect of the crossovers, can also easily be measured as a quasi-static capacitance with a capacitance meter at low frequencies. Typical values are 0.6 pF / mm for M3 and 0.3 pF/ mm for M4. Thus, the relative increases are about 200% and 100%, respectively.

The average density of crossovers with antifuses is 21 per mm for M3 and 23 per mm for M4. Not counting the crossovers without antifuses, we can as a sanity check compute the capacitance of a single crossover by dividing the added trace

capacitance over the number of crossovers, which yields 19 fF for M3 and 7 fF for M4. The true partial capacitance between orthogonal conductors is, of course, identical in both directions. What we see here is the shielding effect explained above.

The target for future Picostrates improvements is clear. The dielectric between the M3 and M4 layers needs to be increased and/or replaced by a dielectric with a lower permittivity. The thickness of the amorphous silicon layer used for the antifuses needs to be increased. The latter is also desirable in order to increase the threshold voltage, which in turn will permit higher operating voltages.

2.5 Trace Inductance

It is very difficult to measure the trace inductance directly. However, it is just as easy to calculate the external quasi-static inductance as it is to calculate the quasi-static capacitance of the isolated trace over a ground plane. "External inductance" is the inductance of the trace / ground plane loop which is attributable to the magnetic field between the conductors. The magnetic field within the conductors is responsible for the "internal inductance". The total inductance is the sum of the external and internal inductances.

The external inductances can be calculated to be 210 pH / mm for M3 and 300 pH / mm for M4. Contrary to the situation on printed-circuit boards or other structures in the macro world, the internal inductance can not be ignored in MCM substrates because the current does not flow close to the surface of the conductors but is rather more or less evenly distributed over the cross-section of the traces. On the basis of a gross estimate, which considers only the M3 trace height of 2 μ m versus the dielectric height of 4 μ m, one should expect an internal inductance which is 25% of the external inductance. Having again compared measured waveforms with TEM-simulated waveforms, we found that a "surcharge" of 30% both for M3 and M4 gives satisfactory results.

2.6 Characteristic Impedance and Attenuation Constant

The determination of the characteristic impedance of a trace as a TEM transmission line is relatively complex, and one should not expect a simple number as it may be the case for the essentially loss-less transmission lines on a printed-circuit board.

The general equation for the characteristic impedance is

$$Z_0 = [\ (R + j\omega\ L) / (G + j\omega\ C)\ ]^{1/2}$$

In the macro world, R and G can usually be neglected, which leads to the simplified equation

$$Z_{00} = [\ L / C\ ]^{1/2}$$

In the case of MCM substrates, one can usually only ignore G, which leads to the equation

$$Z_{01} = [\ (R + j\omega\ L) / (\ j\omega\ C)\ ]^{1/2} = [\ L / C + R / (\ j\omega\ C)\ ]^{1/2} = Z_{00}\ [\ 1 + R / j\omega\ L\ ]^{1/2}$$

Z_{00} can still be calculated and will prove to be a useful reference constant but it must not be confused with the true characteristic impedance Z_{01}, which approaches Z_{00} only for very high frequencies or very small losses.

The two other parameters needed to describe TEM waves, the attenuation constant α and the delay constant D, are generally also complex and frequency-dependent. However, one can again define simplified substitute expressions, which represent exact constants for a loss-less lines, good approximations for lines with small losses, and useful reference constants for lines with significant losses. For negligible shunt conductance G, these definitions are

$$\alpha = R / 2\ Z_{00} \quad D = (\ L\ C\ )^{1/2}$$

For future reference, we introduce further the "critical distance" d_c, which is derived from the primary parameters, and a relative delay constant D_r, which indicates the delay in relation to the speed-of-light delay of 6.67 ps / mm in a dielectric with a permittivity of 4.

$$d_c = \ln 2 / \alpha = 2 \ln 2\ Z_{00} / R \quad D_r = D / (6.7\ \text{ps / mm})$$

From the trace characteristics given above, we can now calculate (surcharges included) the following table for Z_{00} , α , d_c, D, and D_r.

	Z_{00}	α>	d_c	D	D_r
M3, without crossovers	36Ω	0.0157/mm	44 mm	7.6 ps/mm	1.14
M4, without crossovers	51 Ω	0.0129/mm	54 mm	7.6 ps/mm	1.14
M3, with crossovers	21 Ω	0.0262/mm	26 mm	12.8 ps/mm	1.92
M4, with crossovers	36 Ω	0.0183/mm	38 mm	10.8 ps/mm	1.62

Table 1

3. Visualization

The determination of the actual signal propagation delays and the associated signal distortions between any two points in a real net, which is comprised of trunks, branches, drivers, and loads, is a very complex preposition. Fortunately, a good estimate can be derived from TEM simulation on the basis of the parameters developed above. However, a simulation describes only one case at a time and makes it therefore difficult to extract general principles and design guide lines. The subsequent discussion is intended to help with the visualization of general substrate behavior, at least for straight lines, which can then lead to the systematic simulation of categorical configurations.

Fig. 1 looks at the signal propagation delay of a simple transmission line without loads, with a zero impedance driver, and with or without a terminator as required to minimize signal distortion. The curve with the smallest delay is based on the hypothetical speed of light in a medium with a permittivity of 4, which is that of the silicon dioxide used in Picostrates. A different base delay would be valid for other media such as ceramics (much worse), polyimid (slightly better), or partial air (much better). The slope of the delay curve is 6.7 ps / mm as noted in context with Table 1.

The next curve is for a hypothetical transmission line with the finite internal inductance used for the calculation of Table 1 but with no losses due to series resistance. This line is only hypothetical in as much as the internal inductance is caused in a real transmission line by the resistance, which forces the current away from the surface and into the conductors. However, this construction is useful to visualize the result of the fact that the TEM waves in a substrate travel not exclusively in the medium between the conductors as light would do but also inside the conductors. The line may have any length and is envisioned to be terminated with its characteristic impedance Z_{00}.

The next two curves, M3 and M4, consist each of two sections. The lower sections correspond to the delay constants given in Table 1 for the M3 and M4 traces, which means that they recognize the effect of the internal inductance as well as that of the additional capacitance from the crossovers but not yet the effect of the series resistance. Because of this deficiency, the curves are not yet the answer to the general delay question but can get us there in the following way.

Ignore for the moment that our TEM model has only been verified down to 1 ns and presume that a voltage step (zero transition time) is impressed on the input of a long line with series resistance. Then, the TEM analysis will show that the voltage step propagates along the line in such a way that the response at any point is also a step. However, the step is reduced in height and followed by a "tail" which eventually approaches the height of the original step. The delay for the arrival of the initial step is exactly equal to the delay which the hypothetical line would show for any waveform, and the amplitude of the initial step is equal exp ($-\alpha$).

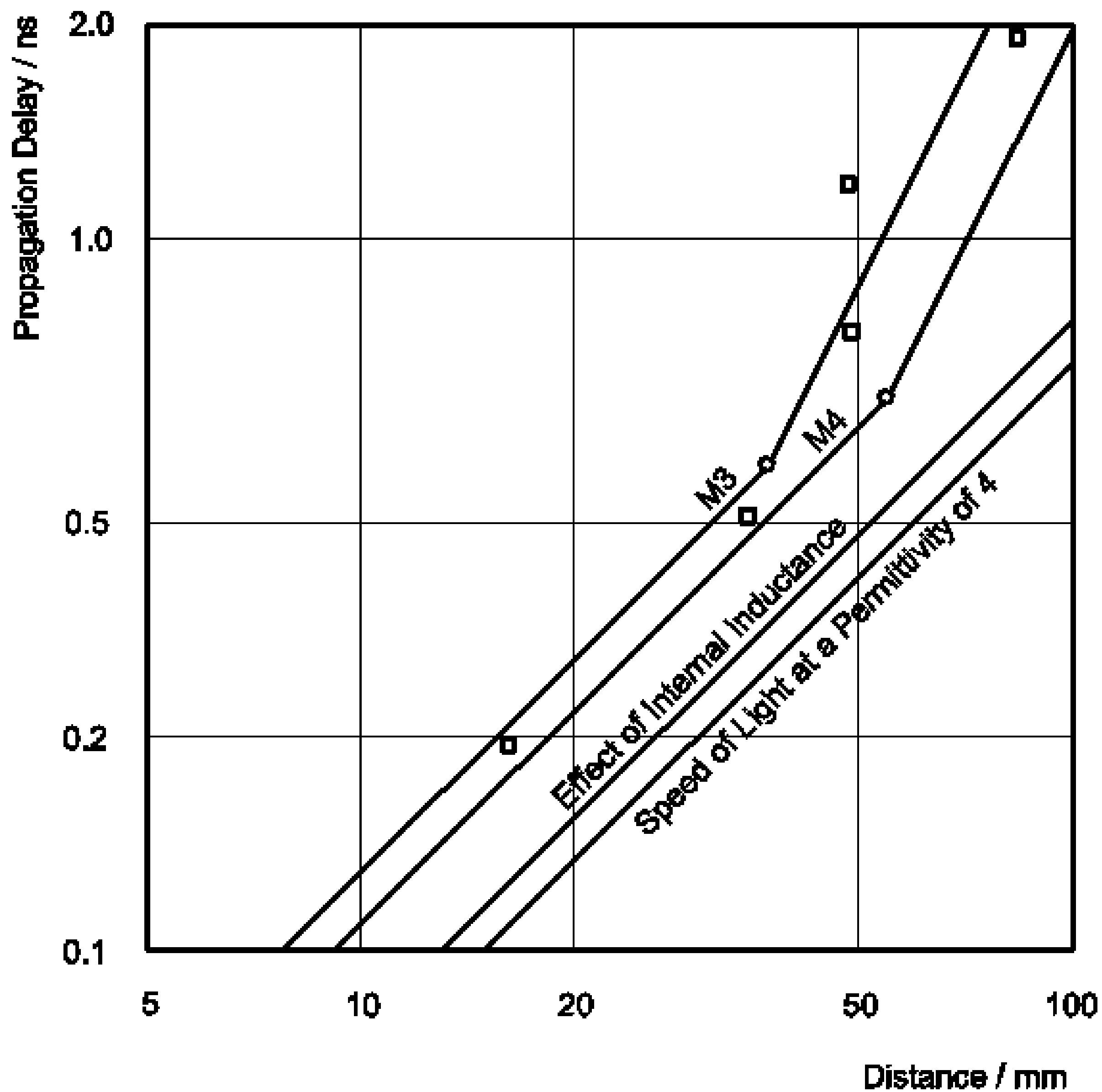


Fig. 1

Let us now define a "digital delay" as the delay at which the waveform at the input of a receiving circuit reaches its threshold, which is assumed to be set to 50% of the full voltage swing. The digital delay is then equal to the hypothetical delay as long as the attenuation does not exceed 50%. The distance at which the 50% attenuation is reached has been defined and calculated before as "critical distance d_c", which is marked in Fig. 1 by circles in the M3 and M4 curves.

The concept of the digital delay becomes more plausible when one considers the line termination. While the loss-less line needs to be terminated with its characteristic impedance in order to preserve the shape of the signal, the serially lossy line is best used with an open end, which means that the actual waveform is the sum of the original waveform and its reflections. Specifically, a line whose length is exactly equal to the critical distance restores the initial step at its end to 100% with the aforementioned tail as a bonus.

With finite transition times, the simulated delays tend to increase somewhat but are still very close to the hypothetical delay towards the end of the line. Thus, the hypothetical delay is indeed a good estimator for the real (digital) delay up to the critical distance.

For transmission lines which are substantially longer than the critical delay we have to look for a different approximation. What comes to mind is the so-called Thomson cable, which ignores the inductance altogether and presumes a transmission line consisting only of series resistance and shunt capacitance. This approximation proves to be way too optimistic for shorter lines but reasonable for longer lines beyond the critical distance. The rational is that L can be

neglected if $(LC)^{1/2}$, the time needed to charge C via L, is small compared to RC, the time needed to charge C via R. In other words, L can be neglected if $(LC)^{1/2} / RC$ is <<1. This condition can be recalculated with our definitions into $d >> d_c / 2 \ln 2$.

For an open-ended Thomson cable, the digital delay of a step function for a line length d is close to $RCd^2 / 2$. For rising transition times, the delay approaches RCd^2. Since the delay varies in either case with the square of the line length instead of proportionally to the line length, the M3 and M4 curves in Fig. 1 have to be continued somewhere beyond the critical distances with twice the slope. The only question is how and where to splice the sections.

It would be nice if we could join the sections right at the critical distance. In order to do that, we would have to satisfy equal delays at $d = d_c$ or

$$D\, d_c = x\, R\, C\, d_c^2,$$

This condition can indeed be met with $x = 1 / 2 \ln 2 = 0.7$, which appears to be a good compromise between the established limits of 0.5 and 1. Therefore, the sections of the M3 and M4 curves in Fig. 1 have been joined at the critical distance point.

In summary, we have now developed an overview for the signal propagation delay in Picostrates albeit without the delay-increasing effects of branch lines, weak drivers, and chip loads. Finally, 5 data points (squares in the graph), which were produced by measurements on real substrates, have been added as a sanity check. These data qualify only as a sanity check and not as an exact verification because they were not taken from simple lines but rather from portions of more complex nets, which were approaching simple lines.

4. The Need for Further Studies

4.1 Systematic Simulation

Fig. 1 explains in a general way and in terms of the underlying physics the delays which can be expected in Picostrates. It is highly desirable to develop a more expansive and more accurate atlas of all kinds of potential delays, recognizing in particular the impact of branches, loads, and transition times. This atlas could be produced by systematic simulation of a significant number of pertinent line configurations.

4.2 Model Verification for Shorter Transition Times

As stated before, the TEM model has been shown to be useful down to 1 ns. It is reasonable to assume that it should work at least to some degree at even smaller transition times. An experimental investigation of the exact limits would be very useful to set up the frame work for future simulations at transition times below 1ns.

4.3 Maximum Clock Rates in Limited Areas

We have so far investigated only delay times but never clock rates. The reason for that is that the substrate controls only the delays, while the clock rates depend in addition to the substrates' signal propagation delays also on the net configuration (linear expansion as well as complexity) and the speed of the active circuits. Let it be mentioned, however, that clock rates of 50 MHz have been implemented on a 75 mm substrate and clock rates of 250 MHz on a 30 mm substrate.

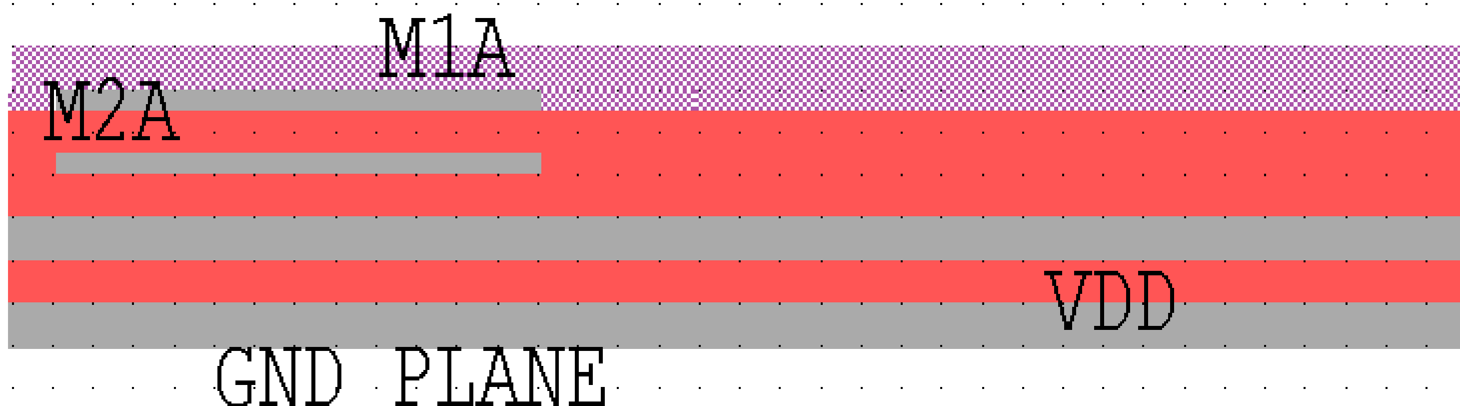
It is reasonable to assume that clock rates of up to 1 GHz can be supported even by present Picostrates over a limited area with a linear dimension of, say, 15 mm. An experiment with limited high-speed circuitry to explore this possibility appears to be desirable. *It is also possible to route signals on transmission line structures mounted on the Picostrate to overcome a routing limitation.*

4.3 Extrapolation to Future Products.

Present Picostrates are based on a process technology, which was developed during the early 90's. In the meantime, new materials have become available and new design ideas for Picostrates have emerged. As these innovations are applied, improved electrical parameters will be realized. Specifically, we expect for the next round of products a reduction of the crossover capacitance and of the line resistance by a factor of 2. This will increase the characteristic impedance, decrease the delay and attenuation constants, and extend the critical distance. It would be desirable to make more specific projections by repeating all of the above analyses on the basis of the improved primary parameters.

5. Conclusion

1. The Pico substrate technology could provide the opportunity for RF and mixed signal rapid prototyping at operating frequencies into the GHz region. This is supported by analysis and logical extension of performance up to 250 MHz
2. Existing models of the substrate technology should be extended to the sub-nanosecond region.
3. Validation and modeling activities using Boundary Element Analysis on coupled transmission line systems, RLCG computations, and S-parameter extraction should be performed by NASA and Pico-Technology in preparation for GHz frequency region validation.
4. The validation activities should be performed on the new production runs of Pico substrates.



4-layer metal cross section of Pico substrate for Boundary Element EM Analysis

6. Concluding Remarks

It is the intent of NASA/GSFC Code 562 to work with Pico-Technology to validate the performance of the substrates in microwave region up to C-band. This would permit the substrates to be used as a platform for circuits such as microwave upconverters, downconverters, automatic gain control, and other useful building blocks for space applications. This work will extend the utility of the 3D-stack substrate development currently under contract with Pico-Technology for the Nanosat program. It is expected that all of the partners in the Sun-Earth Connection missions will benefit from this work.

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