Working Draft- COTS Boards Insertion Methodology and Plan

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Table of Contents

Page

1. Introduction 3
2. Insertion Approach 4
3. Procurement 7

3.1 Manufacturing Redundancy 7

3.2 Single Lot/Lot Traceability 7

3.3 Return Policy 7

3.4 Drawing and Product Specifications 7

3.5 Parts and Materials Lists 7

3.6 Product Change Notifications 8

3.7 Product Characterization Data 8

4. Characterization 8

4.1 Visual Inspection and Part Identification 9

4.2 Radiation 9

4.2.1 Susceptibility Assessment of the Radiation 9

Environment

4.2.2 Application and Mission-Specific Radiation 9

Test Procedures

4.2.3 Proton Testing 9

4.3 Mechanical 10

4.3.1 Resonance Frequencies 10

4.3.2 Random Vibration Board Qualification Testing 11

4.3.3 Maximum Displacement 11

4.3.4 Random Vibration Module Qualification Testing 12

4.3.5 Qualification of the Backplane 12

4.3.6 Acceptance Testing of Flight Box and 12

All its Components

4.4 Thermal 12

4.4.1 Initial Assessment and Thermal Management 13

Feasiblity Study

4.4.2 Characterization 13

4.4.3 Simulation 13

4.5 Chemical/Materials/Contamination 14

4.6 Electrical Characterization 14

4.6.1 Functional Testing 14

4.6.2 Power Consumption 14

5.0 Ruggedization/Remediation/Validation 15

6.0 Reporting 15

Figure 1. Generic COTS Hardware Insertion Methodology 5 & 6

Flow Chart

1.0 Introduction:

The purpose of this document is to show the approach planned for inserting Commercial-Off-The-Shelf (COTS) electronics boards into space flight hardware. The language used herein indicates an insertion philosophy and strategy rather than requirements. This is due to quality and reliability control limitations inherent in COTS hardware. This document does not intend to cover the requirements for qualifying custom designed or custom-built hardware where a much more quantifiable requirement set applies. Thermal, electrical, contamination, mechanical, and radiation issues are discussed. Where possible, lessons learned from the insertion process are included.

This document serves to present a COTS boards insertion methodology and plan and does not directly include procedures, test results and status information. References are made, where possible, to controlled documents that provide this additional information.

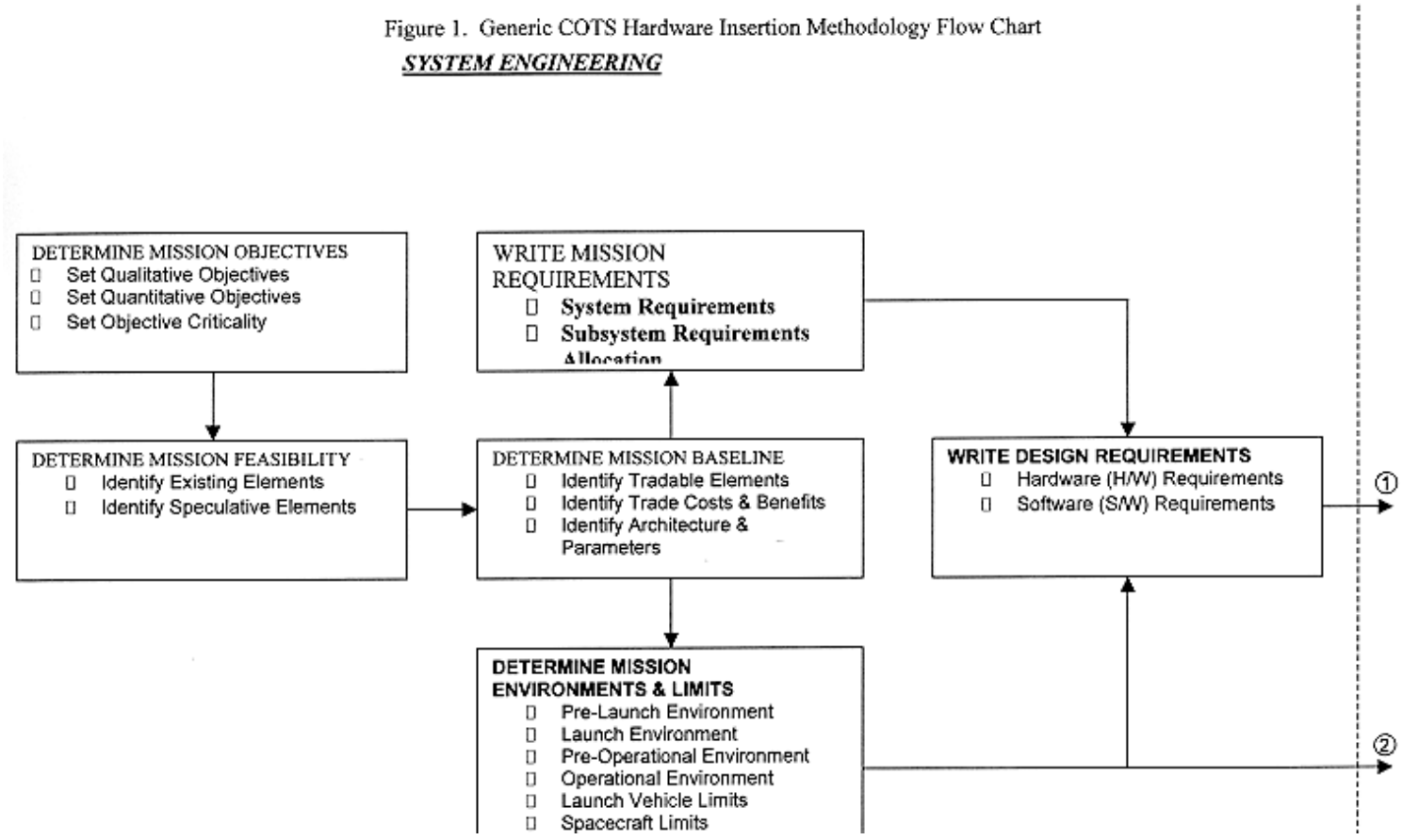
2.0 Insertion Approach:

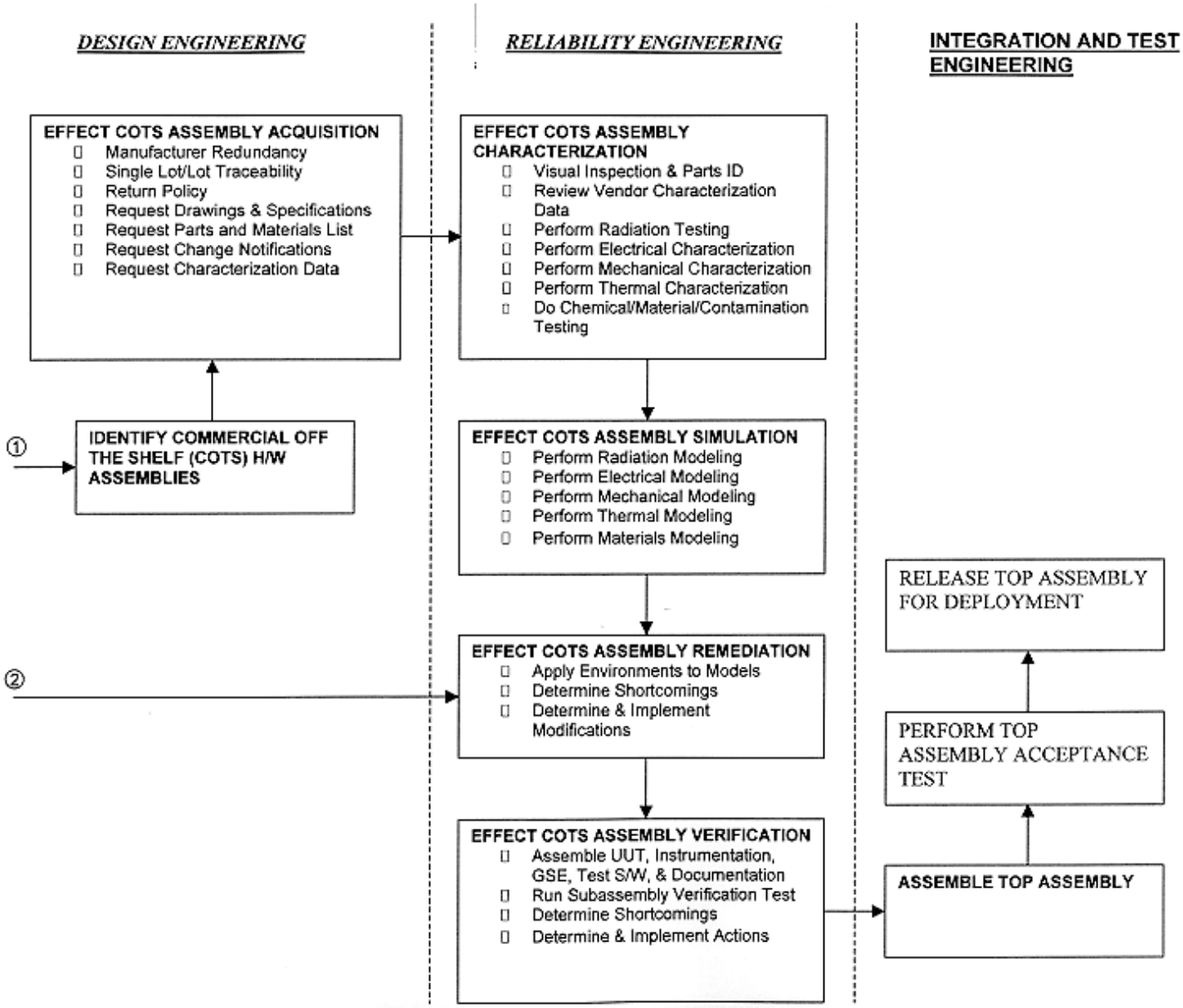
Though COTS can be used to describe a number of levels of hardware integration (dice, part, module, board, box), this project procured hardware at the board level. The strategies and requirements provided herein reflect this level of integration. When inserting hardware at a level of integration that is above or below the board level, some of the approaches and requirements described here must be modified. A unique plan should be developed for these cases.

For a generic COTS insertion methodology a flow chart has been provided in Figure 1. This insertion plan focuses on the Design and Reliability Engineering portions of the flow chart. The Design Engineering portion includes activities association with the procurement of the hardware and the Reliability Engineering portions include characterization, ruggedization/failure mitigation and validation of the as-received hardware.

Characterization includes both theoretical and empirical methods. When the boards are found, through analysis or test, to be incapable of performing as required, a plan and design must be determined that will enable them to do so (or alternate boards must be considered). The theoretical and empirical data will enable the design of ruggedization augmentations such as thermal straps, stiffeners, card guides, and faceplate mounts. Following implementation of these augmentations, an additional validation test must be performed. The same approaches described herein for characterization can be used to verify the acceptability of the ruggedized hardware.

Figure 1. Generic COTS Hardware Insertion Methodology Flow Chart





3.0 Procurement:

-BOARD SELECTION DISCUSSION HERE- Though consistent quality and board-to-part-to-material traceability usually can not be required by the buyer of COTS equipment, the following strategies were used to maximize both at the time of procurement.

3.1 Manufacturer Redundancy. It is impossible to know with sufficient certainty whether or not a COTS system will be able to withstand the rigors of space flight before it is characterized through testing. To realize the schedule benefits which make the use of COTS so desirable, a variety of systems or boards should be procured to increase the chances that the project will have a full compliment of boards to use when the testing is completed.

3.2 Single Lot /Lot Traceability. Wherever possible, single assembly lots and single lot/date codes for components

used in the assemblies, should be requested though it is highly likely it will not be available below the assembly lot level. Sequential serial numbers should be requested.

3.3 Return Policy. The user should be aware of the vendor return policy prior to procurement. In most cases where commercial product is used, flight, spare, and ETU samples are purchased at the same time to avoid delivery driven schedule delays. This however increases cost risks. Depending on the vendor's policies, unopened, unused hardware may be returnable when characterization testing shows critical or unavoidable failure modes or other reasons are found for not using the product.

3.4 Drawings and Product specifications: A thorough review of product specifications, when available, should be performed during the design cycle. Documentation beyond what is available through the marketing literature is often not available. Critical performance parameters, not defined by the manufacturer may need to be requested. Careful consideration must be given to product obsolescence of the higher level assemblies, as well as critical component(s) (i.e. microprocessor and peripheral devices). Significant changes may be made to the product without your knowledge to keep it current with the changing platform environment.

3.5 Parts and Materials List. An "as built" parts and materials list should be requested from the vendor prior to procurement. The purpose of this is two fold. First, potential contaminates can be identified such as outgassing plastics used for connector back shells, epoxies, and cleaning solvents. Second, this allows a parts list review which highlights potential reliability hazards or concerns.

3.6 Product Change Notifications. The user should request to be made aware of product changes that would affect their design. Engineering changes may or may not be adequately reflected by the documentation. It may be the case as well, that documentation such as circuit or layout drawings must be requested or purchased separately.

3.7 Product Characterization Data. The user should obtain all characterization data available from the manufacturer. Depending on a vendor's participation in "high reliability" markets, they may or may not maintain quality or reliability data. Some manufacturers perform acceptance testing and some that ruggedize their products for harsh environments have qualification data to prove the effectiveness of their approaches. Many manufactures of COTS electronics do neither and do not have performance data available.

As COTS find increasing use on flight hardware, historical data will begin to accumulate. At this time this is already occurring and it is prudent to contact NASA and military organization that may have use the products you are considering, to learn about their experiences. It may also pay to consider ISO 9000 certified vendors although this is not a guarantee that the part is suitable for use in space. It is important to remember though that most COTS products are not controlled for quality or designed for reliability and cannot be qualified by similarity.

4.0 Characterization:

The boards must be characterized in order to understand the ability of the "as received" units to withstand the intended application and environment and to understand the engineering challenges associated with providing risk mitigation paths for the hardware. Characterization involves understanding their performance with respect to ionizing radiation, mechanical shock, vibration and temperature. Assessments must also be made with respect to temperature ratings of the boards, increases in ambient temperatures due to self heating, sources of contamination, concerns with respect to use in vacuum, and electrical performance such as power consumption and timing considerations.

Since COTS hardware is normally designed for terrestrial applications which maintain temperatures around 25°C ± 15°C (although "ruggedized" boards and individual parts may have much wider temperature ratings) their ability to withstand the vacuum, thermal, mechanical and radiation environment are unknown until the board is tested. Characterization testing then must be considered to be destructive and extra boards must be procured for it. These destruct units are referred to as Martyr boards.

4.1 Visual Inspection and Part Identification. When the parts are received they should be inspected to verify that they are the hardware that was ordered and to identify any new features not previously identified. Parts and solder joints should be inspected for mechanical, thermal or electrical damage. Contamination or evidence of insufficient cleaning may cause one to reject the use of the hardware. A part map should be be made at this time using available documentation or by hand recording the part numbers shown on the parts. Part numbers which can be identified should be research to identify any known reliability or performance hazards which may be known about the part. Maximum power dissipations and temperature ratings for parts that can be identified should be researched and recorded.

4.2 Radiation. Paragraphs 4.2.1 through 4.2.3 describe issues related to radiation characterization testing and the strategies employed by the Spartan project.

4.2.1 Susceptibility Assessment of the Radiation Environment. Based on the mission launch date, duration and orbit, the radiation environment can be defined. This definition should provide the severity of the proton, gamma ray and heavy ion environment that will allow proper determination of the fluence to use during Single Event Effect (SEE) testing. SEE testing will show if charged particle impacts will cause the electronics to temporarily (upset) or

permanently fail (latchup, lockup, etc.). The environment definition should also describe the total accumulated (electron) dose expected so that the board's ability to withstand deposited charge can be evaluated and/or shielding can be designed. While Total Ionizing Dose (TID) is not an issue for short duration missions in low earth orbits serious risk can be posed by the proton and heavy ion environment.

4.2.2 Application and Mission-Specific Radiation Test Procedures. The test procedure must be based on the conditions of the application and should simulate in-flight usage of the COTS hardware. COTS hardware cannot be "qualified" as a technology like electronic parts are. They must be validated on a lot-by-lot basis so testing must represent the application that the parts will be used in, to the greatest extent possible.

4.2.3 Proton Testing. High fluence proton testing provides data on component susceptibility, rate prediction data and total accumulated dose. High fluence testing is destructive. *(For the Spartan project, 63 MeV incident protons were used with a fluence of 3.8E10 protons/cm^2.)* Low fluence testing is performed on the flight units and is not destructive, however the board is considered to have accumulated total dose. Low fluence testing provides data which gives a reasonable confidence that the flight boards have a radiation susceptibility that is similar to that shown during the high fluence testing.

4.3 Mechanical.

Mechanical qualification of COTS electronics boards is done using both structural analysis and mechanical vibration testing. Resonance frequencies of vibration, random vibration, steady state and transient loading and thermal loading (simulating launch and, if applicable, landing conditions) are applied in the qualification of these items. Excessive deformation, excessive mechanical cycling of the boards and failure of the solder joints are the critical reliability concerns. This is especially the case when the components on the COTS boards are surface mounted. Qualification level vibration testing will not be performed on the actual flight hardware.

These COTS boards were not designed with space flight launch environments considered. A thorough mechanical test evaluation of the COTS boards at board level must be performed in order to identify problems with the boards in their intended configuration. The boards must also be tested at the box level. Structural analysis of the boards includes board-level and box-level evaluations.

Structural Finite Element Models (FEMs) of the boards should be developed for use in all the structural analyses involving the boards or the box enclosure.

4.3.1 Resonance Frequencies. The PC boards should have resonance frequencies of vibration that are sufficiently different than those of the box enclosure in which they are secured so that the resonance frequencies of the boards and box do not couple. If they do couple, excessive mechanical excitation could occur and cause board failure. The mounting position of the boards in the box must be considered when designing the test. Modal testing of each COTS board, using free-free edge conditions should be used as a baseline. This will provide the resonance frequencies of vibration and mode shapes for each board in free-free edge conditions. The FEMs are then adjusted to match the test results. *(SPTN-TEV-112 describes the procedure used for determining COTS boards' resonance frequencies for the Spartan 251 project).*

4.3.2 Random Vibration Board Qualification Testing. Each COTS board will be subjected to board-level 3-axis random vibration qualification testing to characterize the integrity of the boards. These tests are performed in a test fixture designed to secure the boards using the same hardware that will secure the boards in the box and in the same configuration as planned for the box, although the test fixture is more rigid than the box will be. Board preparation steps include: staking the components, soldering in socketed parts, conformal coating of the entire board (except at specified masked off areas) and installation of connectors as applicable. The staking, soldering and conformal coating steps will be duplicated for the flight boards. Care must be taken when applying solder, coating and staking materials so that the temperature ratings of the components are not exceeded.

A full board electrical functional test will be performed after each axis of testing. Careful visual inspections must be made to validate that solder joints are not damaged. Photographs should be taken for this purpose. Concerns about the boards (having almost exclusively surface-mounted components) under vibration are as follows:

- Will board stiffeners need to be added to the boards?

- Will the planned edge restrainers allow too much board reflection?

- Will the cables that attach to the board connectors be too much mass for the boards to handle?

The test results are intended to answer these questions whereupon the process moves into the Ruggedization and Verification blocks of the Figure 1. (*SPTN-TR-008 includes the procedure for random vibration testing used by Spartan 251*).

4.3.3 Maximum Displacement. Maximum displacement of the COTS board is a concern. Clearance between boards in

the backplane must be considered. A random vibration analysis can be performed on the board using the FEM, which includes edge constraints that estimate the fixity that the actual board will have in the box. This analysis will provide a good idea of where to expect the maximum displacement of the board under random vibration loading.

A random vibration test will then be performed on the board with an accelerometer attached to the location that the FEM analysis predicts maximum displacement will occur. The displacement data will be used for the following two purposes: to verify whether or not the two boards will contact during vibration and to update the FEM. The edge conditions simulated in the FEM will be modified so that the FEM random analysis results match the random test results. Sine sweep test data obtained during the test is also used in the adjustment of the edge restraint simulation. *(SPTN-TEV-112 describes the procedure for performing this testing for the Spartan 251 project)*.

4.3.4 Random Vibration Module Qualification Testing. Modules which may be attached to the board should be characterized using board-level, 3-axis random vibration qualification testing. These tests should be done with the module attached to the carrier board and does not require that that the carrier board be electrically functional. These tests are performed in the test fixture designed to secure the boards using the same hardware that will secure the boards in the box and in the same configuration as planned for the box, although the test fixture is more rigid than the box will be. The module components may be staked or soldered where needed. Conformal coating should be put on the boards if needed except at specified masked off areas. Any staking, soldering and conformal coating must be duplicated for the flight boards. Care must be taken when applying these materials so that the temperature rating of the components are not exceeded. The connectors attaching to the carrier board will also be included. Electrical functional tests should be performed on each module after each axis of testing. Careful visual inspections must be made to validate that solder joints are not damaged. Photographs should be taken for this purpose.

4.3.5 Qualification of the Backplane. The backplane should be subjected to 3-axis random vibration qualification testing at the box-level. A survivability test is not required if its configuration, the light weight of the components attached to it and its construction make it sufficiently mechanically robust.

4.3.6 Acceptance Testing of Flight Box and All its Components. The flight unit will undergo Acceptance level random vibration testing.

4.4 Thermal**:**

Thermal characterization is intended to determine the thermal stress on parts and materials due to self-heating, the availability of thermal paths, and the lack of convective cooling in vacuum. Theoretical and empirical analysis must be done to establish the thermal conditions of the flight configuration.

4.4.1 Initial Assessment and Thermal Management Feasibility Study. A review of vendor supplied thermal characterization data concerning the parts and the materials on the COTS boards must be done to identify gaps and deficiencies in that data and to identify potential thermal problems. A feasibility study assessing the use of heat pipes, thermal strapping, and other methods of thermal management must be done to identify ruggedization and remediation limitations (such as space between the boards).

4.4.2 Characterization. Gaps and deficiencies in the vendor supplied thermal characterization data must be rectified by means of thermocouple and infrared imaging temperature measurements. Infrared imaging measures the energy radiated from hot objects. These radiations, which are in the infrared frequency range, can be translated to temperature provided the laboratory environmental conditions and the emissivities of the COTS assemblies are known. Extreme care must be taken when collecting this data to avoid reflected emissions and to isolate the unit under test from cooling mechanisms that will not be available in flight configuration. An understanding of how the camera works and its limitations are critical for making correct temperature measurements.

In flight configuration, the boards are arranged one behind another. This does not allow the infrared camera to see all of the boards and creates a very synergistic thermal environment for the system. Raising each COTS board and module above the others by means of an extender card allows each assembly to be seen, in turn, by the infrared camera. The resulting infrared images identify where thermocouples should be placed to allow temperature measurements to be made when the boards and modules are in flight configuration.

The procedure used to take this data is described in SPTN-PROC-129, Spartan 251 IR Imaging Test Plan. Infrared data is compared to thermocouple data, and computer software available from the infrared camera vendor generations isotherm plots.

4.4.3. Simulation**.** Based on measured temperatures and researched power dissipation data, thermal models must be constructed which are used to predict thermal problems in flight configuration that could not be measured during testing. The results of these models suggest ruggedization and remediation

alternatives.

4.5 Chemical/Materials/Contamination**:**

Since the boards are not designed for use in applications that are extremely sensitive to contamination such as open semiconductor sensors and optical windows, the COTS hardware must be reviewed and tested for sources of contamination and moisture. The first place to collect this data is from the manufacturer where it may or may not be available. If the materials cannot be adequately documented in this way testing is required.

First the boards should be baked out in an oven at the highest temperature allowed by the manufacturer's ratings. This should be done for as long as the schedule will allow (one to two weeks for maximum temperatures of 50°C). An instrumented outgassing test then should be run on the baked out board to verify that the contamination level is acceptable. Following bake outs, the boards should be conformally coated in accordance with NASA standard procedures. Extreme care should be taken to avoid exposing components to temperatures beyond their rating.

4.6 Electrical Characterization:

Electrical characterization testing consists of functional testing and power consumption evaluations. Care must be taken to avoid damage to the boards due to electrostatic discharge during this testing. This portion of characterization also gives another opportunity to inspect the boards visually for defects.

4.6.1 Functional Testing. Electrical characterization of the COTS hardware consists of functional verification and power characterization. Each board should be inserted into the backplane and powered independently to insure no electrical shorts are present. Power can be supplied to the system via a COTS power supply or by using a bench top power supply.

Functional testing of the COTS boards should be preceded by thorough perusal of the manufacturer's documentation. Functional testing should be done using the manufacturer supplied and user developed software to simulate the conditions under which it will actually be applied. User developed software can be provided to enable carrier to processor communication and to functionally test each board. Test cables should be developed to provide input stimulus, to simulate various load conditions and to monitor output of the module under test.

4.6.2 Power Consumption. Power information and board level schematics should be requested from the vendors for system power calculations and circuit interface documentation. Try to obtain worse case and typical power consumption for each COTS board. This will enable one to determine typical power consumption and heat dissipation for thermal modeling and to optimize efficiency of the power supply. Power consumption should be measured with the system in its quiescent and active states. The test software should simulate worse case operating conditions.

Power consumed by the processor in a system configuration should be measured by placing the unit on an extender card that provides output nodes to monitor the current consumption. To measure power consumed by the modules, extender cables should be used between the modules and the carrier. In-line current meters should be used where possible. Current consumption should be measured with each board in an active and in the quiescent state.

5.0 Ruggedization/Remediation/Validation:

Based on the findings during characterization, ruggedization or remediation hardware/software may need to be put in place. Ruggedization refers to hardware or materials added to the COTS system to increase its survivability. Remediation refers to methods for rebuilding the system to increase its survivability. These could include shielding for total ionizing dose, heat strapping or the use of a sealed enclosure and a fan, addition of edge clamps to improve vibration performance or removal of a part and replacement with another. The same techniques used to characterize the hardware should be used to validate that the ruggedization and/or remediation techniques achieve their intended purpose with no unexpected side effects.

6.0 Reporting:

Reporting should be done for all procedures used and to document the results. Procedures should be configuration controlled.