Thermal Cycle Reliability and Failure Mechanisms of CCGA and PBGA Assemblies With and Without Corner Staking

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Abstract

Area Array Packages (AAPs) with 1.27 mm pitch have been the packages of choice for commercial applications; they are now starting to be implemented for use in military and aerospace applications. Thermal cycling characteristics of plastic ball grid array (PBGA) and chip scale package (CSP) assemblies, because of their wide usage for commercial applications, have been extensively reported on in literature. Thermal cycling represents the on-off environmental condition for most electronic products and therefore is a key factor that defines reliability.

However, very limited data is available for thermal cycling behavior of ceramic packages commonly used for the aerospace applications. For high reliability applications, numerous area array packages are available with the same design pattern both in ceramic and plastic packages. This paper compares assembly reliability of ceramic and plastic package with the same I/O and pattern. The ceramic package was in the form of CCGA with 560 I/Os peripheral array with the same pad design as its plastic counterpart. The effects of the following key parameters on reliability of both CCGA and PBGA assemblies were investigated.

- Thermal cycle ranges, –50/75°C, -55/100°C, and -55/125°C
- Corner staking on failure mechanisms for two thermal cycle profiles, –55/125°C and –50/75°C
- Package interchangeability, i.e. using PBGA package on CGA pad design with a larger pad
- Heat sink attachment on the top of package

Packages were assembled on polyimide board and their daisy chains were continuously monitored. Optical photomicrographs were taken at various thermal cycle intervals to document damage progress and behavior. Representative samples along with their cross-sectional photomicrographs at higher magnification, taken by scanning electron microscopy (SEM), are also presented. These were used to determine crack propagation and failure analyses for packages with and without corner staking.

Key Words: ball grid array, BGA, PBGA, thermal cycle, stake, solder joint, column grid array, CCGA, CGA, inspection

Introduction

Advanced IC electronic packages are moving toward miniaturization from two key different approaches, front- and back-end processes, each with their own merits and challenges. Successful use of more of the front-end processes for the back-end packaging, e.g. microelectromechanical systems (MEMS) and Wafer Level Package (WLP), enable further reduction in size and cost. Direct flip-chip die attachment has become the most efficient approach for the 2nd level assembly. If and when the die can be easily screened to produce high yield known-good die, high density boards can be fabricated at low cost to accommodate high I/O with finer pitches, and defects associated with fine pitch 2nd level assembly are minimized. Wafer level packaging solves the known-good die issue by enabling ease of die testing in a package style, but they have other concerns including the I/O limitation, additional cost, and lack robust reliability. From the back-end approach, system-in-a-package (SIAP/SIP) development is a response to an increasing demand for package and die integration of different functions into one unit to reduce size, cost, and improve functionality.

BGAs and CSPs (chip scale package) are now widely used for many electronic applications including portable and telecommunication products. SIP development is the most recent response to further increasing demand for integration of different functions into one unit to reduce size and cost and improve functionality. The BGA version has now started to be extensively implemented for high reliability applications with generally more severe thermal and mechanical cycling requirements. The plastic BGA version of the area array package, introduced in the late ‘80’s and implemented with great caution in the early ‘90’s was further evolved in the mid ‘90’s to the CSP (also called fine pitch BGA) with a much finer pitch to 0.4mm. Now, distinguishing between size and pitches has become difficult for the array packages.

These packages with balls/columns underneath and irrespective of the die/package ratios are now categorized as area array packages in order to be able to distinguish them from the flip chip bare die category. Bare dies have been around for a longer time, but their associated issues- including known good die and difficulty in direct attachment to printed wiring boards (PWB)- have limited their wide implementation. Wafer level packages were introduced several years ago to address the key issues of bare die and take the advantage of package ease of testing and handling. As PWB technology with finer features becomes widely available with lower cost, bare die becomes more attractive.

Extensive work has been carried out by the JPL consortia in understanding technology implementation of area array packages for high reliability applications. These included process optimization, assembly reliability characterization, and the use of inspection tools, including X-ray and optical microscopy, for quality control and damage detection due to environmental exposures. Lessons learned by the team have been continuously published [1-5].

This paper will first provide a summary of most recent assembly reliability data presented on in literature for I/Os

from 255 to 1657 and pitches to 1mm for CBGAs and CCGAs. Then, it will provide details on design and assembly of the experimental test vehicles including the design of printed wiring board (PWB) and solder paste print efficiency using automatic and manual printing. Manual printing using mini stencil was needed in order to have much higher localized solder paste print recommended for CCGAs. Failure mechanism changes due to two different maximum thermal cycle temperatures for the CCGA and PBGA are compared. Finally, thermal cycle data and cross-sectional photomicrographs for these packages under two different thermal cycle regimes are presented.

Literature Review on 2nd-Level CCGA Reliability

Area arrays come in many different package styles. These include plastic ball grid array with ball composition of eutectic 63Sn/37Pb alloy or its slight variation. The ceramic BGA package uses a higher melting ball (90Pb/10Sn) with eutectic attachment to the die and board. Column grid array (CGA or CCGA) is similar to BGA except it uses column interconnects instead of balls. The lead-free CCGA uses copper instead of high melting lead/tin column. Flip chip BGA (FCBGA) is similar to BGA, except it is internal to the package and flip chip die is used.

Three package configurations are popular. These are a) full array; b) staggered array; and c) peripheral array. Plastic packages come in all styles whereas ceramic package are limited to generally full array configuration. Fully populated array packages presents some significant routing challenges if conventional printed wiring board with plated through-hole (PTH) vias are considered for the design. Peripheral plastic packages have been developed to reduce solder joint failures at the die edge as well as to improve routability characteristics. However, for ceramic package there is a lesser need for peripheral array because the CTE mismatch between die and package material is negligible. Most ceramic packages are supplied in full array configuration. The CCGA used in this investigation; however, was a peripheral array since the package pad pattern simulates its plastic package version.

Table 1 lists cycles-to-failure for a number of CCGAs/CBGAs with different configurations, selected from a very limited data reported on in literature. Data were chosen to be able illustrate the effects of a few key parameters on reliability. The following parameters were considered when test data were tabulated even though in some cases specific information was not reported and is missing.

Thermal cycle range, ramp rate, dwell times

- For example, the CT50%F (cycles-to-fifty percent-failure) for CBGA 361 over the range of 0/100°C was 2700 cycles (Case #3); it reduced to 1190 cycles when the temperature range increased to –55/110°C (Case #6)

Package size, thickness, materials, configuration, and I/Os

- For example, compare Case#2 to Case#3, a relatively large reduction in CT50%F is shown when package thickness increased from 0.8mm to 1.2 mm (4535 vs 2700 cycles). When package thickness further increased to 2.9 mm, its CT50%F further reduced, a reduction by 3.2 times relative to the package with 0.8mm thickness. A similar reduction was observed for CCGA 1657 I/Os when the package thickness increased from 1.5 mm to 3.7 mm (Case #13). Reliability will decrease by increasing package I/O since this means increasing distance to neutral point. CT50%F reduced from 4535 cycles to 2462 cycles when I/Os for the 0.8 mm thick package increased from 361 to 625 (Case #2 vs Case #5). Use of higher CTE ceramic materials, in order to better match ceramic CTE to PWB, will also improve reliability. For example, compare Case #6 to the Case #7 for the 361 I/O CBGA assemblies. CT50%F increased from 1190 to 2160 cycles for the HiCTE package.

Die size and its relation to the package size and ball configuration

- The effects of die size and package configuration (full vs peripheral) arrays on reliability are more pronounced for plastic rather than ceramic package assemblies.

PWB thickness, definition of pad, surface finish

- Preferred thickness was defined as 2.3 mm in IPC 9701[6] since it is known that generally plastic packages assembled on thinner PWBs show higher cycles-to-failure. The effect of board thickness for ceramic packages is not well established yet, but its effect may be less critical for column grid array than plastic package assembly, especially when dominant failure is column. .

Single side or double side, relative offset of package on top and bottom

- This is not shown here, but discussed by this author in another paper[7,-8]. Reliability decreased for double-sided PBGA assembly. The author is not aware of any published data on this subject for CBGA/CCGAs.

Table 1 Cycles-to-failure data illustrating the effect of a number of key variables)

Case #	Package (I/O, Pitch)	Pkg Size (die size) mm	Thermal Cycle Condition (ramp, dwell, Cycle/hr)	First Failure	Mean Life ($N_{63.2\%}$)	Comments
1	CBGA-255-1.27	21x21 (1mm substrate)	0 to 100°C (10, 5, 2cycles/hr)	1980 (1% failure)	2426 ($N_{50\%}$)	PWB, 1.55mm Thk Ref. Burrnette (Motorola)
2	CBGA-361-1.27	25x25 (substrate 0.8 mm Thk)	0 to 100°C (3 cycles/hr)	NA	4535 ($N_{50\%}$)	Avg solder paste vol 5,900 mil^3 PWB, 1.57 mm Thk Die 15x10 mm
3	CBGA-361-1.27	25x25 (substrate 1.2 mm Thk)	0 to 100°C (3 cycles/hr)	NA	2700 ($N_{50\%}$)	Note: Increase from die Thk .8 to 1.2 and 2.9, reliability reduction by 1.8 and 3.2 times Ref Master, 1998
5	CBGA-625-1.27	32.5x32.5 (substrate 0.8mm Thk)	0 to 100°C (3 cycles/hr)	NA	2462 ($N_{50\%}$)	PWB, 1.57 mm Thk Ref [9]
6	CBGA-361-1.27	25x25 (substrate 0.8 mm Thk)	-55 to 110°C (2 cycles/hr)	890 (100 ppm)	1,190 ($N_{50\%}$)	PWB, 1.57 mm Thk Ref [10]
7	CBGA-361-1.27-HiCTE Substrate	25x25 (substrate 0.8 mm Thk)	-55 to 110°C (2 cycles/hr)	1,310 (100 ppm)	2,160 ($N_{50\%}$)	Substrate CTE, 12.2 ppm Ref [10]
8	CGA-361-1.27-Interposer	25x25 (substrate 0.8 mm Thk)	-55 to 110°C (2 cycles/hr)	1,350 (100 ppm)	2,320 ($N_{50\%}$))	NTK Interposer CGA PWB, 1.57 Ref [10]
9	CGA-361-1.27- IBM	25x25 (substrate 0.8 mm Thk)	-55 to 110°C (2 cycles/hr)	1,080 (100 ppm)	1,520 ($N_{50\%}$)	Ref [10]
10	CBGA-1681-1.27-HiTCE	42.5x42.5x1.85 substrate)	-25 to 125°C (1, 9min, 3 cycles/hr)	613 (1st failure)	1142 ($N_{50\%}$)	PWB, 93 mm Thk Ref [11]
11	CBGA-625-1.0	32x32x2.4mm (substrate)	0 to 100°C (2 cycles/hr)	NA	740 ($N_{50\%}$)	Ref [12] IBM-2003
12	CBGA937-1.0	32x32x1.5 (substrate) 32x32x2.4	0 to 100°C (2 cycles/hr)	NA	1,860 ($N_{50\%}$) 1,310 ($N_{50\%}$)	Reference M. Ref [12]

13	CCGA1657-1.0	42x42x1.5 42x42x2.55 42x42x3.7	0 to 100°C (2 cycles/hr)	NA	1,530 ($N_{50\%}$) 990 ($N_{50\%}$) 620 ($N_{50\%}$)	Ref [12]
14	CCGA 1657-1.0 Cu	42.5x42.5x 2.55	0 to 100°C (2 cycles/hr)	1660 (1st failure)	2410 ($N_{50\%}$)	Cu Column, solder paste 96.5 Sn3.5Ag Ref [13]

Objectives

The purpose of this investigation was to characterize the reliability of area array packages with 560 I/Os. This included ceramic column grid array and its plastic counterparts with the same peripheral package configuration. A designed experiment was utilized to cover many aspects that are considered to be unique for the potential use of these packages. Solder joint reliability is affected by many variables as briefly discussed in the previous section. The following parameters were either characterized or evaluated as part of the DOE implementation.

- Two pad design, one for CCGA and smaller pads for PBGA attachment. PBGAs were assembled on both pad sizes to evaluate PBGA interchangeability with CCGA.
- Two stencil designs, a relatively thicker mini stencil especially designed for CCGA and a standard stencil to assemble PBGA and other surface mount packages. Solder paste print volumes were measured and their variation shown in graphs.
- CCGA and PBGA Assemblies without and with corner stake adhesive bonds. Corner adhesive bonds are used to improve resistance to mechanical vibration and shock loads.
- Heat straps were added to the top of PBGAs to determine bonding attachment durability of the heat strap.

The assemblies were subjected to three types of thermal cycles. The process and results for CCGA package assemblies are discussed and compared to their PBGA counterparts in the following.

Test Vehicle

Polyimide printed wiring board (PWB) was designed to accommodate two pads configuration, one for PBGA and the other for column grid array. The pad size for the PBGA was 24 mils whereas for the CCGA was 33 mils that they were attached with their traces to their plated through hole, (PTH) vias with 24 mil diameters. The specific pairs of pads were connected through PTH such that these and those connections within a package pair completed daisy chain patterns to be used for solder joint continuity monitoring. Four daisy chains for each package were used for continuous monitoring. Four additional pads were added at each side of the package for manual probing and failure identification to narrower regions. These were used when an overall failure detected through continuous monitoring.

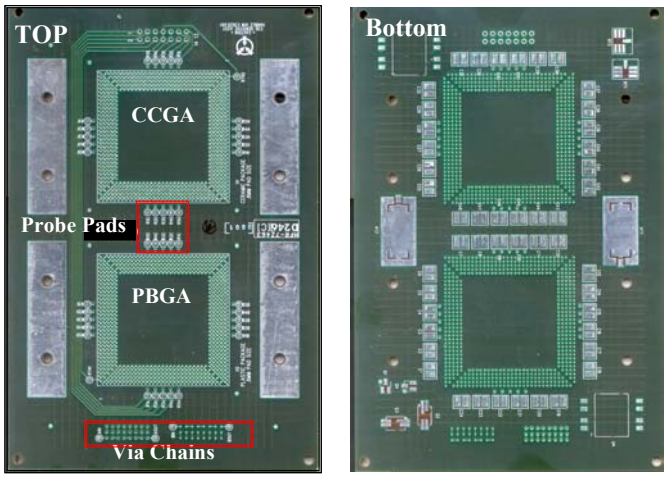

Figure 1 Printed wiring board design showing package daisy chain, probing pads, and via daisy chains

Similarly, two daisy chain sets, each with three rows, using PTH vias representative of the test design were added to monitor behavior of PTHs during thermal cycling. Continuity of the PTH daisy chains was performed manually at each thermal cycle interval when assemblies were removed from the chamber for inspection. PWB's pads had HASL (Hot Air Solder Level) surface finish. HASL and OSP surface finishes are specified in IPC 9701 as the recommended surface finishes for solder attachment reliability evaluation. The key reason for such recommendation is to avoid potential immature intermetallic failures such as those occasionally observed for the Au/Ni surface finish. Because of space availability, additional parts such as leaded and leadless packages and capacitors were added in order to assess their reliability; reliability of these conventional packages is not discussed in the paper. Figure 1 shows the top and bottom of the board design showing daisy chain configurations for package, probing pads, and PTH vias.

Stencil Design, Paste Print, and Volume Measurement

In a previous study, only the 8 mil thick stencil thickness was used to assembly both CCGA and surface mount assemblies. However, to achieve optimum solder paste volume for each part assembly, two stencil types with two different thicknesses were used to meet two solder volume requirements. Much higher solder volume was recommended to be used for CCGAs by the package supplier. Table 2 lists estimated solder paste volumes that can be achieved with different stencil thicknesses and aperture openings. The 7 mil stencil thickness represents the general stencil that could be used for paste application on PBGA and other package pad

patterns. The mini stencil with 10.5 mil thickness was used only for the manual paste print application for CCGA in order to achieve the higher paste volume recommended by the package supplier. Previously, it was shown that higher solder paste volume could improve reliability of CBGAs (ceramic ball grid array) and CCGAs with 1.27 mm pitches. This effect is now being questioned for the CCGAs.

Table 2 Stencil parameter and solder volume

Stencil Thickness	**Solder volume** $(mil)^3$	**Option**
BGA-Aperture 23 mil-Stencil 7mil	2909	Stencil
BGA-Aperture 24 mil-Stencil 7 mil	3168	No
CCGA-Aperture 32 mil dia-stencil 7 mil	5632	Stencil
CGA-Aperture 33 mil dia-stencil 7 mil	5990	No
CCGA- Aperture 32 mil dia- Stencil 8 mil	6430	Stencil (Previous study)
CCGA-Aperture 32 mil dia-stencil 10.5 mil	8440	Mini stencil

An RMA paste, type III (-325+500) mesh was used for paste printing using automatic and normal manufacturing parameter setup for the case of 7 mil stencil thickness. Manual paste printing was performed when the mini stencil was used. Each paste print on PWB was visually inspected after printing for gross defects such as bridging or insufficient paste. Paste print quality was improved by adding paste when insufficient paste was detected and solder paste was removed when bridging condition discovered. Solder paste heights were measured using a laser profilometer. Measurement was carried out at 16 locations that included corner and peripheral center pads in order to accumulate solder volume data and their distributions.

Figure 2 shows plots of solder volume distribution for two different stencil thicknesses (7 and 10.5 mils) and pad opening for the 7 mil stencil thickness. Note the solder paste height measurement was done relative to the PWB surface rather than the Cu pad; therefore, the heights are a Cu thickness higher than their actual values. No adjustments were made when the solder volume was calculated based on the height and the pad diameter. Figure 2 shows distributions of solder volumes for the 16 locations. It is apparent that mini-stencil produced a wider distribution in the solder paste volume that can be achieved through automatic printing. Improvement in distribution was improved slightly after a 2nd manual printing, but distributions are still much wider than in the automatic version.

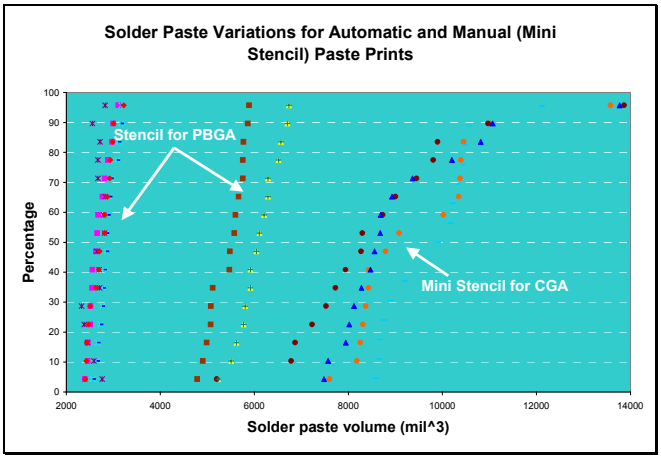

Figure 2 Paste volume variations and the effect of automatic and manual using mini stencil for printing

Designed experiment for Assembly

The objectives and parameters considered in designed experiment were discussed previously. Packages are 42.5 by 42.5 mm in dimension; they are peripheral array with 5 rows and 1.27 mm pitch. CCGA has a 0.2 mm ceramic interposer between package and column and a gap of 0.1 mm between interposer and package. Solder column is a high melt solder with diameter of 0.89 mm and height of 1.62 mm. The plastic package had a cavity down configuration with the die directly attached to an integrated copper heat sink. Solder balls were tin/lead eutectic with 0.75 mm in diameters.

Inspection Before Environmental Tests

For high reliability electronic applications, visual inspection is traditionally performed by Quality Assurance Personnel at various levels of package and assembly, i.e., mandatory inspection points (MIPs). Solder joints are inspected and accepted or rejected based on specific sets of requirements. Further assurance is gained by subsequent short-time environmental exposure, by thermal cycling, vibration, and mechanical shock, etc. These screening tests also allow detection of anomalies due to workmanship defects or design flaws at system level. For space application, generally 100% visual inspection is performed at prepackage prior to its closure (precap) and after assembly prior to shipment.

Visual inspection provides some usefulness for the area array packages, but no value for the hidden balls and columns under the package. X-ray inspection is needed for area array packages even though for CCGAs, the hidden solder joint could not be distinguished because of the heavy ceramic lid that inhibited X-ray penetration[7]. Visual inspection has a higher value for CBGA and CCGA assemblies since generally the solder fails at the exposed corners or periphery ball attachments. Peripheral balls and columns were inspected visually using an optical microscope at the start and during thermal cycling to document damage progress. Figure 3 shows photomicrographs of solder joints of PBGA and CCGA assemblies prior to thermal cycling.

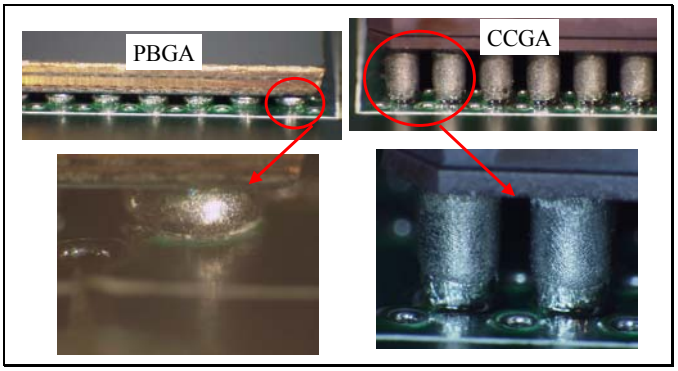

Figure 3 Optical Photomicrographs of PBGA and CCGA after assembly

Thermal Cycle Test

An industry-wide guideline document, IPC SM785, for accelerated reliability testing of solder attachment has been around for more than a decade. Only recently, industry agreed to release an industry-wide specification, IPC9701, in response to BGA and CSP technology implementation[6]. The IPC SM785 guideline, although very valuable and still valid, did not answer the key question of what the data means in terms of product application and data comparison. As is well established by industry and the JPL Consortia [1-5], many variables could be manipulated to either favor or disfavor test results.

Also, in some cases, considerable resources and time could be wasted to generate failure data not related to solder attachment. An example is the use of a surface finish having the potential of inducing intermetallic rather than solder joint failure. This is especially likely for a novice user/supplier.

The IPC 9701 specification, addresses how thermal expansion mismatch between the package and the PWB affects solder joint reliability. In order to be able to compare solder joint reliability for different package technologies, PWB materials (e.g., FR-4), using a relatively larger nominal control thickness to minimize bending (0.093"), surface finish choice to eliminate intermetallic failure (OSP, HASL), pad configuration to eliminate failure due to stress riser (non solder mask defined), and pad size to have a realistic failure opportunity for package/PWB (80%-100 package pad), etc. were standardized in order to minimize their effect on the test results.

The thermal cycle (TC) test ranges, test profile, and the number of cycles (NTC) reported were also standardized. These include the reference cycle in the range of 0 to 100° C (TC1) and a severe military cycle condition of –55 to 125°C (TC4). Three out of five total TC conditions are identical to the test conditions recommended by JEDEC 22 Method A104, Revision A. The NTC varied from a minimum value of 200 cycles to a reference value of 6,000 cycles.

Two different thermal cycle profiles were used. One is the same range specified by IPC9701 and the other one was specific to the mission specific thermal cycle range requirement. These were:

- Cycle A: The cycle A condition ranged from –50 to 75°C with 2-5°C/min heating/cooling rate. Dwell at extreme temperatures were at least 10 minutes with duration of 105 minutes for each cycle.
- Cycle B: The cycle B condition range from –55/100°C with 2-5°C/min. Dwell at extreme temperatures were 30 minutes.
- Cycle C: The cycle C condition ranged from –55 to 125 °C with 2-5°C/min heating/cooling rate. Dwell at extreme temperatures were at least 10 minutes with duration of 159 minutes for each cycle.

The criteria for an open solder joint specified in IPC 9701 were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, there were many additional interruptions within 10% of the cycle life. This was especially true for the ceramic packages. Open was verified manually after removal from the chamber at the earliest convenient time.

Test Results

Figure 4 shows optical photomicrographs of a CCGA assembly after 200 B condition (-55/100°C) thermal cycles. Even though no failure observed yet, but solder joints showed significant damages, especially the joint at the corner column. As stated previously, these were assembled with an 8 mil stencil rather than thicker mini stencil used in the subsequent characterizations. Reductions in solder volume and graininess appearance are other feature of these solders. This is clearly evident from the optical photomicrographs at 200 cycles. Figure 5 shows scanning electron microscopy of the solder and cross-section. Significant cracking both at interposer interface and board solder interconnection is apparent.

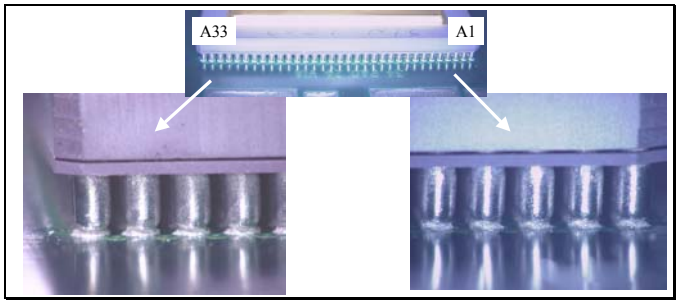

Figure 4 Optical photomicrographs of CCGA built with 8 mil thick stencil after 200 cycles (-55/100°C). Note graininess and solder volume reduction as well as solder column shifts at corners.

Figure 6 shows optical photomicrographs of both PBGA and CCGA after 2937 (-50/75°C) and 478 (-55/125°C) thermal cycles. There is no apparent degradation of the solder joints for both PBGA and CCGA for the A condition where maximum temperature was only 75°C. Even though, most of CCGA assemblies had failed by this cycle; however, the board solder joint interconnects appear to be similar to the pristine condition shown previously in Figure 3. The failures were from package side within package and interposer where it is not visually apparent and cannot be inspected easily. The solder joints at the board interface showed insufficient solder with graininess for the case where the maximum temperature

was 125°C. To the best of the author's knowledge, this feature is not reported on in the literature. The feature changes with cycling for the C condition are similar to the B condition with a 100°C maximum temperature. The PBGA balls exposed to a similar maximum temperature condition did not show this reduction in solder volume

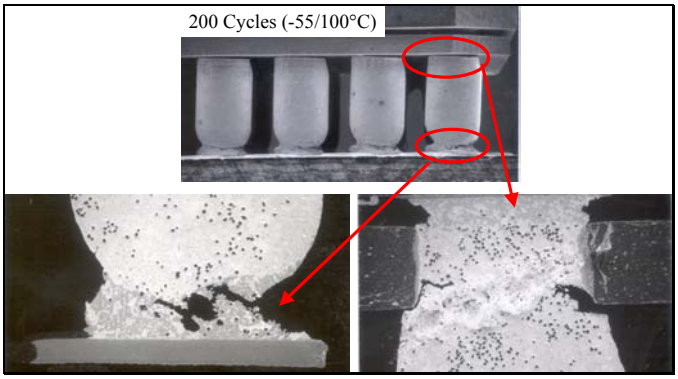

Figure 5 SEM photomicrographs of CCGA built with 8 mil thick stencil after 200 cycles (-55/100°C). Note cracking from board solder joint and interposer interface at package side.

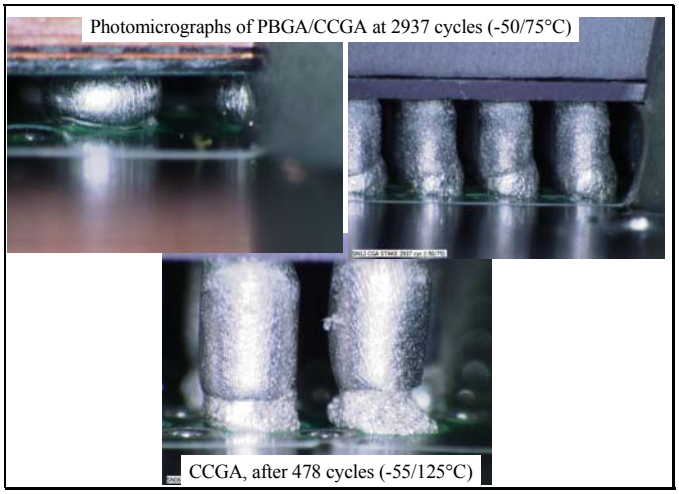

Figure 6 Optical photomicrographs of PBGA and CCGA under two different thermal cycle conditions. Note graininess and solder volume reduction for CCGA exposed at 125°C. CCGAs are built with a 10.5 mil stencil thickness

Figure 7 compares optical and SEM photomicrograph of a PBGA ball after exposure to 1819 cycles (-50/75°C) and another one subjected to 588 cycles in the range of –55/125°C. Both assemblies had corner staked. No significant microstructural changes for the A condition whereas a small microcrack was initiated in the solder joint at the package interface for the C condition (-55/125°C). The latter photo also clearly shows the grain growth due to exposure to elevated temperature. Similar optical photomicrographs for CCGA assemblies with corner staking after the same number of cycles and conditions (1819 (-55/75°C) and 588 (-55/125°C)) are shown in Figure 8. Note that even though both assemblies had corner stake, failure mechanisms were different. One failed away from staking whereas the other (-55/125°C) failed within the staking adhesives at the interposer solder interconnection interfaces.

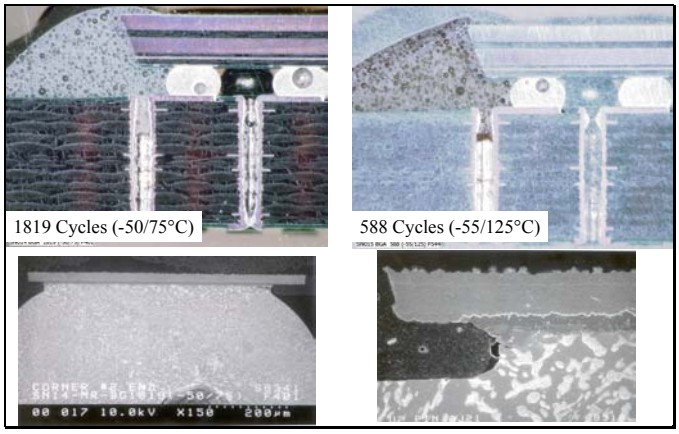

Figure 7 SEM Photomicrographs before and after cross-section for PBGA package after 588 cycles (-55/125°C)

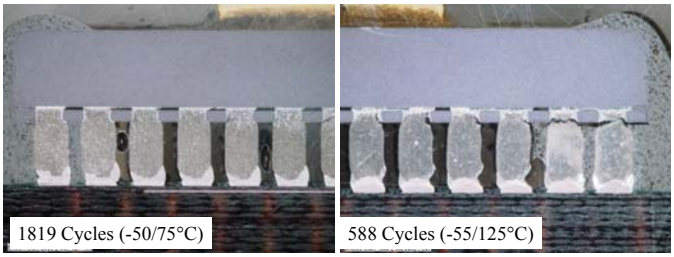

Figure 8 Photomicrographs of column failure at interposer with corner staked over two thermal cycle ranges

Conclusions

It is well established that generally solder joint reliability of plastic packages on polymeric boards is better than that of their ceramic counterparts. This trend was verified through our investigation. In addition, the effects of the following parameters are also identified for a PBGA and its CCGA version that had the same pad pattern and I/Os.

- Plastic package assemblies did not show failures to 2,000 cycles whereas CCGA assemblies showed the first failure at slightly above 1,000 cycles when they were subjected to –50/75°C cycle. The solder ball attachment for the plastic package version; however, did not meet the package level die burn-in requirements generally performed at 125°C for space application.
- CCGA solder joints at the board interface, showed signs of graininess and reduction in volume when they were exposed to thermal cycling with a maximum temperature of either 100 or 125°C. These changes were not observed for the PBGA solder joints or when CCGA assemblies were exposed to a 75°C maximum temperature.
- The PBGA assemblies with the corner stake adhesive showed no additional degradation or changes in failure mechanism compare to those without corner staking when subjected to thermal cycling to 2,000 cycles.

- The CCGA assembly with the corner stake; however, showed changes in failure mechanism. For –55/125°C cycle condition, failures were at the interposer interfaces of those columns that were covered on by the adhesive. For –50/75°C cycle, failures were still at the interposer; however, they were away from those covered by adhesive.

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