

# Implementing SpaceWire Routers as Standard Products using FPGA Technology

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# Introduction



Field Programmable Gate Array (FPGA) devices are often being used for glue logic between complex devices.

With their increasing complexity and operating speed, FPGA devices can now be used to replace these complex devices (e.g. processors), allowing unprecedented flexibility and adaptability.

Application Specific Standard Products (ASSP) have traditionally been based on ASIC technology.

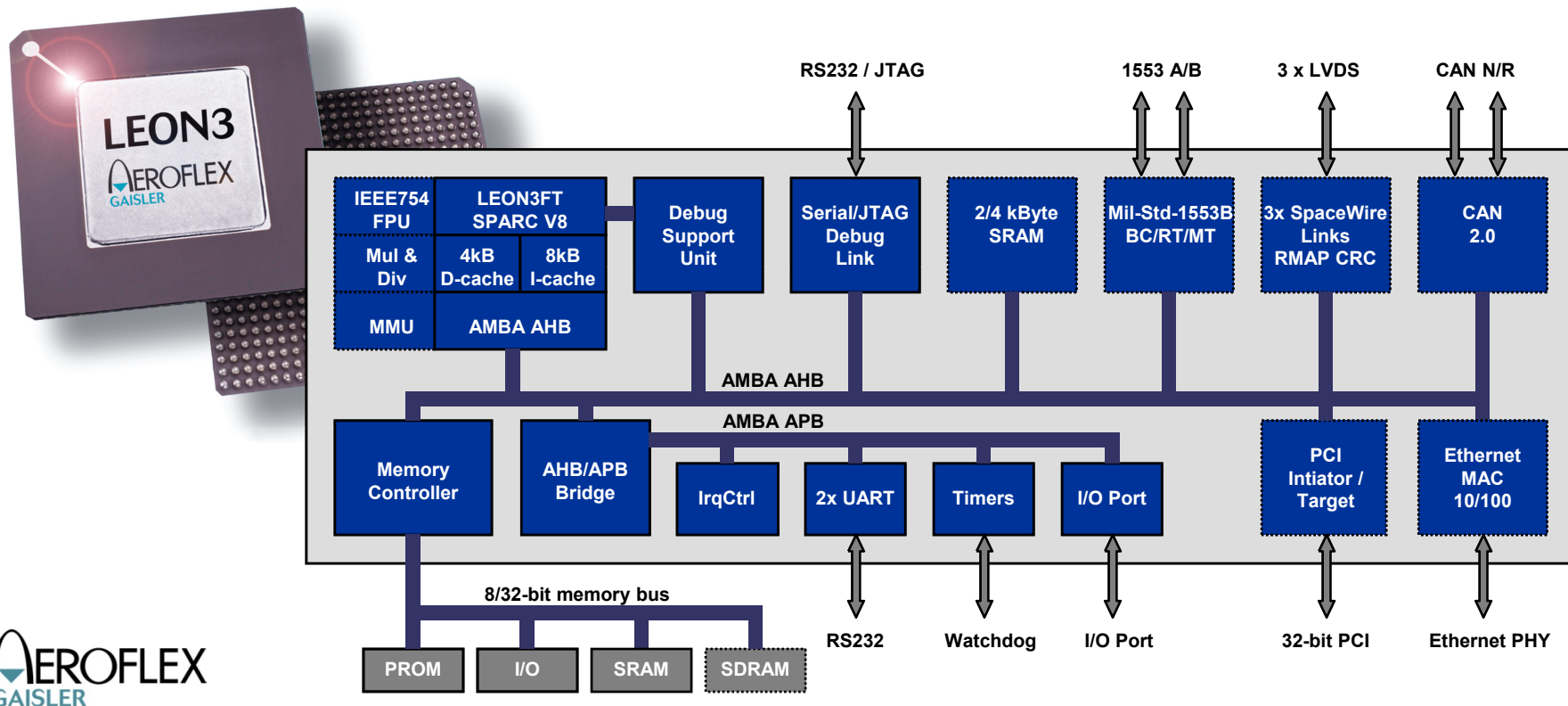
Our approach is to base standard products also on new FPGA technologies, taking advantage of the technology evolution as well as being able to provide users with a greater variety of products.

Our FPGA based ASSP approach, being technology independent, has the advantage of also being portable to ASIC or custom IC design solutions to meet the increasing demands of the future.

# LEON3FT-RTAX/RT3PE family



The LEON3FT-RTAX/RT3PE processor family is based on a common architecture, featuring a rich set of interfaces and configuration options. All configurations are implemented in Actel RTAX2000S(L) or RT3PE3000L FPGA devices and shipped in CQ352, CG484 or CG624 packages.

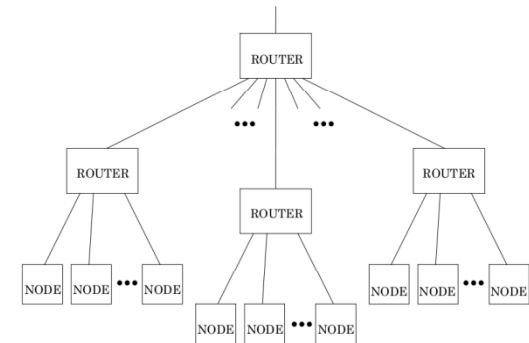


# SpaceWire routing switch



SpaceWire routing switches are an integral part of most SpaceWire networks and some are available as discrete components or IP cores from several providers.

Aeroflex Gaisler has developed a highly configurable SpaceWire router VHDL IP core to meet the needs for technology independent router designs. It is fully compliant to the ECSS standards.

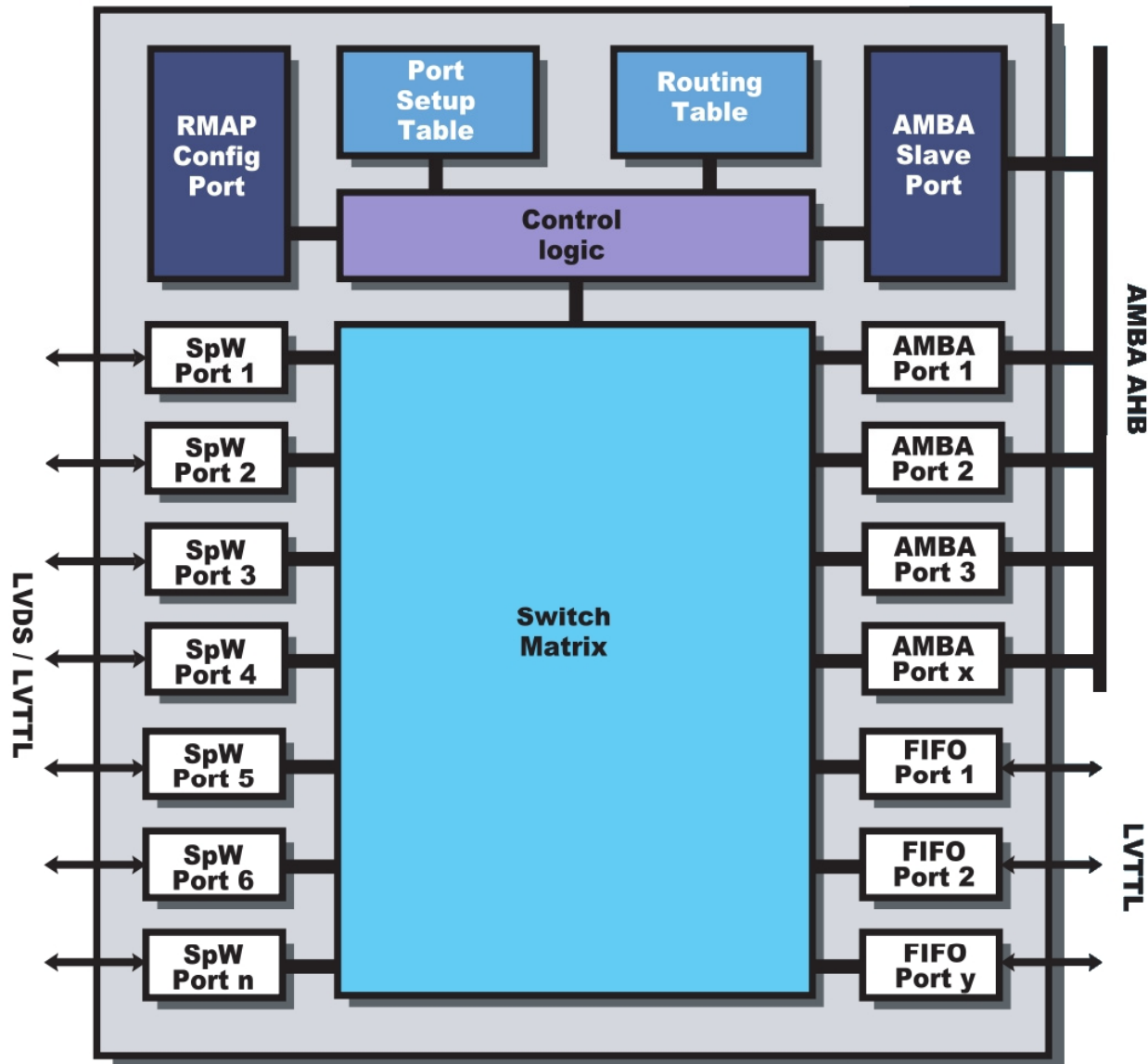


*SpaceWire network example*

Main design goals have been configurability, technology independence, support of all standard features and expandability.

The Aeroflex Gaisler SpaceWire router IP core has been used to develop ASSPs using Actel FPGA technology.

# SpaceWire router IP block diagram



# Router ports



The SpaceWire router IP core can have 2 to 31 ports (in addition to the configuration port).

Up to 31 ports can be external SpaceWire links.

Up to 16 ports can be AMBA AHB based DMA engines.

Up to 31 ports can be FIFO interfaces (e.g. external).

AMBA AHB slave ports are based on the GRSPW2 IP core and can optionally include an RMAP target.

The FIFO interfaces are 9-bit parallel interfaces with configurable FIFO depth.

The number of ports cover the range allowed by the standard (ECSS-E-ST-50-12C).

# SpaceWire ports physical interface



Uses the Aeroflex Gaisler SpaceWire codec IP core.

Supports several input and output physical layer implementations.

Input: Self-clocking (XOR),  
SDR sampling, DDR sampling,  
Aeroflex external SpW transceiver (UT200SpWPHY01)

Output: SDR, DDR,  
Aeroflex external SpW transceiver (UT200SpWPHY01)

The various interfaces have different features making them suitable for different technologies and link speeds.

# Configuration port



Uses port 0 as defined in the SpaceWire standard (ECSS-E-ST-50-12C).

Uses RMAP command for read and write accesses (ECSS-E-ST-50-52C). Configuration registers and routing table are located on a static range of RMAP addresses.

The SpaceWire router IP core configuration area can also be accessed through an AMBA slave interface in SOC designs.

<i>First byte transmitted</i>			
	Target SpW Address	....	Target SpW Address
Target Logical Address	Protocol Identifier	Instruction	Key
Reply Address	Reply Address	Reply Address	Reply Address
Reply Address	Reply Address	Reply Address	Reply Address
Reply Address	Reply Address	Reply Address	Reply Address
Initiator Logical Address	Transaction Identifier (MS)	Transaction Identifier (LS)	Extended Address
Address (MS)	Address	Address	Address (LS)
Data Length (MS)	Data Length	Data Length (LS)	Header CRC
Data	Data	Data	Data
Data	...	...	Data
Data	Data CRC	EOP	
<i>Last byte transmitted</i>			

*RMAP write command example*

# Routing switch matrix and capabilities



Each port can be connected to any of the other ports through wormhole routing.

Instead of duplicating the routing table a single one is used with pipelined access. Performance penalty only if the majority of the packets are very small and arriving simultaneously. Single routing table leads to reduced area.

All the routing features in the SpaceWire standard are supported (ECSS-E-ST-50-12C), with additions:

- Header deletion and individually assignable ports are configurable for each logical address.
- Port setup register provided for each physical or logical address which can be used to configure the router to send the packet on the nominal destination port or any port marked as equivalent.
- Support for packet distribution. Each logical or physical address has a register which determines to which ports (one or more) the packet will be sent.

# Product matrix



	RT-SPW-ROUTER-10X	RT-SPW-ROUTER-6X
SpaceWire ports	8	4
FIFO ports	2	
AMBA ports with RMAP		2
Configuration port with RMAP	Yes	Yes
Configuration port with AMBA		Yes
PCI Initiator/Target		Yes
AMBA status		Yes
UART/JTAG Debug Link		Yes
FPGA	Actel RTAX2000S(L) CQFP352,CCGA624	Actel RTAX2000S(L) CQFP352,CCGA624
	Actel RT3PE3000L CCGA484	
SpaceWire physical interface	LVTTL	LVTTL
	LVDS	LVDS

# SpaceWire Router 10x



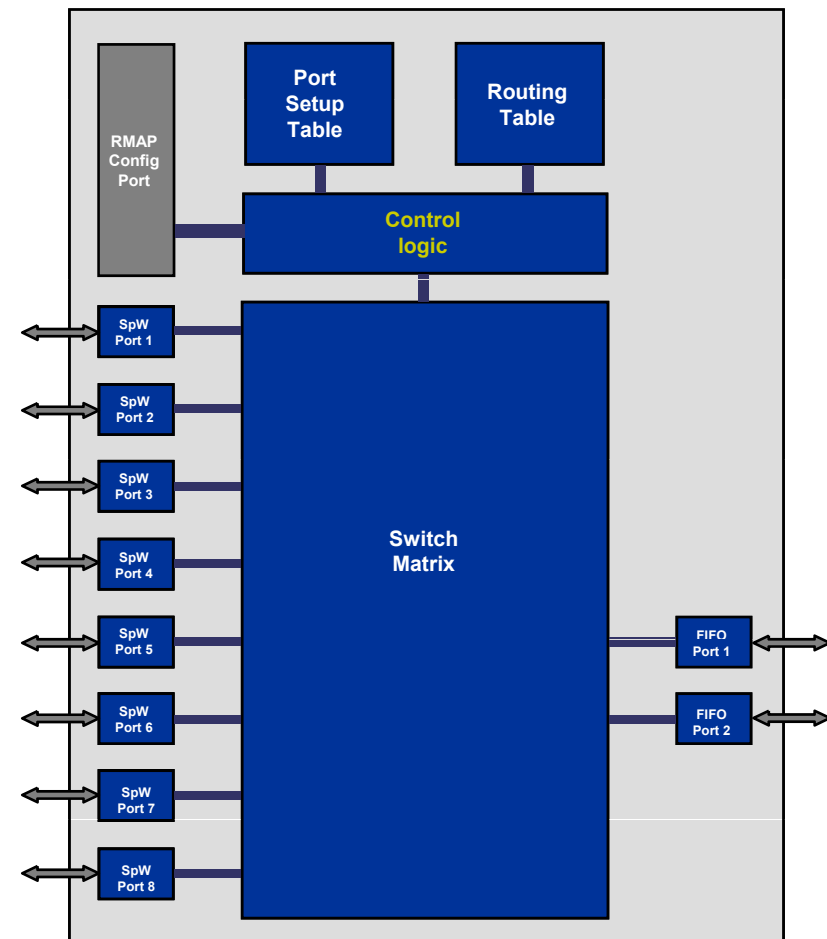
Synthesis and place&route results have been obtained for the targeted FPGA technologies:

Ports: 8 SpaceWire ports,  
2 FIFO ports

Area: 92% of Actel RTAX2000S  
Speed: 200 Mbit/s on SpaceWire links

Area: 82% of Actel RT3PE3000L  
Speed: 100 Mbit/s on SpaceWire links

Clocks: 200 MHz RX  
100 MHz TX  
25 MHz system  
(e.g. UT7R995 clock generator)



# SpaceWire Router 6x with PCI



Synthesis and place&route results have been obtained for the targeted FPGA:

Ports: 4 SpaceWire ports,  
2 AMBA ports with RMAP target,  
PCI initiator/target

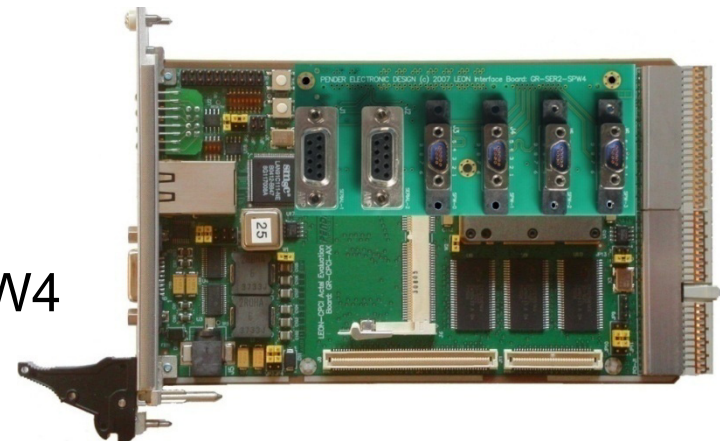
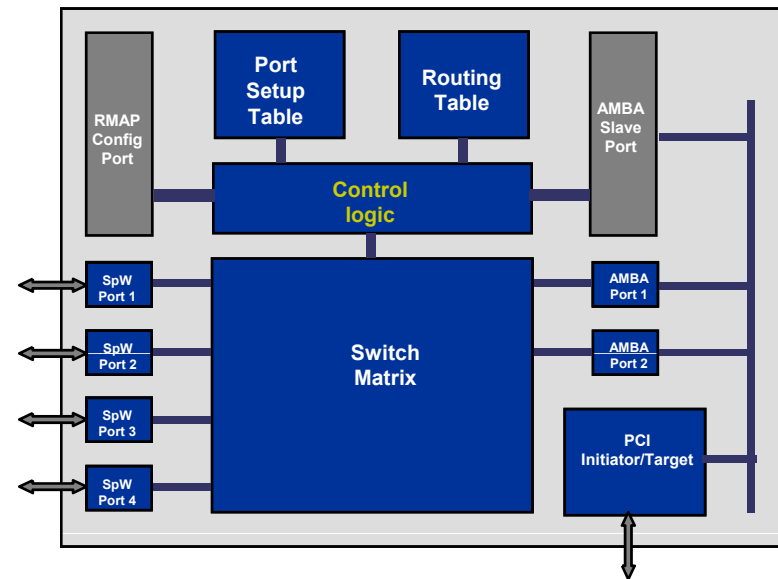
Area: 87% of Actel RTAX2000S

Speed: 200 Mbit/s on SpaceWire links  
33.3 MHz PCI operation

Clocks: 200 MHz RX  
100 MHz TX  
33.3 MHz system  
(e.g. UT7R995 clock generator)

Prototyping board available:

GR-CPCI-AX2000 & GR-SER2-SPW4



# Comparison



	RT-SPW-ROUTER-10x	RT-SPW-ROUTER-6x	AT7910E 10x-SpW	UT200SpW4RTR 4x-SpW
SpaceWire ports	8	4	8	4
External / FIFO ports	2		2	1
AMBA ports w. RMAP		2		
PCI Initiator/Target		Yes		
Configuration port w. RMAP	Yes	Yes	Yes	Custom
Configuration port w. AMBA		Yes		
Group adaptive routing	All ports	All ports	All ports	Single port
Packet distribution	All ports			
Timers	Yes	Yes	Yes	
SpaceWire physical interface	LVDS or LVTTL	LVDS or LVTTL	LVDS	LVDS
Software compatibility with SpaceWire IP cores		Yes		

# Conclusions



The Aeroflex Gaisler SpaceWire router is a highly configurable and technology independent core. It supports all functions of the SpaceWire standard with additional features.

The SpaceWire router can easily be expanded through one or more AMBA interfaces connected to the router ports, allowing access to existing IP cores, such as Mil-Std-1553B, CAN bus or Ethernet MAC (or PCI as used in the 6x SpaceWire router).

As an alternative to on-chip or external LVDS drivers, an external SpaceWire physical transceiver (UT200SpWPHY01 from Aeroflex) can be used to implement the physical layer.

On customer request, a 12x SpaceWire router with 100 MBPS support can also be implemented in an RT3PE3000L device.

The 10x and 6x SpaceWire routers are available for ordering.

# General contact information

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- SpaceWire / LEON3 / GRLIB information:  
<http://www.Aeroflex.com/Gaisler>
- RT-SPW-ROUTER-10x/6x data sheet and user manual:  
<http://www.Aeroflex.com/Gaisler>
- LEON3FT-RTAX-S data sheet and user manual:  
<http://www.Aeroflex.com/Gaisler>
- LEON3FT-RT3PE data sheet and user manual:  
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