

MAPLD NOVEMBER 2010

# ATF280F Rad Hard SRAM Based Dynamic Partial Reconfiguration



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## Overview

- **SRAM based FPGA ATF280**
  - NO MITIGATION, Radiation Hardened By Design
  - In-Equipment or In-Flight reconfiguration
  
- **AT697, SPARC V8 Processor**
  - 0.7W @100MHz
  
- **Reconfigurable Processor**
  - Multi-Chip Package
  
- **Partial Dynamic Reconfiguration**
  - Study done by EADS under CNES request with ATMEL support



## Atmel Radiation HardenING By Design

### ■ Layout rules

- Improved to avoid multiple nodes charge collection during a single heavy ion impact

### ■ SEU hardened Memory points

- Core cell Flip-Flops, embedded memory, configuration memory based on radiation hardened Flip-Flops

### ■ Controller protected by classical TMR

- Including combinatorial logic and flip-flop of all states machines

### ■ Clock and reset trees

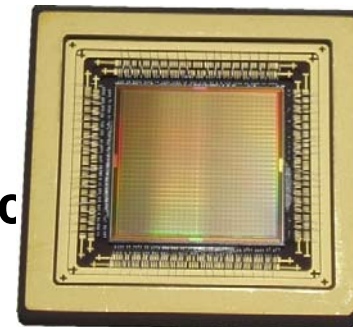
- Protected by DMR (resistive isolation path based on N and P isolated path carrying the same signal)

### ■ Your Design is radiation Hardened by construction

- No need for SEU/SET mitigation

## ATF280F Key Features

- 280K equivalent ASIC gates
- 50MHz maximum system clock
- 14400 core-cells (each 2 LUT + 1 DFF)
- 115 Kbit FreeRAM (900 modules of 32x4 blocks)
- 1.8V Core / 1.8V and 3.3V I/Os
- Dedicated LVDS buffers: 8 Rx + 8 Tx
- Cold-sparing and 3.3V PCI-compliant I/Os
- Radiation
  - TID tested up to 300Krd
  - no SEL up to LET of 76 MeV/(mg/cm<sup>2</sup>)
  - no SEU up to LET of 30 MeV/(mg/cm<sup>2</sup>)
  - no SET up to LET of 43 MeV/(mg/cm<sup>2</sup>)



## SPARC V8 AT697F

- **SPARC V8 LEON2-FT Integer and Floating Point Unit**
  - Embedded Instruction and Data caches (Icache : 32Kbytes; dcache : 16 Kbytes)
  - EDAC protection for external memories (PROM, SRAM, SDRAM)
  - SDRAM memory controller
  - PCI 2.2 interface (33 MHz)
  - Easy to use Debug Support Unit
- **Fault tolerance by design**
  - Triple Modular Redundancy with natural skew or controlled skew
  - EDAC on register file
  - Multiple parity bits on the caches
- **Radiation**
  - TID tested up to 300 Krad
  - no SEL up to 80 MeV.cm<sup>2</sup>/mg@125°
  - no SEU up to LET 30MeVxcm<sup>2</sup>/mg
  - no SET up to

## ■ Multi-Chip Package with

- [illegible]

- **What support AT697F and ATF280!**

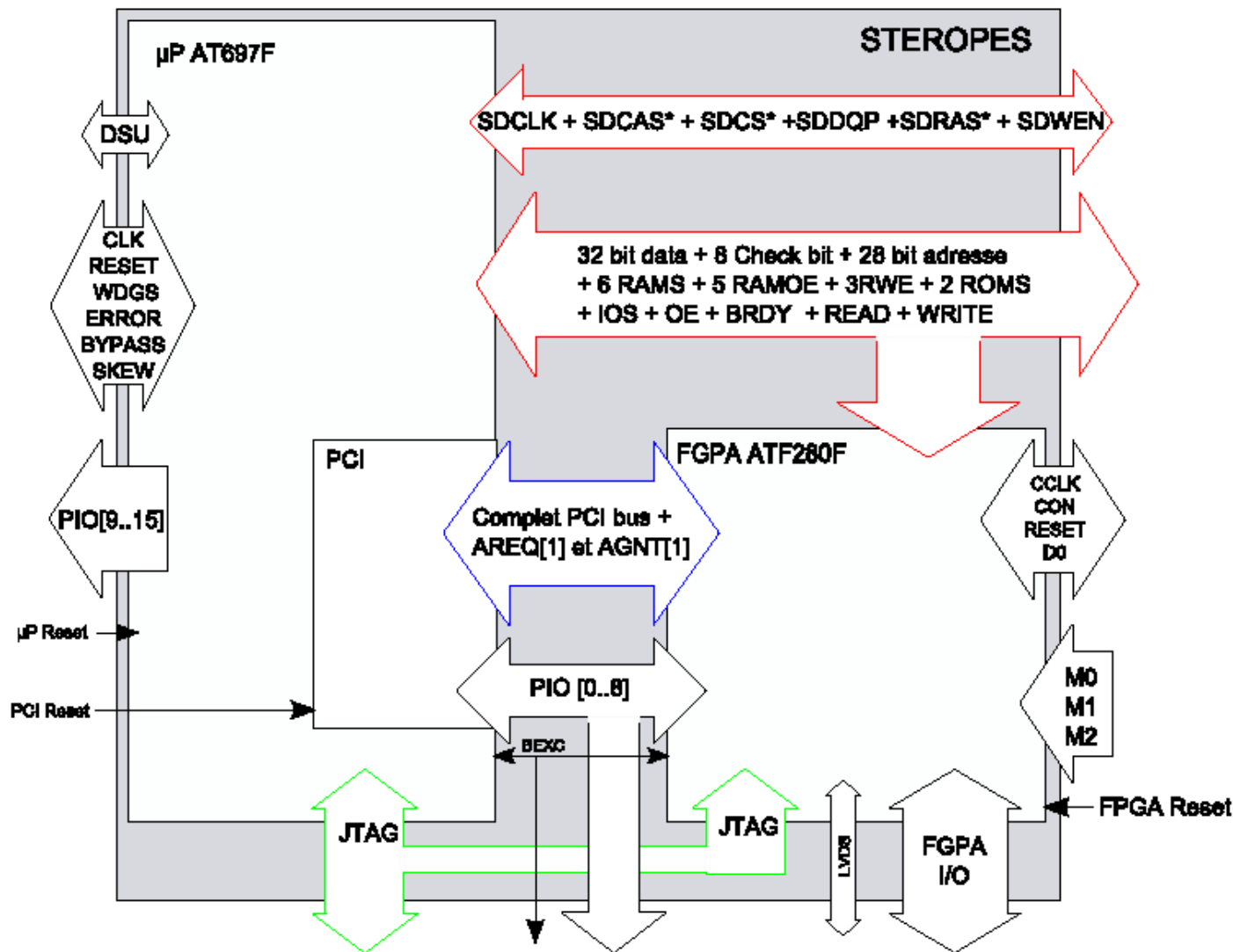
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## Reconfigurable Processor Synoptic



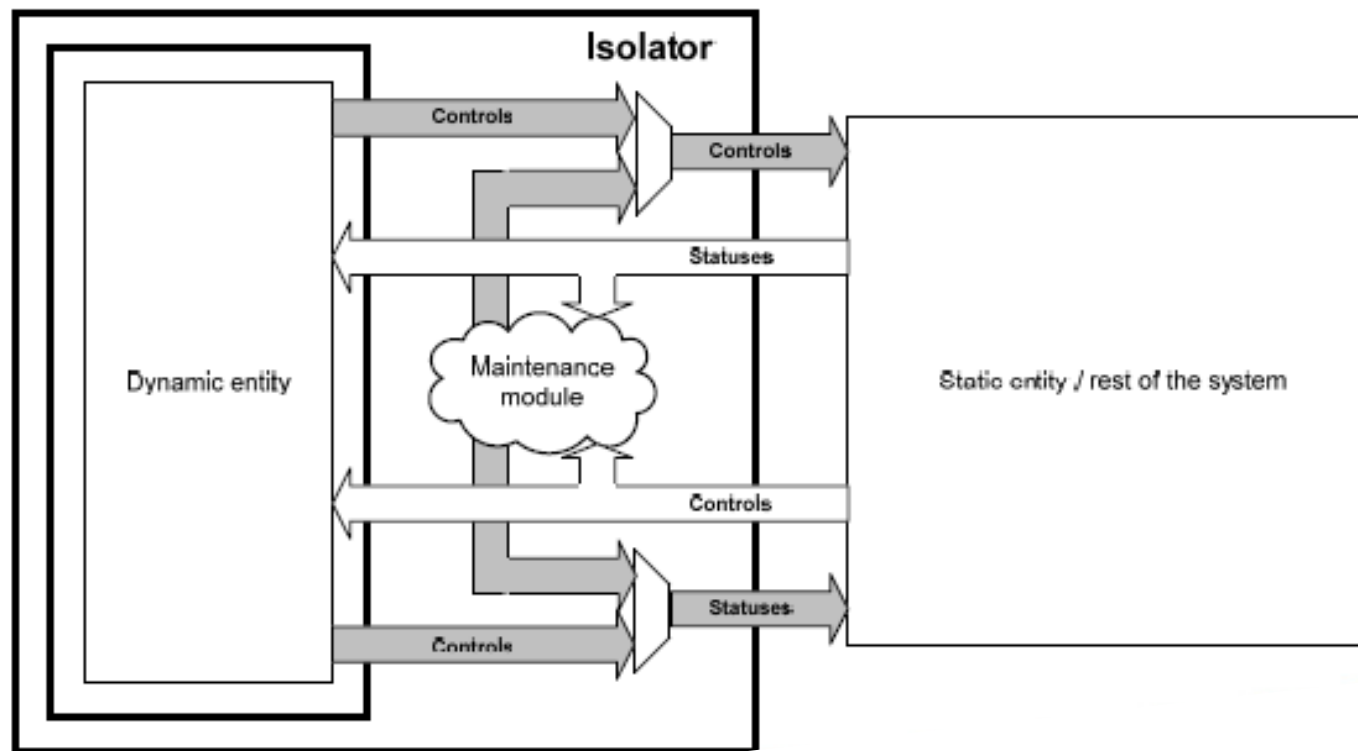


## RECONFIGURATION

### ■ Why Reconfiguration

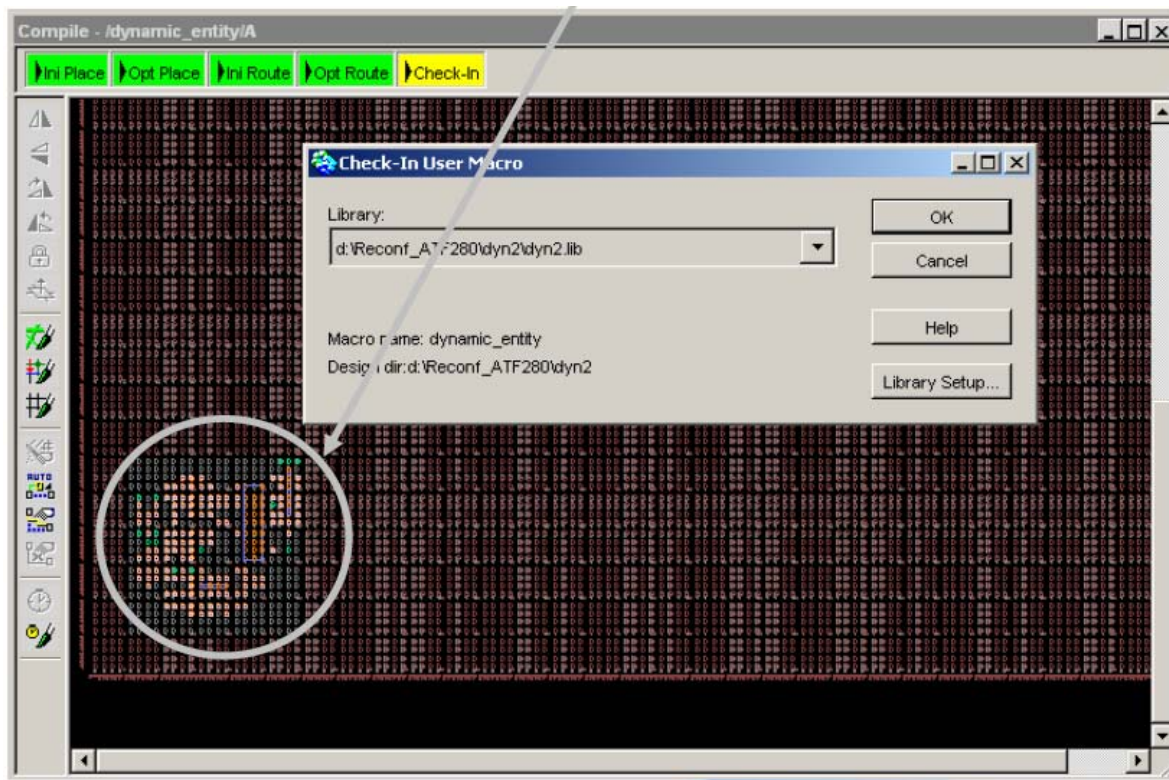
- **Last Minute Design Modifications**
  - Flight Model Equipment delivery
  - Single 2/4 bit connector
- **Experimental Satellites**
  - Multiple Missions
  - Missions Updates
- **Telecommunication Satellites**
  - Growing Satellites lifetime (10y → 15y → 18y → 20y → ...)
  - Obsolescence or evolution of Telecommunication Standard
  - Correction or adaptation of functions

- **Static entity may be disturbed by dynamic entity**
  - Dynamic entity is not available
  - Dynamic entity can trigger events
- **Dynamic Partial Reconfiguration**
  - Redundant Configuration EEPROM
  - Galvanic Isolation of the dynamic entity

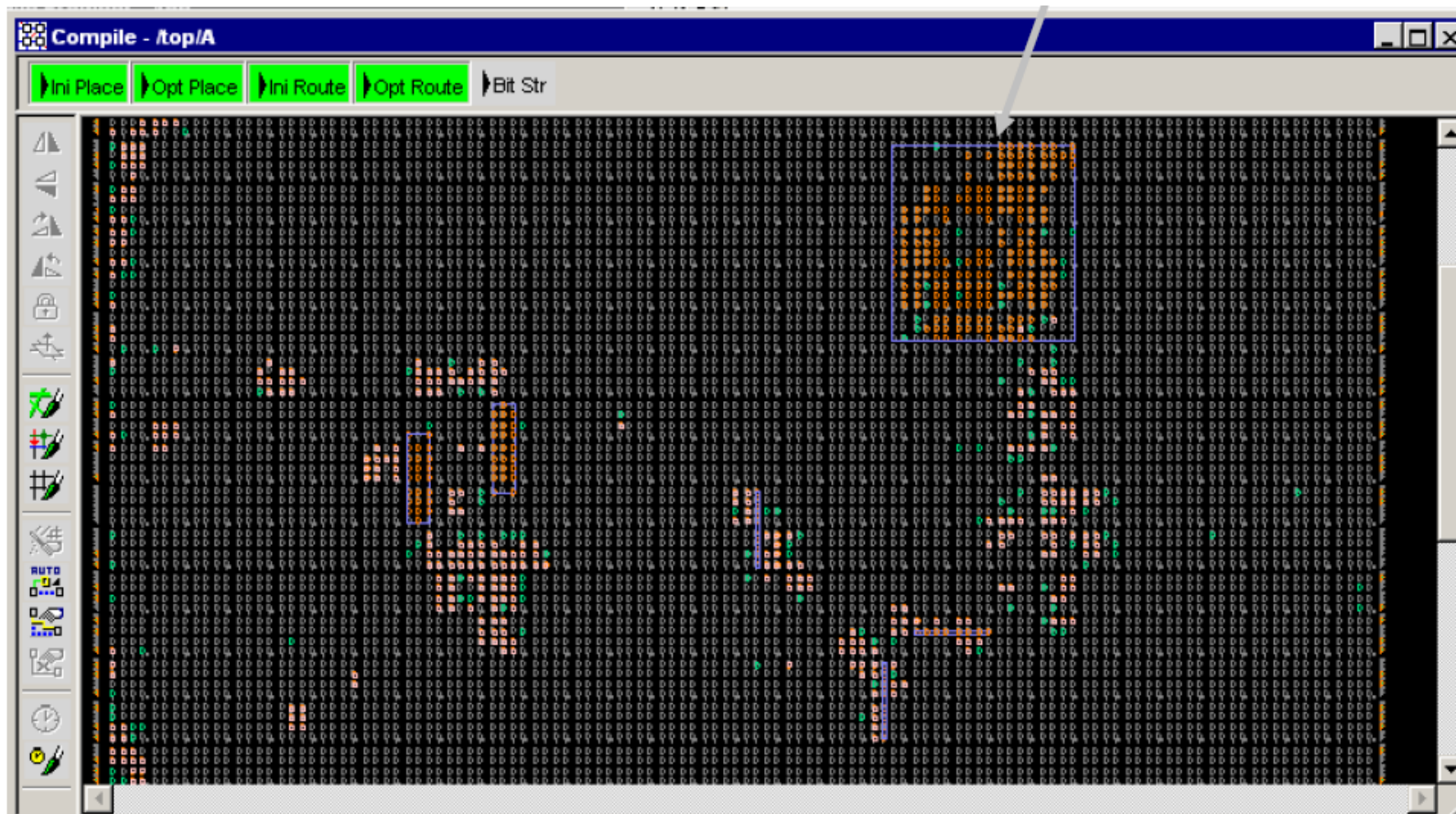


## ■ Use Hard Macro

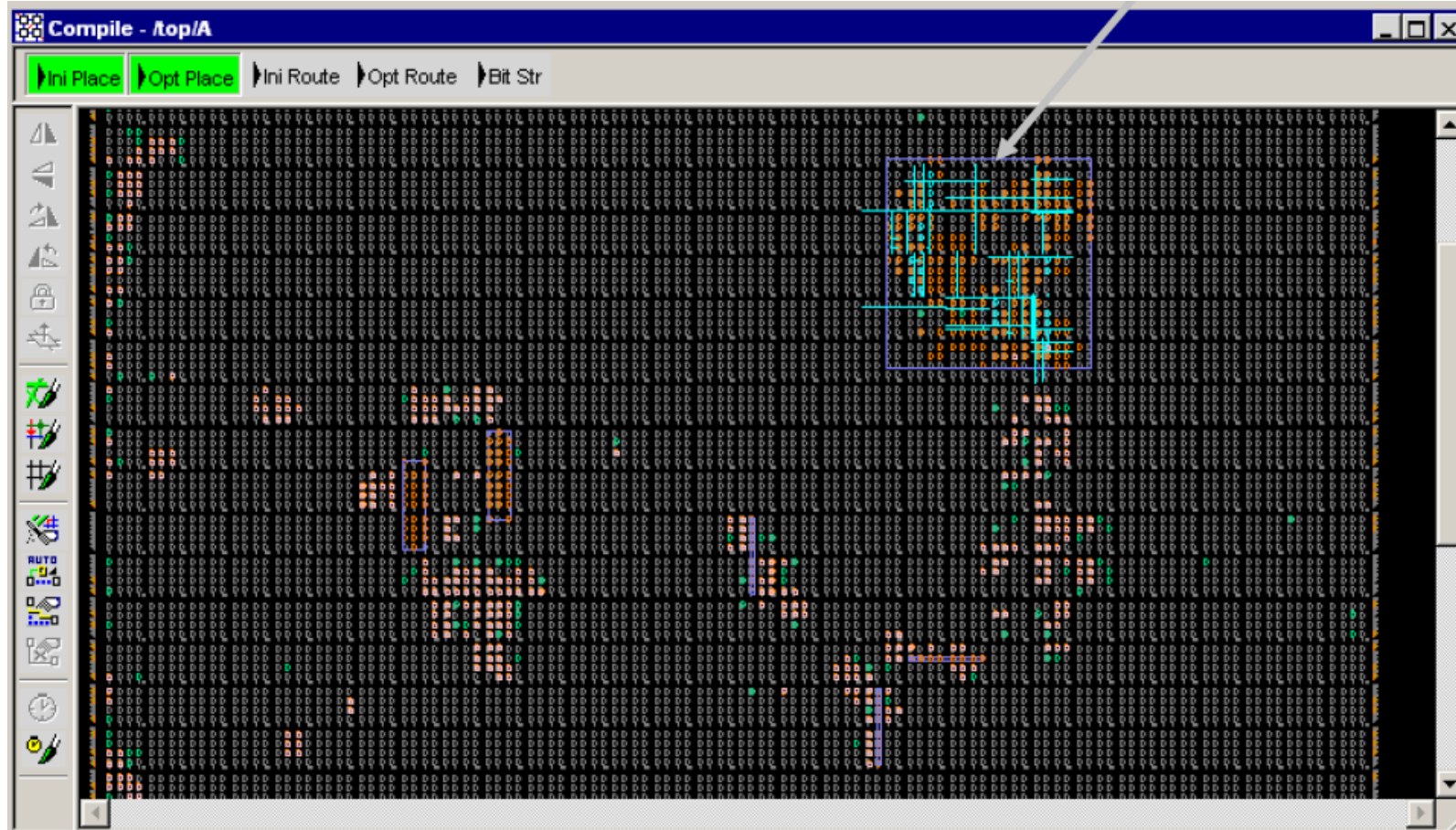
- Static and Dynamic Entities designed separately at top level
- Synthesis at top level
  - Static Entity with a Black-Box instead of Dynamic entity
  - Dynamic entities versions P&R and placed in library



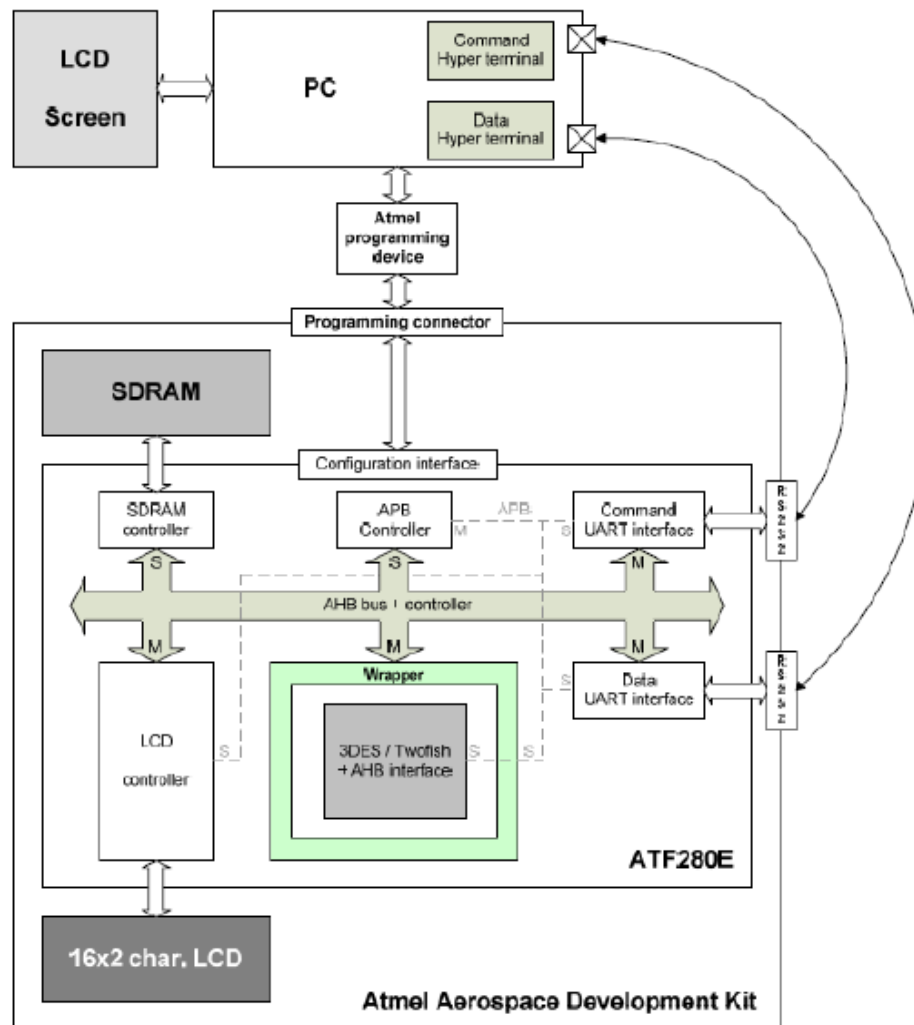
## ■ P&R complete design with First Dynamic Entity



## ■ P&R complete design with Second Dynamic Entity



## Example



**Text encrypted in two half**

- First 3DES
- Second TwoFish
- Clear Text stored in SDRAM

**3DES loaded, data deciphered and stored**  
**TwoFish loaded, data deciphered and stored**  
**3 texts displayed**



# QUESTIONS