Peregrine Semiconductor

DC-DC Converters for FPGA Applications

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Peregrine Semiconductor

DC-DC Converters for FPGA Applications in Space

- FPGAs and other advanced logic operate from very low supply voltages
- Even (chip) I/Os are trending downward
- Legacy 5V interfaces persist, legacy 5V "bricks" are lowest commonly-available regulated supply
  - SPA-U - 5V resource
  - 3.3V supplies are slowly replacing 5V, paced by new vs retrofit decisions at higher levels of assembly
- FPGAs require at least two "special" low voltage supplies for I/O and core; sometimes more.
- Voltage regulation must be done somewhere between the appropriate power source and the load (FPGA)

DC-DC Converters for FPGA Applications in Space

- Linear regulators are one option
  - Familiar
  - Simple
  - Quiet
  - Woefully inefficient
    - 5V to 2.5V: 50% best case
    - 5V to 1V @ 10A: 20% best case - 40W to dissipate from 1 IC.
    - Iin=Iout - a 5V, 500mA "USB" resource gives you 1V, 500mA.
- Switching regulators dominate high current "big logic" applications
  - Efficiencies >80% at full load, peak >90% at any stepdown ratio
  - Iout/Iin ~ Vin/Vout - a 5V, 500mA "USB" resource gives 1V, 2.5A
    - A "no-brainer" when power budget is limited
  - Complex operation but less thermal management problems
    - SWAP far superior when thermal hdwr considered

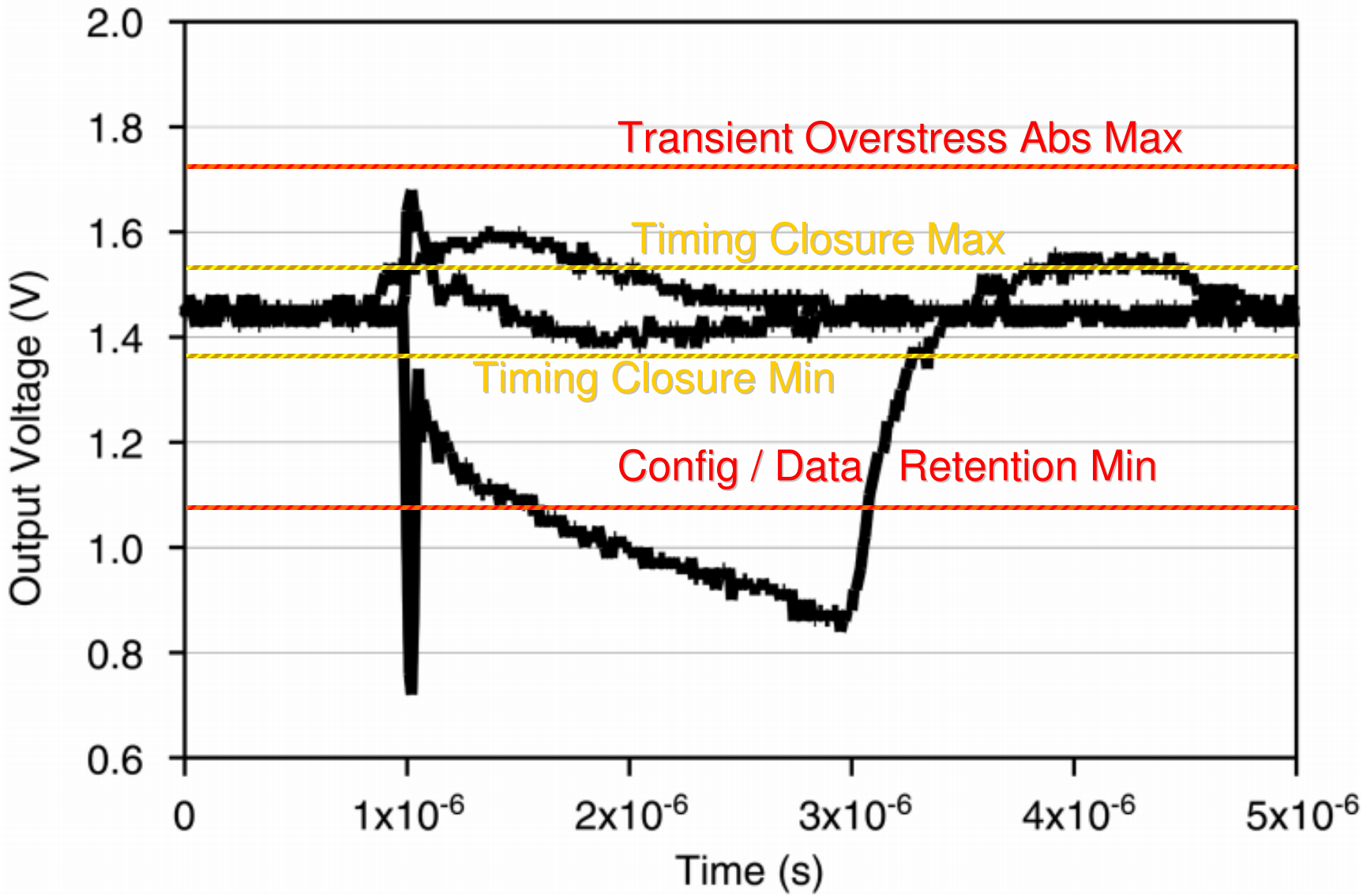
The "Power Problem"

- Resolved: operational integrity is the prime attribute
- FPGA vendors invest heavily in providing single-event-robust products and design tools
- FPGA designers spend man-months to -years developing and proving designs / applications
  - The basis of proof, and the underlying assumptions - more, shortly.
- Somebody is going to spend even more money testing and qualifying the board, the box, the payload.
- To most people, the power supply is a "given".

The "Power Problem"

- Every IC has a band of supply voltage where performance is guaranteed
  - Pin electricals (DC / timing): +/-5% is the norm
  - Data / configuration retention, SRAM FPGA: -25% (X)
  - Data retention (register, SRAM block), OTP FPGA: ??? (A)
  - Internal timing models: "Worst case" is -6.7% (A)
  - Abs Max core supply ("might cause permanent damage") : +10% (A)
  - Transient damage, no duration allowed: +20% (A)
- Design closure is predicated on operation within tight limits
- Designs exposed to out-of-limit supplies must be assumed unreliable without comprehensive overtest
  - Do you know a priori, how much margin and how much threat?
- The power supply's "single event" = your "global event"

The "Power Problem"



FPGA power requirements - general

- Low voltage, high current, noise + DC tolerance 5?%
- High speed data I/Os require low ripple supply for signal integrity (HF PSRR / timing modulation).
- Effects of large supply perturbations (beyond the ripple specs) are not known, suspect loss of data is possible.
- Little margin for overvoltage (damage).
- Little margin for undervoltage (logic / data integrity)
- Potential for large load steps
  - Requires agile control loop to maintain QOR in spec
  - Impractical at low switching frequencies
  - Impractical by filtering alone at 10A currents and 50mV tolerances

FPGA power requirements - specific

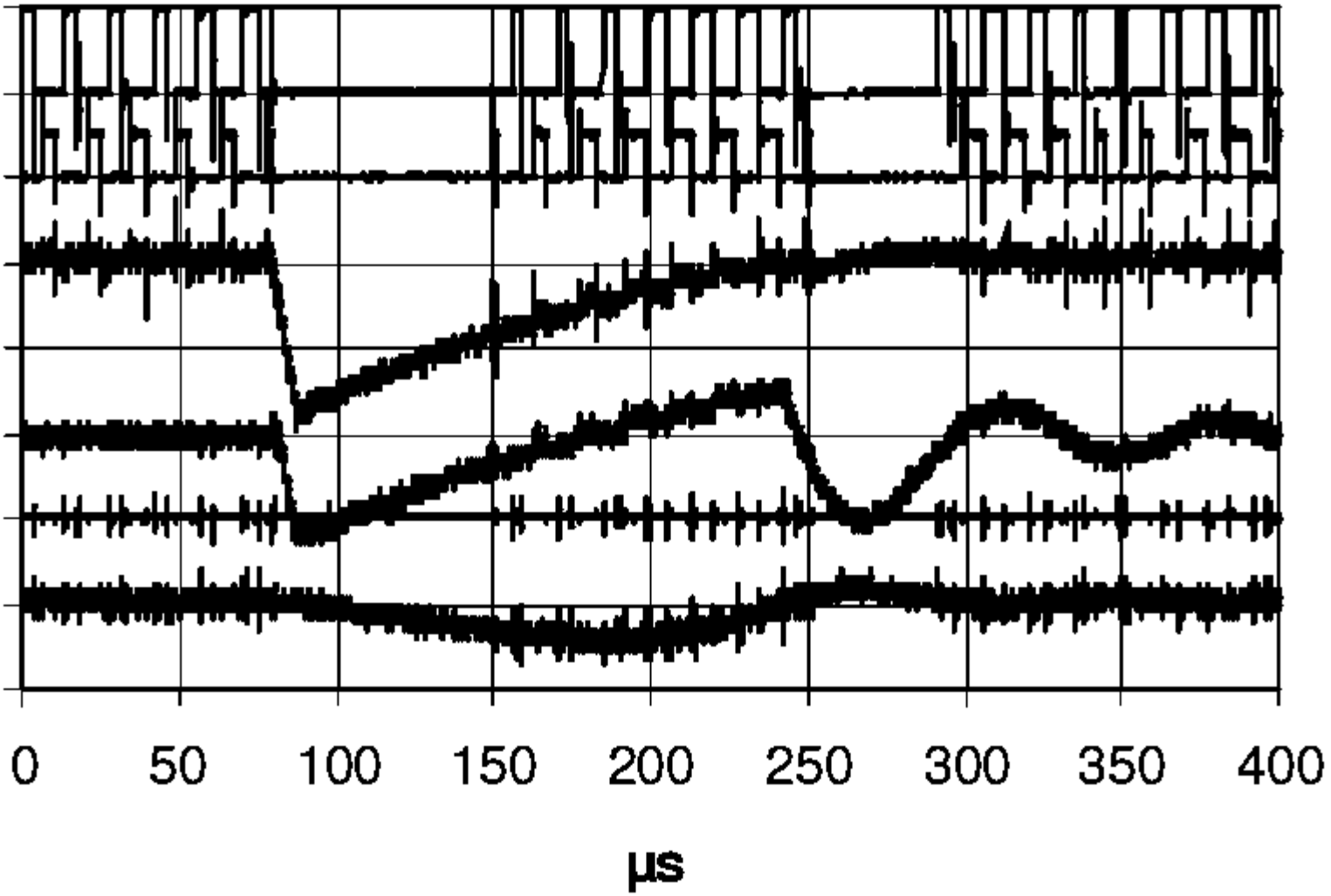
- Xilinx V5 / SIRF
  - 0.95-1.05V core @ up to 11A (config, clock, activity dependent) is design guidance we have received. Large load steps likely.
  - 2.375-2.625 AUX, low current
  - Wide range I/O supply, system variable, >1 amp range (I/O config, rate dependent). Many hundreds of I/Os possible. Load step likely.
  - Explicit power supply sequencing is required
- Actel RTAX/S
  - 1.35 - 1.65V core @ 10 amps max (config, clock, activity dependent; using power calculator WAG)?
  - 2.5-3.3V I/O, >1A at high I/O count
  - VCCA Supply current spike during VCCDA dropout event could exacerbate supply droop if not over-designed to normal ICC
  - No power sequencing requirements
  - On-chip POR, low-going threshold not specified

Space environment and power converter response

- Reference accuracy (rollup of bandgap, error amp, pin leakages) drift w/ TID is a problem against 5% supply limits.
- Single event perturbations -will- occur; "how big?" is the question.
  - "Within specified tolerance" is the right answer
- Non-hardened designs contain critical features which commonly produce extreme dropout events (soft start / shutdown)
- Non-hardened designs present a destructive overvoltage overshoot risk (control loop slew high)

Space environment and power converter response

An old-school bipolar PWM shows SEE sensitivity; typical of non-SEE-hardened DC-DCs in CMOS as well.

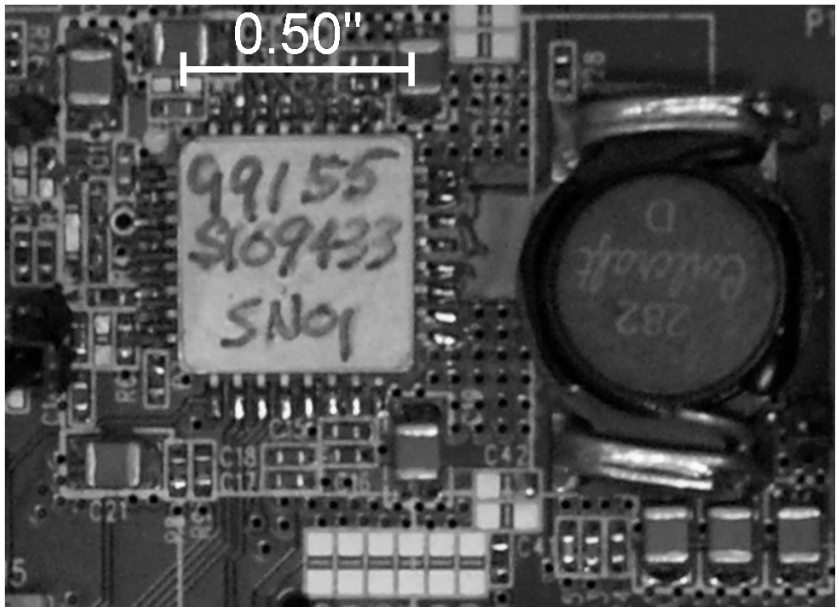


Product upscreening / designed radiation hardness

- Upscreening commercial power management parts may find adequately total dose tolerant, SEL survivable types
  - Unlikely to find any without SEFI/SEU/SET issues.
  - A 1mS "upset" in a regulator is a lifetime in a 400MBPS packet engine (bye, bye, gross BER). Even if the logic comes back right side up.
- Several space market vendors developing designed rad hard products.
  - Guaranteed, lot-tested TID hardness beyond most mission rqmts
  - Characterized SEE response (ideally, none; in any case, known and low enough to be budgetable)
  - Of course we have a favorite.

PE9915x product attributes

- 2, 5, 10A integrated buck converters (no RH FETs to buy)
- Compact solution size
- Operable up to 5MHz (if you can find unobtainium filter caps) and two free-running freq selects
- The usual shutdown, soft start features without the usual SEE sensitivities
- High degree of configurability (VOUT, current limit, SS ramp, frequency)
- PGOOD output for supply sequencing and telemetry

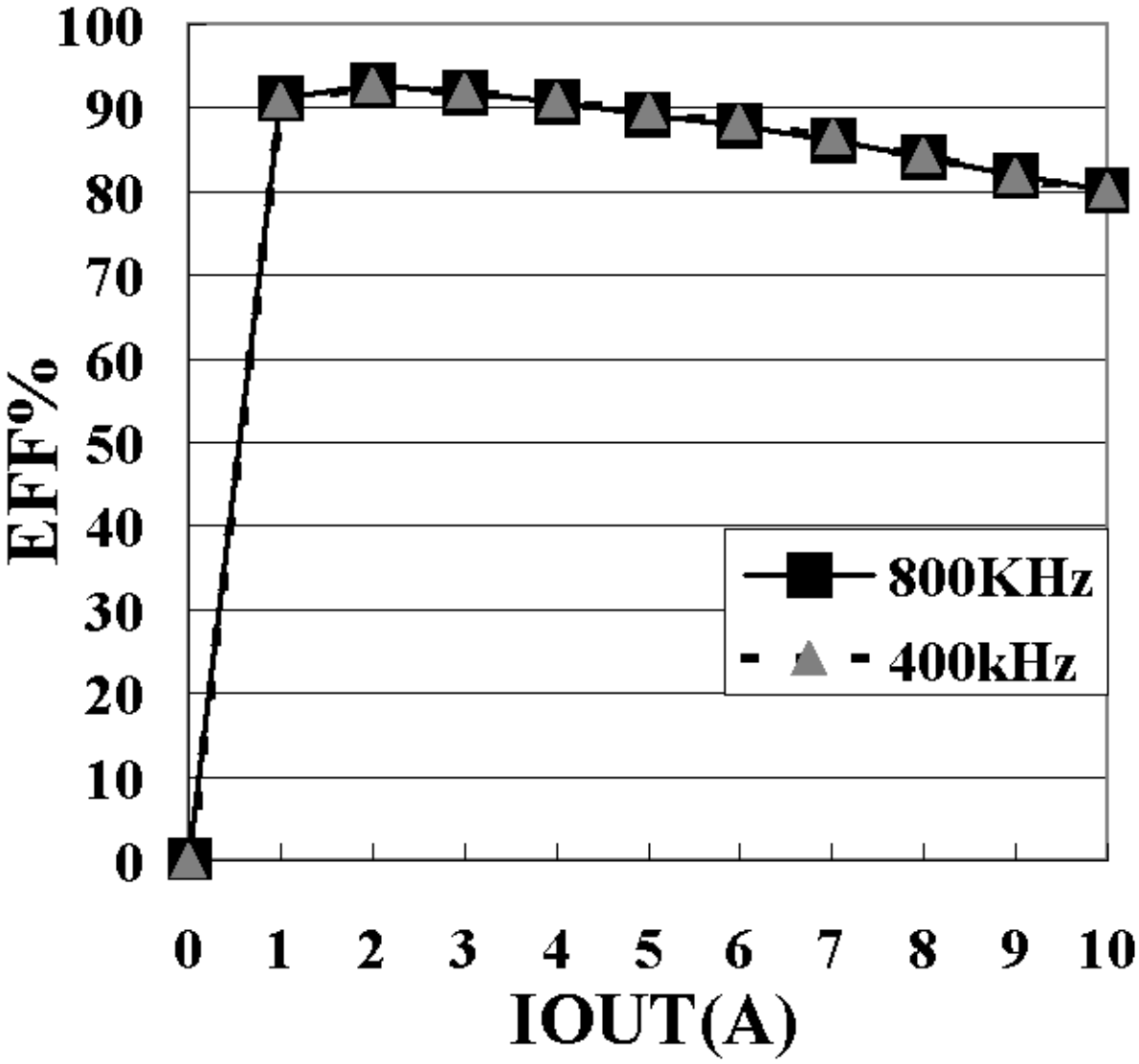


10A Buck Eval Board

All components exc connectors

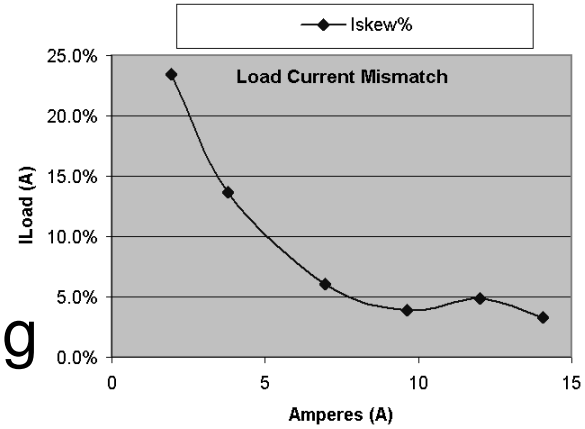
PE9915x product attributes

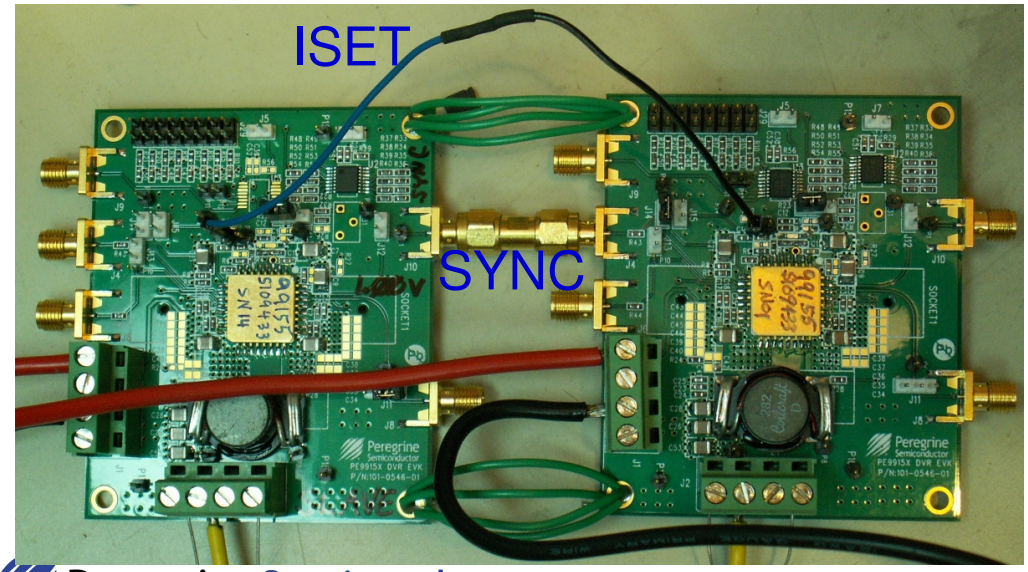
- Low (1-2mA) standby current - 0.2% on a 10A converter. Hot spareable for N+K
- 94% real board peak "wallplug" efficiency - no "de-embedding" - $(I_{OUT}*V_{OUT})/(I_{IN}*V_{IN})$ - 89% half , 80% full load
- Pulse-by-pulse user programmable current limit, failsafe overcurrent limit

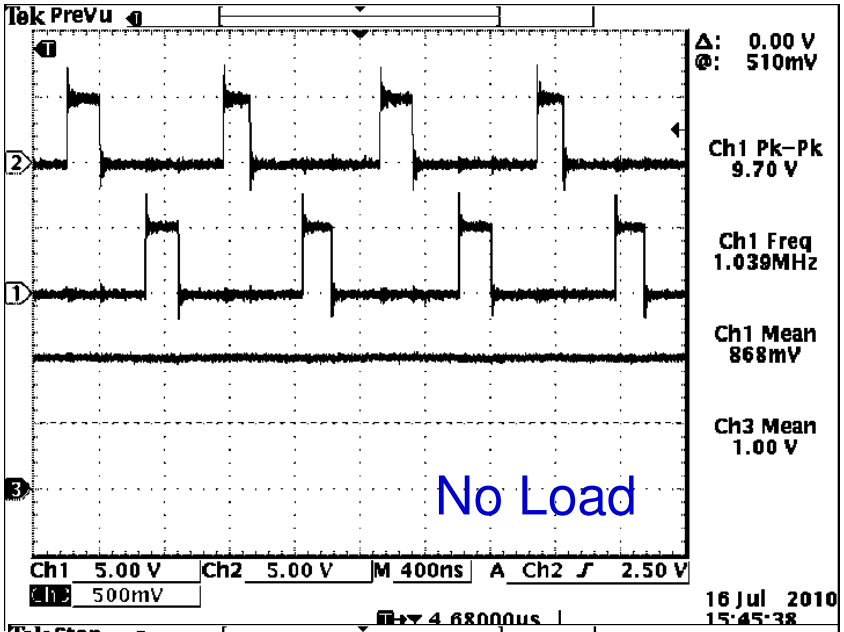


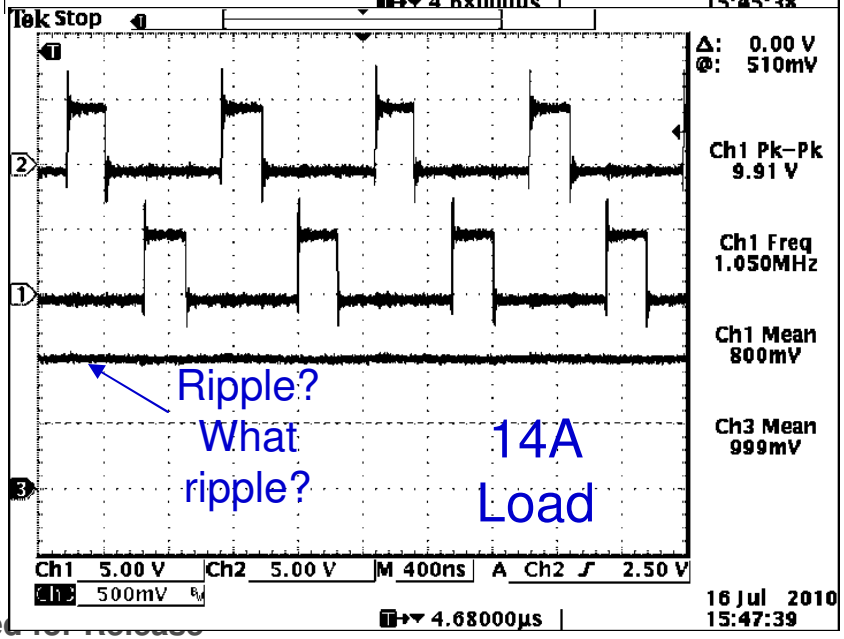
PE9915x product attributes

- Synchronizable for EMI control
- Simple 2-wire implementation of 2-phase buck (halving ripple) with balanced current sharing



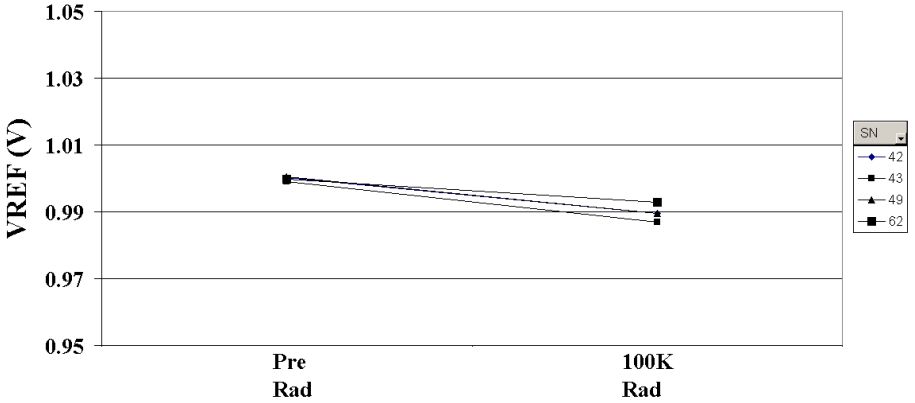


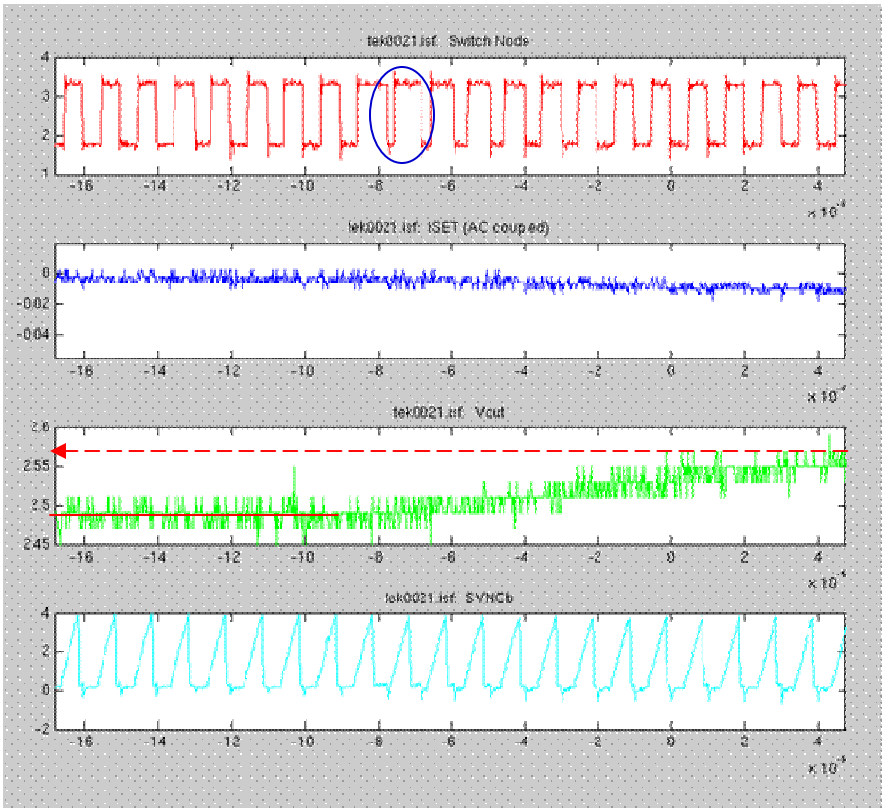




PE9915x product attributes

- Sub-1% Reference / output drift at 100KRad





- SEL, SEFI, SEGR, SEU immune.
- SET (Spin2) ΔVOUT close to 2% design goal at 100uF Cfilter. Competitor requires 800uF of space-grade caps. Design tightened on Spin3.

Conclusion

- Newer logic and FPGA generations are increasingly demanding of power supply quality and performance
- Power supply "SEU" can cause global errors or damage when it exceeds FPGA tolerances
- Most "space grade" power conversion ICs have poor SEU/SET performance.
- Older options
  - are unsuitable for lower voltage input supplies and output voltages,
  - are limited in step-down ratio from higher supplies,
  - cannot run efficiently at high frequency / small inductor
  - require external rad hard power FETs ($$$$)
- New high efficiency, fully rad hard integrated circuit POL DC-DCs provide the quality-of-regulation necessary for true FPGA reliability on orbit, in a very small PCB footprint.