Highly Scalable / Highly Configurable FPGA Based Solid State Recorder for Multi-Mission Space Applications

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Abstract

- Many missions require bulk storage
  - Solid State Recorder (SSR) with gigabits (Gb) to terabits (Tb) of memory.
- Feeding the SSR is commonly tasked to a mission unique interface module
  - Aggregate high bandwidth science data from multiple instruments
  - Data pre-formatting before storage to SSR?
- Playback from the SSR
  - May require additional formatting
  - Ultimately interfacing to the comm system
    - Another mission unique function

Abstract

- Consolidation of mission unique and SSR functionality
  - Minimizes integration issues along with cost, mass and power
- Goal: provide performance (in terms of bandwidth, density, and playback rates) AND also provide tailorable capability with minimal NRE and support *multi-mission usage*
  - Amortize board NRE across many missions
- The Multi-Mission Mass Memory (M4) is an FPGA based module that provides a flexible mission payload interface with integrated solid state recorder capability, high speed playback and formatting over a flexible downlink interface

Motivations

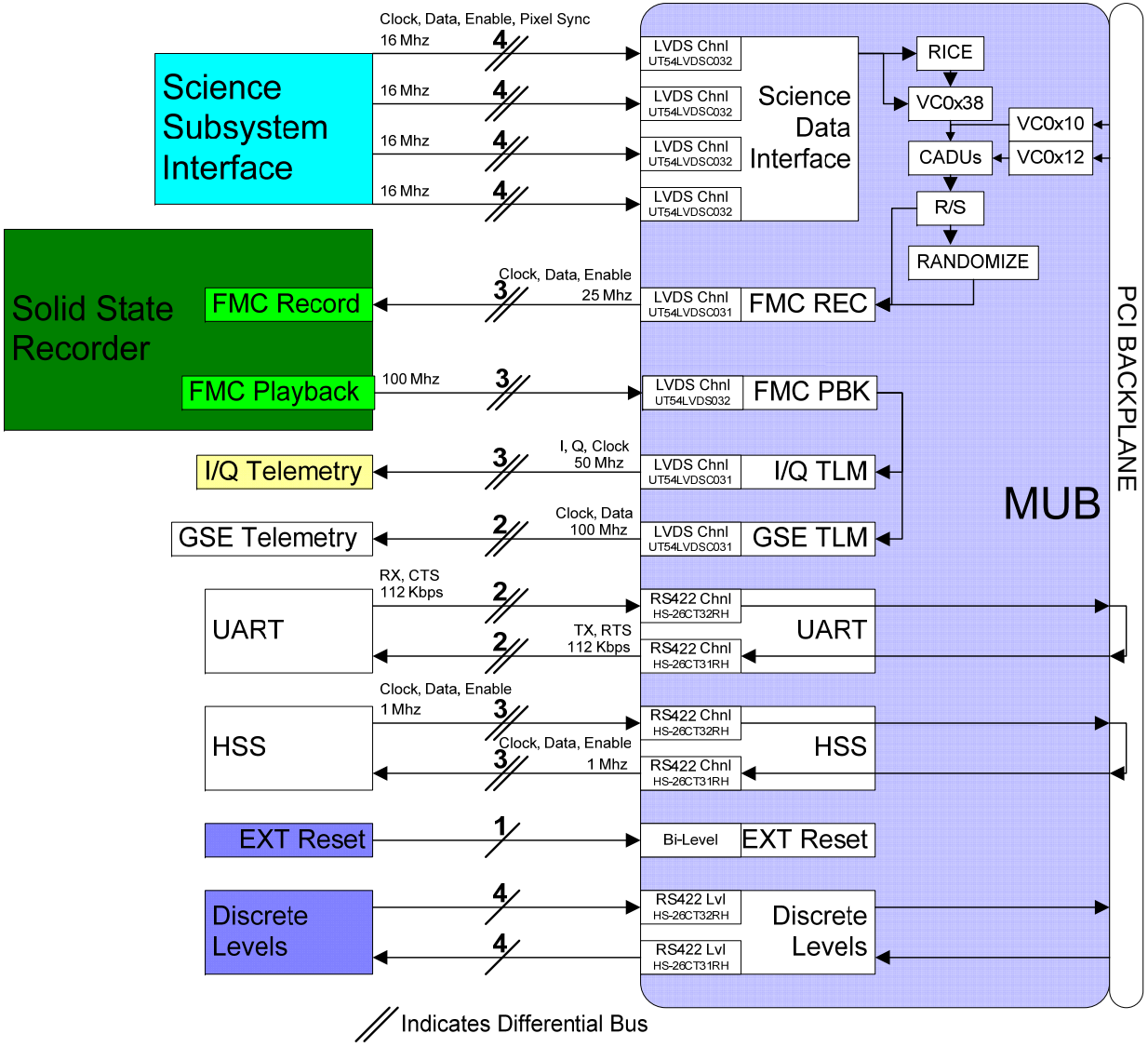
- Rising costs and increased mission requirements
  - *High data rates*
  - *Onboard storage*
  - *Mission unique interfaces*
- Basic system topology
  - Standard bus, standard product BUT with mission unique interfaces

IT'S ALL ABOUT THE PAYLOAD

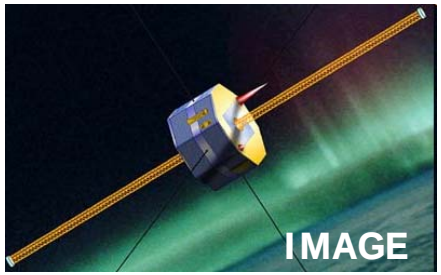
Background – WISE

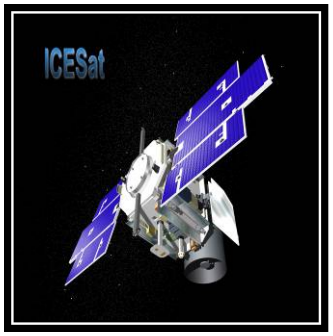
- WISE mission architecture
  - Mission Unique Data Processing
  - High Capacity SSR
  - CCSDS Formatting
  - Comm/System Playback Interface

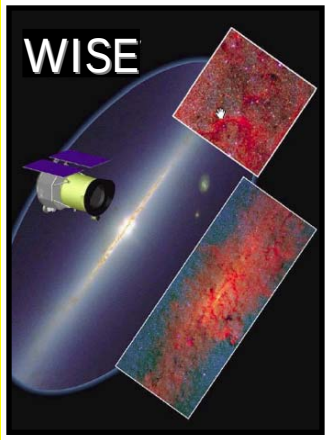
WISE Science Dataflow

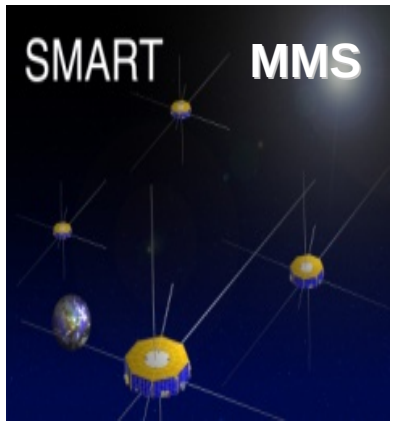


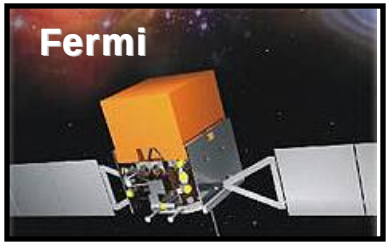
SwRI Heritage Avionics Combining Mission Capabilities

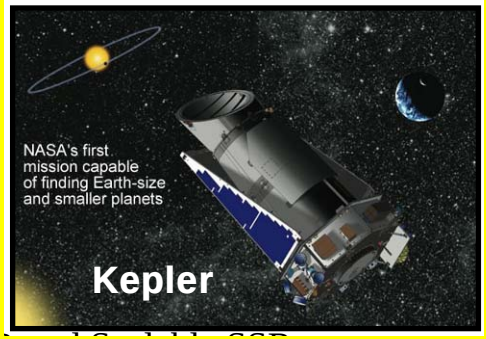


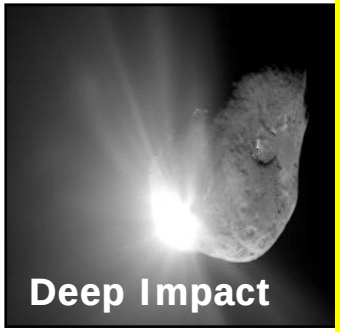










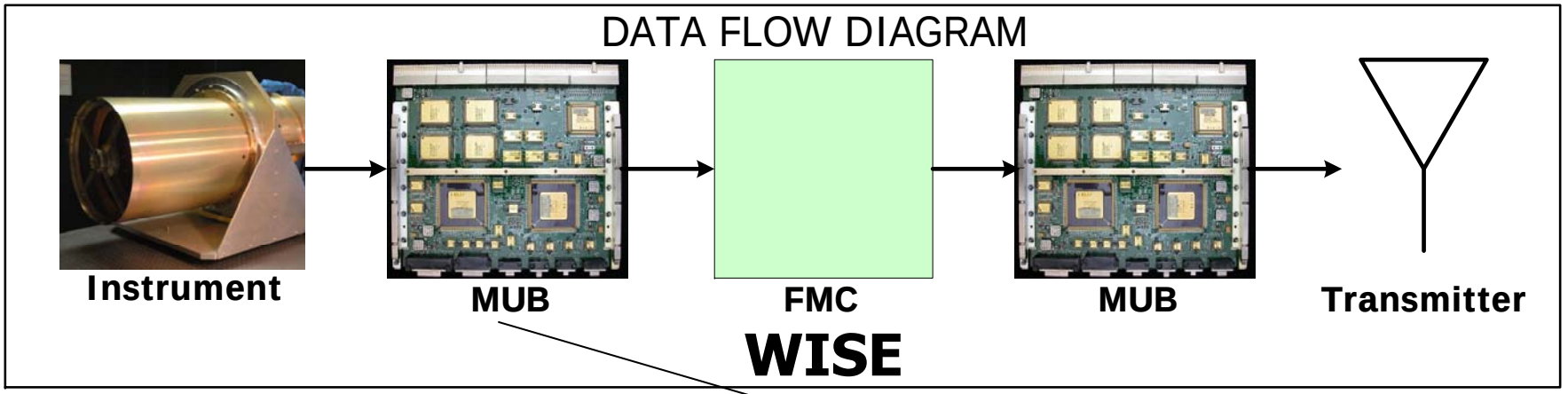


Multi-Mission Mass Memory (M4)

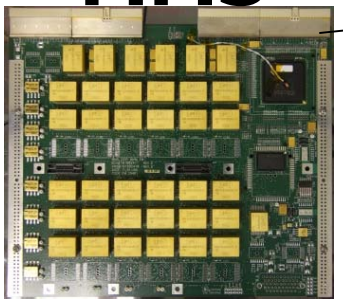
- FPGA Based Solid State Recorder
  - Low to high density, depending on mission need
- Highly Scalable
  - Meet I/O needs (number and protocol)
  - Meet bandwidth needs
- Highly Configurable
  - Satisfy requirements for partitioning
    - NVM applications (file system)
    - Serial Recorder (linear storage)
    - Both
  - Provide mission unique data ingest capability
    - Support for a variety of protocols
    - Provide data manipulation
  - Support Data Formatting needs
- Multi-Mission Space Applications
  - Eliminate Board NRE
  - Minimize cost, mass, power

M4 Evolution – WISE and MMS

- SwRI IR&D at work



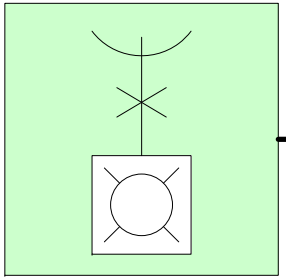
MMS



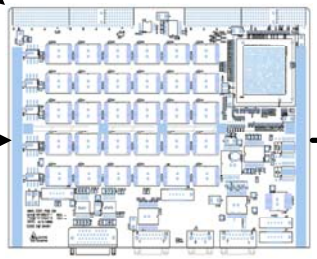
Mass Memory Module

Combine functionality of MUB and MMM into a single board: M4

+



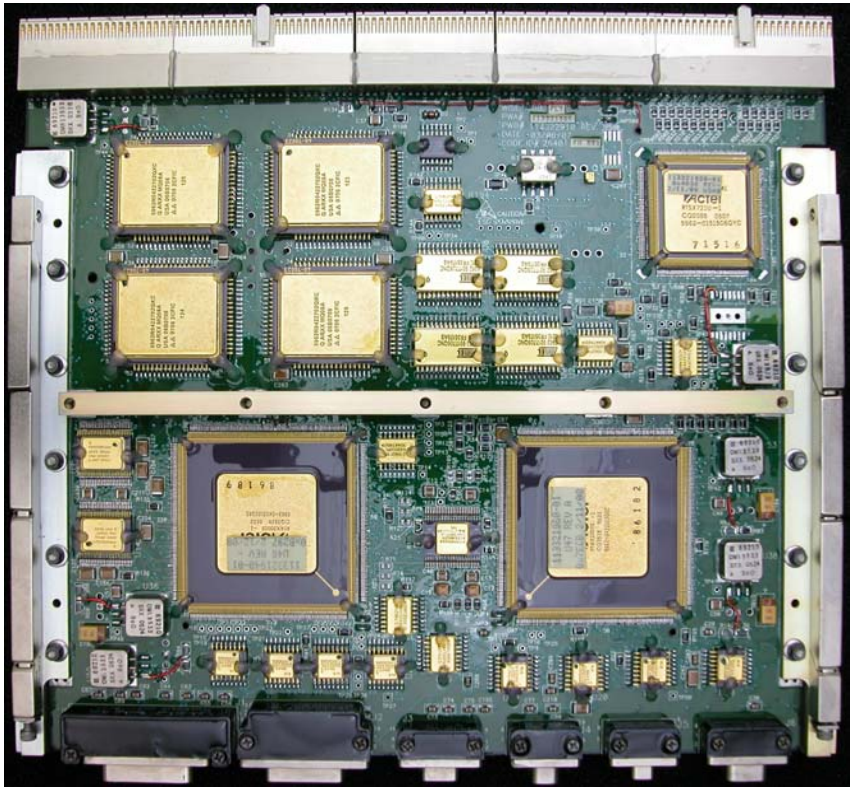
Instrument



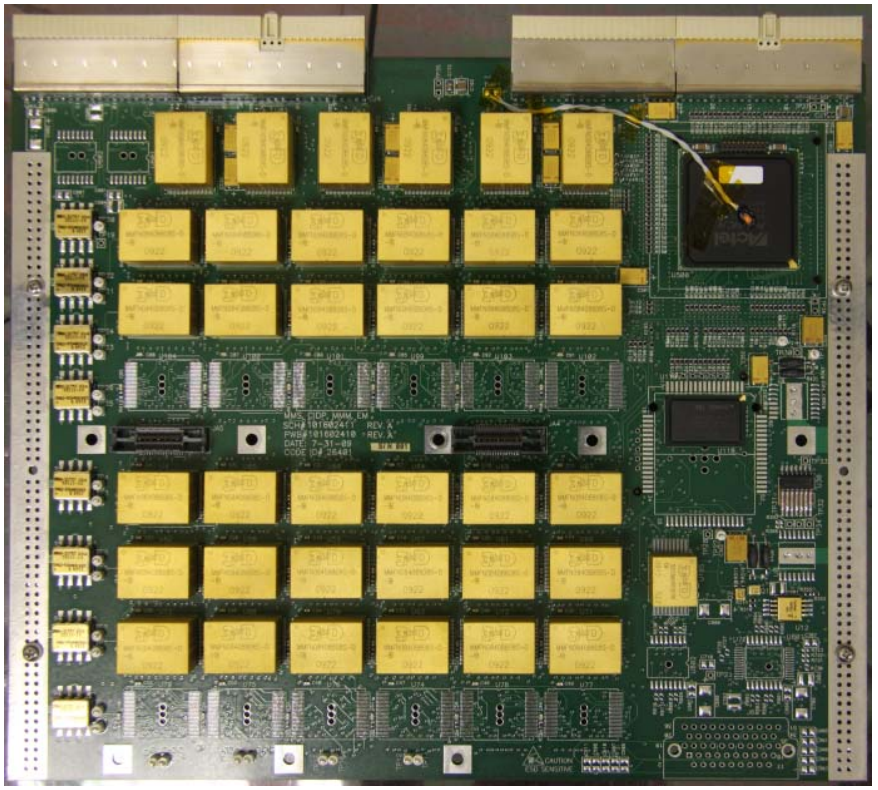
ISM

Transmitter

WISE MUB + MMS MMM



128 GB SSR

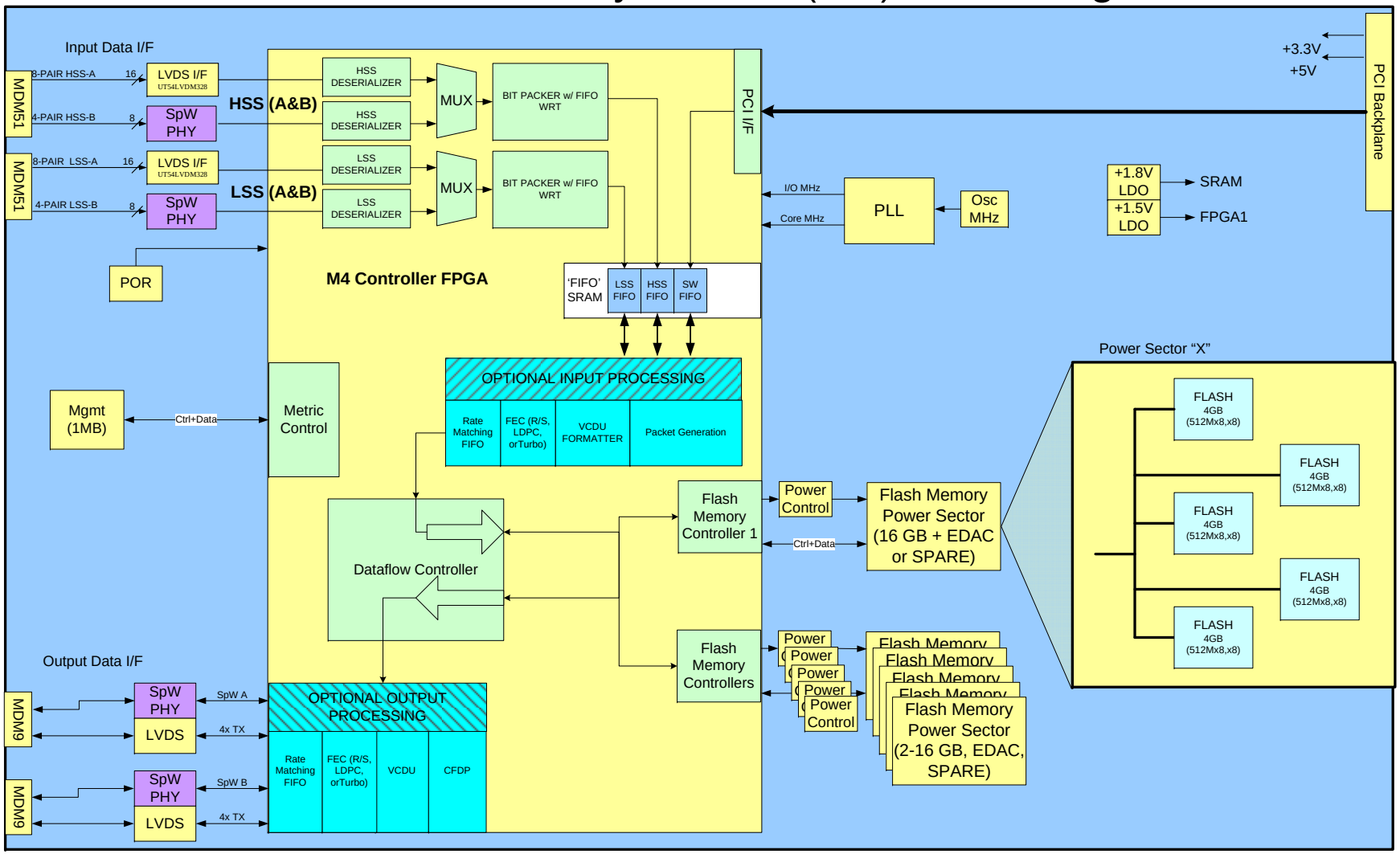


Science Data Interface and Telemetry Formatter

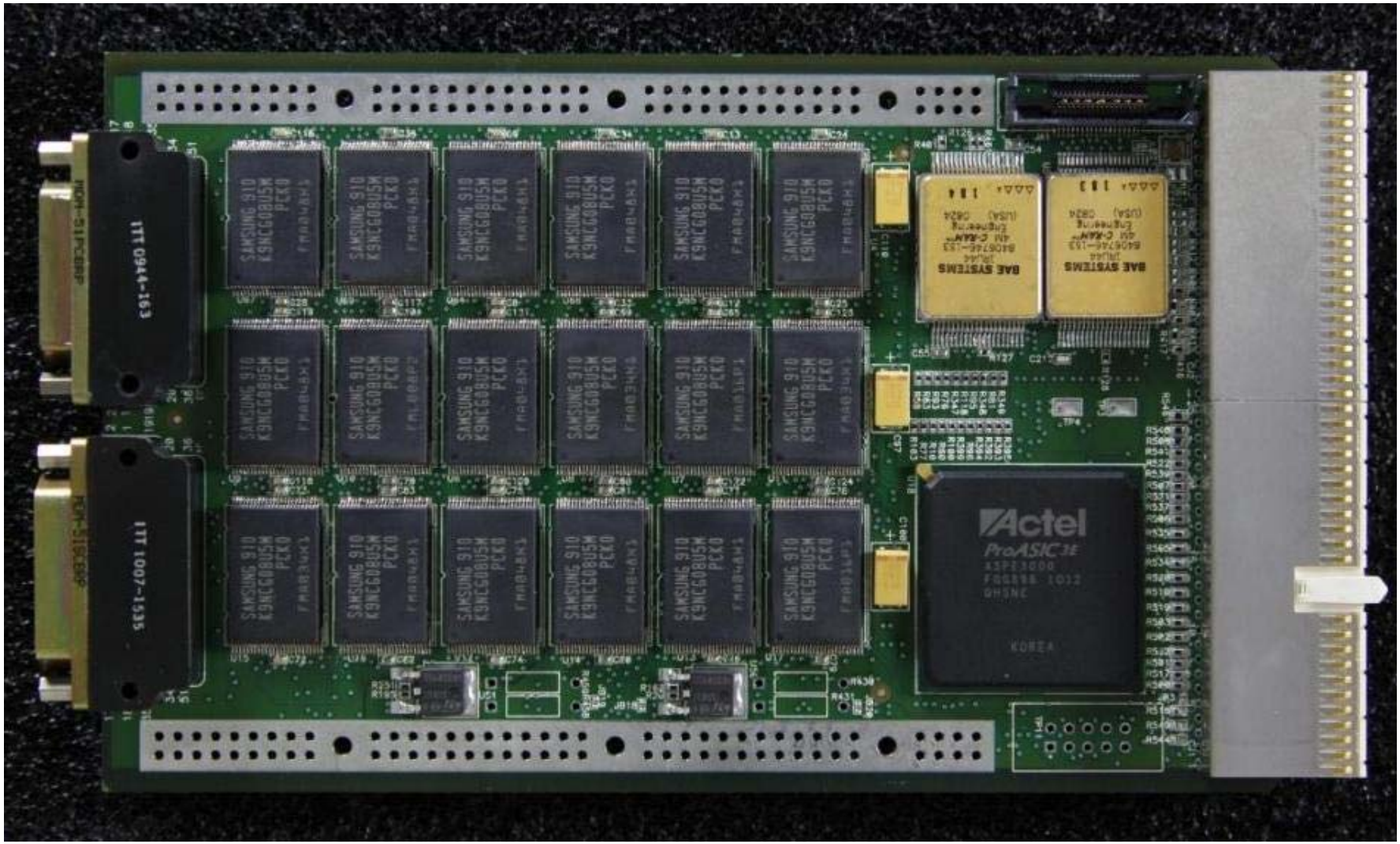
M4 Architecture

Multi-Mission Memory Module (M4) Block Diagram

Revised 05/30/2010



3U M4 Board



Inherent Benefits

- Multi-Mission Capable Platform
  - Common platform
  - Customization available & expected
    - Configuration at assembly
    - FPGA enhancements
      - Low cost prototyping platform
  - Board NRE is highly amortized

M4 FUNCTIONS

- Mission unique data processing
  - High Bandwidth Capability
  - Direct Payload interface
  - Customizable input processing
- Flexible storage architecture
  - General purpose file system & linear storage
  - Multiple “slices” (drives) and partitions
- Direct Comm System interface
  - Customizable output formatting

FPGA ARCHITECTURE

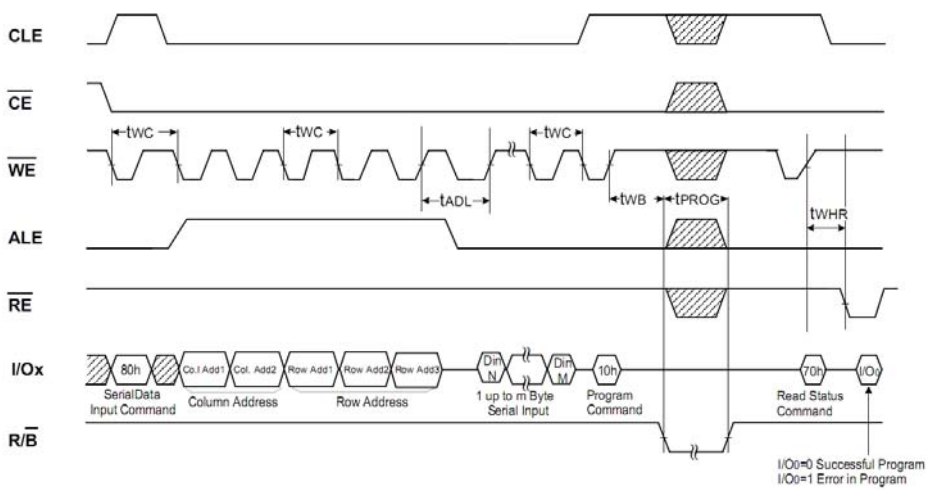
- Modular architectural approach to FPGA
  - Ingest, Storage/Management, Playback
  - Dataflow and Metric Arbiter are key items
- Flexible I/O
  - Queuing : many to 1, 1 to 1, etc…
  - Protocols
- Flexible storage architecture
  - Variable width or interleave
  - Configurable “drives” within memory space
    - Expectation of modulo 32-bit architecture
- Parameterize core functions and interfaces for generic applications

Storage Elements

- NEPP/SWRI testing of FLASH
- SEE response is generally excellent for all flash products
  - 1.13e-21 double bit error/byte-day
- None of the parts suffered SEL
- The SEFI rate is a concern with flash memories.
  - “The SEFI (Single Event Functional Interrupt) rate is of greater concern for space applications than the bit error rate”
    - TID and SEE Response of Advanced 4G NAND Flash Memories
      - NSREC08, T.R. Oldham
- Mitigation strategies outlined MAPLD09

THEORETICAL FLASH BW

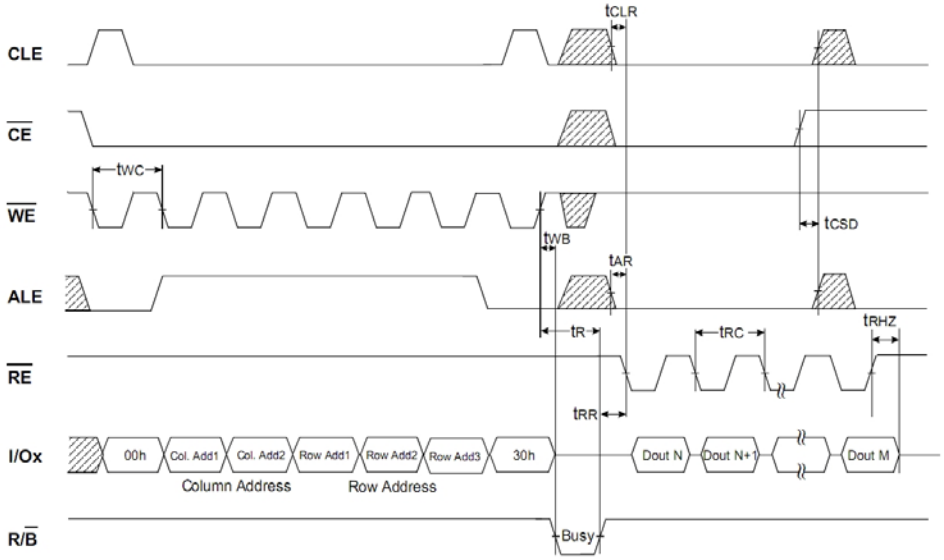
WRITE



Cycle	Duration	Units
CLC	25	ns
ALC	127	ns
CLC	25	ns
IDLC	46499	ns
tPROG	600000	ns
TOTAL	**646676**	**ns**

Value	Units	Bus Width
26.1	Mbps	x8
104.5	Mbps	x32
3.26	MBps	x8
13.06	MBps	x32

READ



Cycle	Duration	Units
CLC	25	ns
ALC	127	ns
CLC	25	ns
Tr	25000	ns
DOb	20	ns
DO	52800	ns
TOTAL	**77997**	**ns**

Value	Units	Bus Width
216.66	Mbps	x8
866.67	Mbps	x32
27.08	MBps	x8
108.3	MBps	x32

Maximum interface rates (Derate factors for MCM access → 78Mb/s & 514Mb/s)

ACTUAL MEMORY BANDWIDTH

- Modest interface clock rate of 40MHz
- Data Arbiter modification only
  - 32bit WRITE bandwidth per “slice”
    - 126Mb/s with current state machine
    - Eliminating half the wait states → 280Mb/s
  - 32bit READ bandwidth per sector “slice”
    - 160Mb/s current state machine
    - 320Mb/s by reducing wait states
- 3-6 slices per assembly
  - Usable bandwidth > 700Mb/s

CURRENT EFFORTS

- VALIDATE USABLE I/O BANDWIDTH
  - Ingest test setup is 2bit data @ 60MHz X #slices
    - Mimic SpaceWire up to 200Mb/s
  - Update flash I/F & increase data rate
- Maximum BW will be over proprietary interface
  - SERDES capability --> 1Gb/s
  - Custom parallel LVDS implementation
- CORRELATE MEASURED POWER VS BW
  - Validate power vs bandwidth calculations

PERFORMANCE ENHANCEMENTS

- Increase clock rate to flash memory I/F
  - Data Pipelining
  - Interleaving
  - Pipeline for ECC
- Improve playback interface data rate
  - Multi-bit (parallel) interface
  - SERDES
- Enhance PCI DMA performance
- IP integration
  - CCSDS formatting

M4 APPLICATIONS

- Science data processing, storage and comm interface board
  - 3U and 6U modules
- General Purpose NVM board
  - HW protected bootloader / OS partition
- CCSDS formatting in HW including CFDP engine for either Class 1 or 2

Multi-Mission Benefits

- Standard M4 platform can be used across multiple missions
  - Reduce SW development costs
- Amortized Mission Costs
  - PSDA / WCCA, etc…
  - Signal Integrity Analysis
- Mission related NRE is relegated to FPGA: documentation, and some analysis tasks
  - WCTA is straightforward – updated each revision
  - Thermal will be re-calculated versus bandwidth requirements

Multi-Mission Mass Memory

- The M4 is a feature rich FPGA based platform that provides a flexible mission payload interface with integrated solid state recorder capabilities and high speed downlink interfaces.
  - 6 to 96GBytes of non-volatile ECC protected memory
  - 3-6 storage partitions (individual or concatenated)
  - 200Mbps cPCI interface (DMA capable)
  - Support for 120Mbps serial input interfaces
  - Playback over multiple interfaces at 300Mbps
  - Hardware file management
  - CFDP capability in HW

SUMMARY

- The M4 includes the capabilities required for a variety of missions due to the flexibility of the FPGA based architecture
- Architected around configurable storage space
- Support for multiple physical interfaces and a variety of protocols

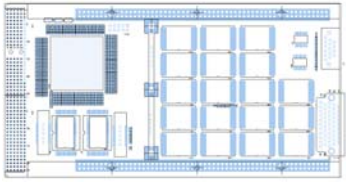
Highly Scalable / Highly Configurable FPGA Based Solid State Recorder for Multi-Mission Space Applications

Sources

- TID and SEE Response of an Advanced Samsung 4Gb NAND Flash Memory (NSREC07); T. R. Oldham, M. Friendlich, J. W. Howard, Jr., M. D. Berg, H. S. Kim, T. L. Irwin, and K. A. LaBel
- TID and SEE Response of Advanced 4G NAND Flash Memories (NSREC08); T. R. Oldham, Fellow, IEEE, M. Suhail, M. R. Friendlich, M. A. Carts, R.L. Ladbury, Member, IEEE, H. S. Kim, M. D. Berg, C. Poivey, Member, IEEE, S. P. Buchner, Member, IEEE, A. B. Sanders, C. M. Seidleck, and K. A. LaBel, Member, IEEE
- SEE and TID of Emerging Non-Volatile Memories; D.N. Nguyen and L.Z. Scheick, Jet Propulsion Laboratory California Institute of Technology, http://parts.jpl.nasa.gov/docs/PID16621.pdf
- A Case Study of Single Event Functional Interrupts (SEFIs) in COTS SDRAMS (NSREC08); Joe Benedetto and George Ott, Radiation Assured Devices
- A High-Density, Non-Volatile Mass-Memory and Data Formatting Solution for Space Applications (IEEE Aerospace 2010); John Dickinson, Charlie Howard, Steven Torno

BACKUP

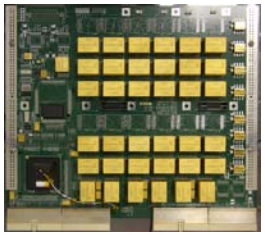
M4 Roadmap



SwRI IR&D
3U M4 Module
Prototype (6-80GBytes)

3U M4 Prototype Features

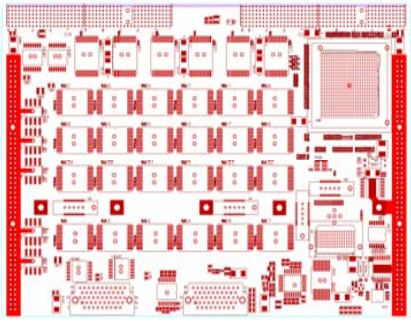
- Scalable memory size (6GB – 48GB)
- Board Layout accommodating front and backplane LVDS I/O
- Reprogrammable FPGA
  - Provides in the field re-programmability to allow the board to grow with the avionics architecture
- Up to 300 Mbps throughput (cPCI or Serial)
- Up to 8 Serial Inputs / 8 Serial Outputs
- Up to 3 drives, 8 Memory Partitions
- Lead time: 12 weeks ARO



MMS (2010)
6U Mass Memory Module
(1Tb)

6U MMS Mass Memory Module

- Scalable memory size (16GB – 128GB)
- Board Layout accommodating front and backplane LVDS I/O
- Reprogrammable FPGA via Aldec Adapter
  - Provides in the field re-programmability to allow the board to grow with the avionics architecture
- Up to 200 Mbps cPCI bus throughput
- Lead time: 6 weeks ARO



SwRI IR&D
6U M4 Module
Prototype (6-128GBytes)

6U M4 Prototype Features

- Scalable memory size (12GB – 96GB)
- Board Layout accommodating front and backplane LVDS I/O
- Reprogrammable FPGA
  - Provides in the field re-programmability to allow the board to grow with the avionics architecture
- Up to 600 Mbps throughput (cPCI or Serial)
- Up to 16 Serial Inputs / 16 Serial Outputs
- Up to 6 drives, 8 Memory Partitions
- Lead time: 18 weeks ARO

Observations

- ECC covers SEU errors
- Warm Spare compensates for SEFIs and block errors
- ECC with Warm Spare is a superior option
  - Susceptibility to permanent SEFIs plummets
  - Memory availability remains near 100%
    - Block based errors mapped to spare
    - SEFI based errors map to spare
- ECC with Warm Spare is roughly equivalent to full TMR at half the power, mass, area, and cost