Micro-RDC

Microelectronics Research Development Corporation

90nm Design-Hardened Structured ASIC

"The Next Generation of Digital ICs for Space"

ReSpace/MAPLD Conference 2010

Microelectronics Research Development Corporation

4775 Centennial Blvd., Suite 130
Colorado Springs, CO 80919
719-531-0805

8102 Menaul Blvd., Suite B
Albuquerque, NM 87110
(505) 294-1962

Stephen Philpy
Director of Programs

ViASIC

AEROFLEX

90nm Design-Hardened Structured ASIC

AFRL SBIR PROGRAM: FA9453-06-C-0200

With Special Thanks to our Program Sponsors: MDA/SMC/AFRL

Program Directors: Davis of SMC

Creigh Gordon of AFRL

PROGRAM GOALS:

- Enable Easy Design and Quick Production of
- Advanced (Deep Submicron) -> High Performance,
- Low Cost, Application Specific Digital ICs,
- For Use in Low Volume Space Applications

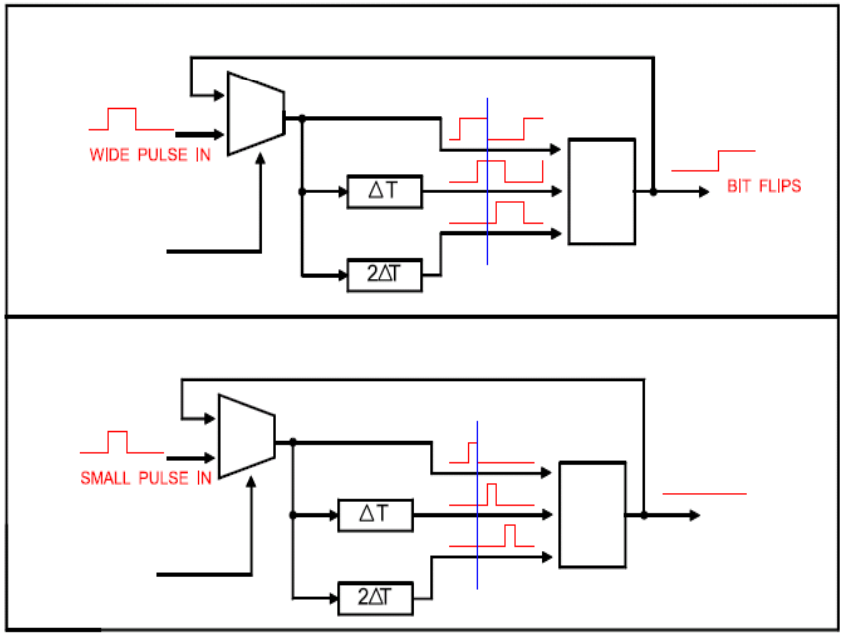
Benefits of Micro-RDC's DH SASIC Family

- **Advanced Technology Processes**
  (Within One generation of State of the Art) 90nm = IBM 9LP process -> Future = 45nmSOI
- **Processing is done in Trusted On-Shore Fab**
  (Easy Access to Quick Turn fabrication) 3 – 4 Mo. - > w/wafer banking = 2 mo. future
- **Low Cost ICs from Low Volume Fabrication**
  - Standard Low Cost Commercial Process — Frequent Lots Assure Fabrication Reliability
  - Only One Layer Mask Cost — Cost Sharing because of MPW
  - Multi-Project Wafer (MPW) Fabrication — Cost Sharing because of MPW
  - Only a few Wafers are Fabricated — Lower Fabrication Cost
  - Flight Qualification Chip on MPW Reticle — Qualification Cost Sharing because of MPW
- **Low Design Costs / Quick Design Implementation**
  (PC-based design tools, Auto Place and Route) Like FPGA design w/Custom ASIC Attributes
- **Low Power w/Built-in (Cell Library) Hardness** Hardness Testing is not Needed

Features of Micro-RDC's Design-Hardened SASIC

- **90nm IBM 9LP CMOS Fabric (Logic Cell w/Embedded Dual-Port SRAM / Tile)**
  - Distributed SRAM under the routing enables near 100% gate utilization
- **Radiation-Hardened Logic Cells based on Patented Adjustable Temporal Latch w/Delay Control to Provide SEU/SET Mitigation**
  - Temporal sampling to achieve both spatial and time redundancy
  - Variable sampling delay for hardness / performance tradeoff
  - Immune to multiple node strikes and transients on any node
  - Self scrubbing, does not integrate errors as normal TMR

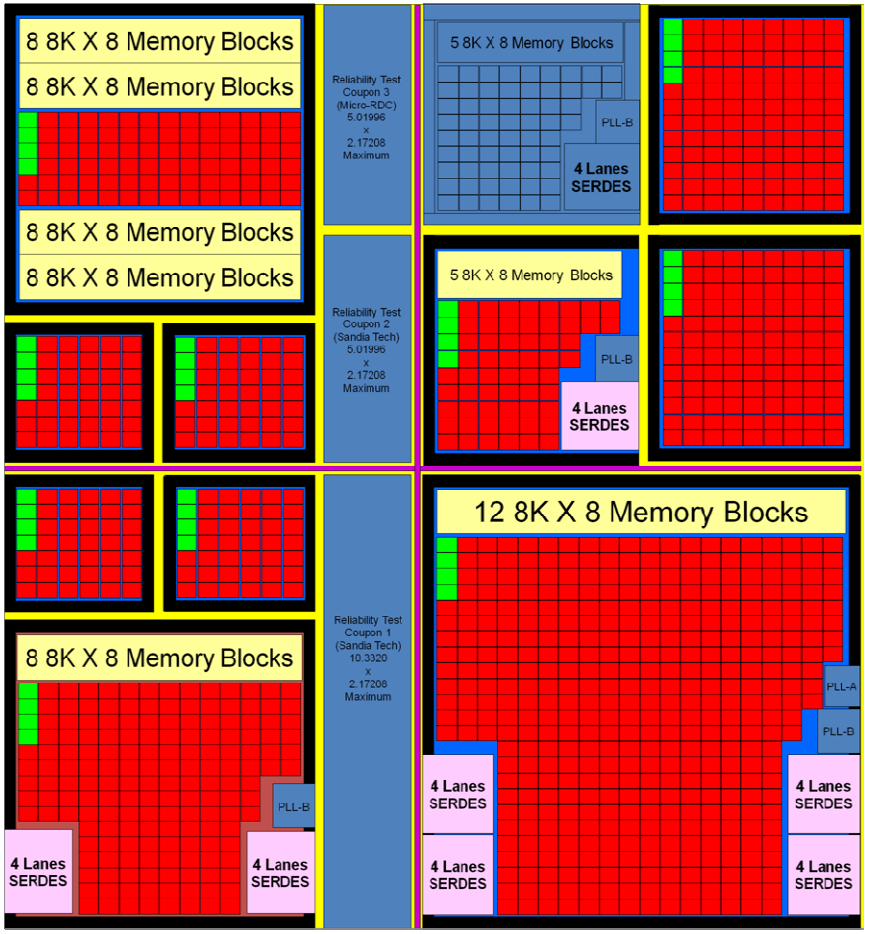
Patent No. 6,127,864



Features of Micro-RDC's Design-Hardened SASIC

- **Radiation-Hardened Configurable 8K X 8 SRAM Memory Blocks with SEU Mitigation**
  - Conventional 4T storage with dual-port PMOS access
  - EDAC for single bit errors
  - Scrubbing to reduce multiple bit errors
- **Radiation-Hardened Via Programmable ROM and General Purpose IO**
- **Radiation- Hardened PLL Macros**
- **Radiation-Hardened 1.25 Gbps 10B SERDES or LVDS Channels**

Micro-RDC's Design-Hardened SASIC MPW Reticle



21 mm

20 mm

10 USER CONFIGURABLE DIE SITES PER MPW RETICLE:

4 – 3mm x 3mm (Logic Only)

3 – 5mm x 5mm
- **2 – Logic Only**
- **1 – Full Feature Set**

2 – 7mm x 7mm
- **1 – w/Extra Memory**
- **1 – Full Feature Set**

1 – 10mm x 10mm (Full Feature)

Die Features of Micro-RDC's Design-Hardened SASIC

- **10 Individual Customer Designs are Fabricated per Lot**
  - 50 Die of each Customer Design are fabricated per Wafer
  - A Minimum of 3 Wafers are Fabricated per Lot, providing ~150 die/Customer Design

- **Features Available within each Die:**

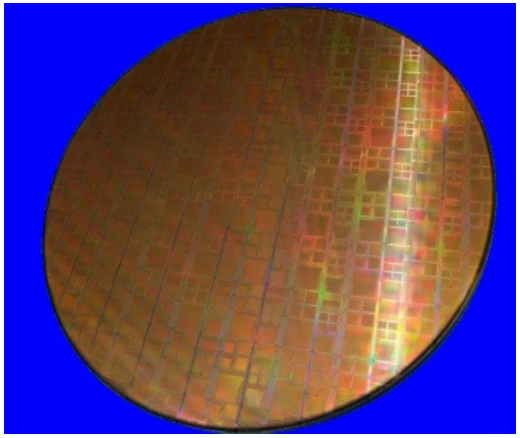
Die Size (mm^2)	User Die / Reticle	CMOS User IO	LVDS*	Equivalent Logic Gates	Distributed DP SRAM Memory	Block Memory SRAM w/EDAC	VROM	SERDES	PLL
~ 3 X 3 (LO)	4	96	None	~107K	~78K Bits	None	288K Bits	None	None
~ 5 X 5 (FF)	1	118	4 Pair	~177K	~129K Bits	5 Blocks 8K X 8 / Block	288K Bits	4 Channels	1 PLL
~ 5 X 5 (LO)	2	158	None	~293K	~213K Bits	None	288K Bits	None	None
~ 7 X 7 (FF)	1	192	8 Pair	~490K	~356K Bits	8 Blocks 8K X 8 / Block	288K Bits	8 Channels	1 PLL
~ 7 X 7 (EM)	1	248	None	~225K	~164K Bits	32 Blocks 8K X 8 / Block	288K Bits	None	None
~ 10 X 10 (FF)	1	256	16 Pair	~1.17M	~848K Bits	12 Blocks 8K X 8 / Block	288K Bits	16 Channels	1 PLL

LO = Logic Only; FF = Full Feature; EM = Extra Memory

* LVDS IO is only available if not using the SERDES channel(s)

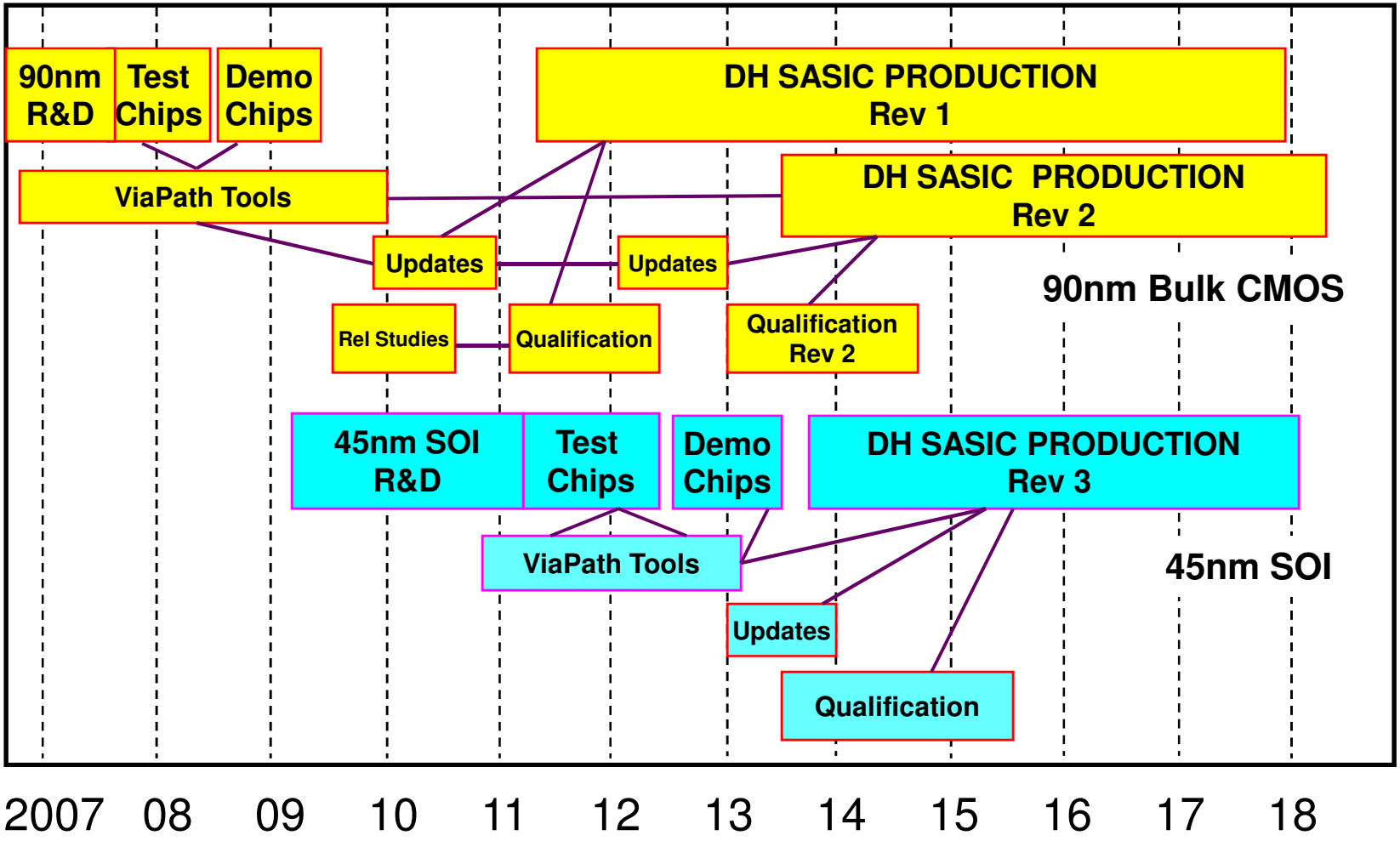
Micro-RDC's Productization Status

- **P&Q Program is in progress**
  - FMEA Complete – 31 Areas of IBM's 9LP process were investigated – no issues
  - Physics of Failure Studies are Complete - Greater than 15 yr. life expected
  - Tech. Qual. for QMLV to be completed in early 2012



- **1st Fabrication Lot is Complete**
  - 6 Customer Designs + 3 Test Chips & SEC Qual. Chip
- **2nd Fabrication Lot is in Process**
  - 9 Customer Designs & SEC Qual. Chip
- **Next Fabrication Lots are now being planned**
  - March 2011 and June 2011
- **Next Design Class / Workshop to be held in December or January**

D-H Structured ASIC Roadmap



Summary

- **Micro-RDC & ViASIC have developed a Family of General-Purpose Structured ASIC Die fabricated within an MPW Reticle**
  - 90 nm On-Shore Trusted Foundry - Leveraging existing Advanced Technology
  - Fabrication of a variety of die sizes/features per fab run
- **Designs use Hardened By Design Libraries/Macros**
  - Excellent Device Hardness (Contact Author for more information)
  - Temporal Latch structures provide SEU and SET mitigation
  - Pre-developed Hardened Macros (SERDES/LVDS, PLLs, Block SRAM, Via-Config. ROM)
- **Providing Advanced, High Performance Hardened-by-Design ICs**
  - Dense Logic – 100k Gates/mm2
  - Reasonable Speed – GP IO up to 125 MHz or 1.25 Gbps SERDES/LVDS
  - Low Power – Much Lower power than FPGA's, Low Voltage (1.2V core & 2.5V IO)
- **Enabling Significant Cost Reduction (~3X lower than low volume ASICs)**
  - Greatly reduced design cost/cycle time over custom ASICs
  - Reduced & Shared NRE and fabrication cost (One layer configurability and with the use of Multi-Project Wafer Reticle), providing low volumes of die for Flight
  - Shared Flight silicon qualification costs (Lot qualification die on reticle)

FOR MORE INFO CONTACT: Stephen.Philpy@Micro-RDC.com (719) 531-0805