

LANL CubeSat Reconfigurable Computer (CRC)

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LANL History in Space

Operational Sensors



Vela W-Sensor



GPS IIA/IIR W-Sensor



GPS IIF V-Sensor

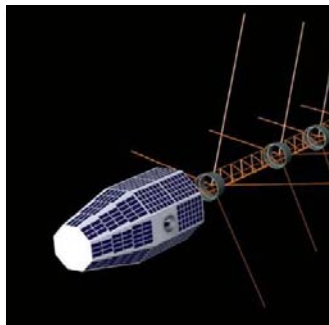


CubeSats

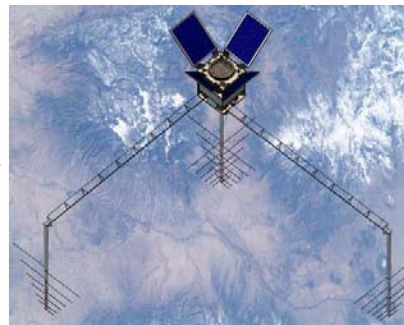
R&D Sensors



ALEXIS/Blackbeard



FORTE



Cibola Flight Experiment



TeraOps SDR

LANL Reconfigurable Computing History (1 of 3)

■ Cibola Flight Experiment (CFE)

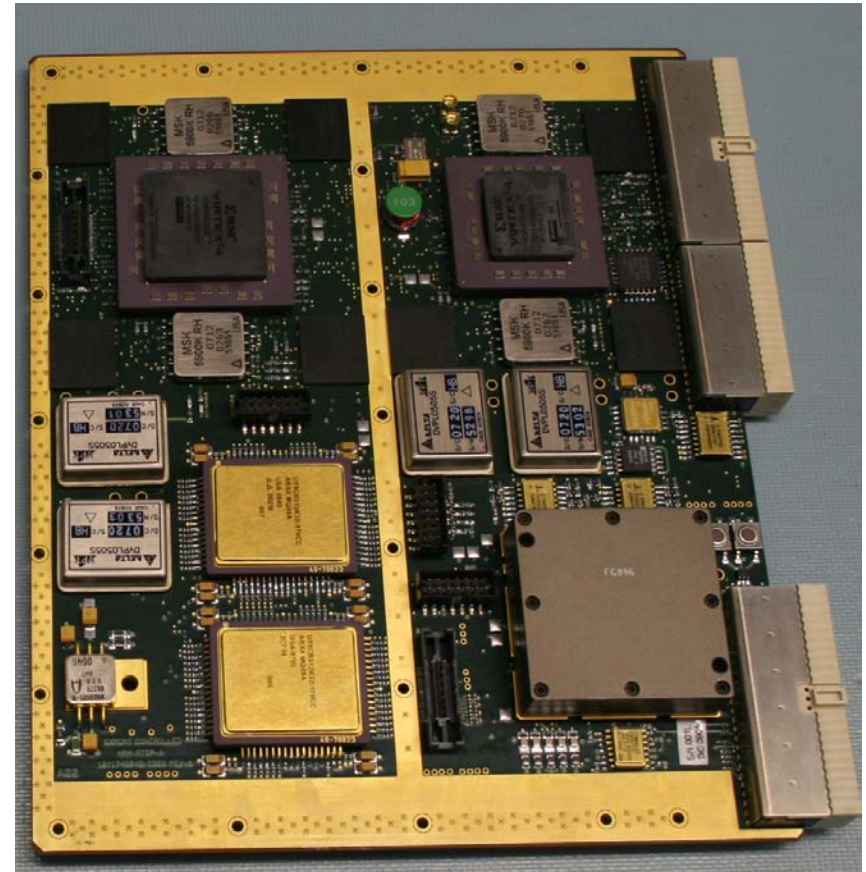
- Experimental Satellite for DOE
- Project Objectives
 - Technology Demonstration: responsive, flexible multi-mission RF payload with continuous data processing
 - Adaptability: Re-configurable post-launch
 - Smart and adaptive reconfigurable computing at sensor for super-computer processing speeds, enhanced sensitivity and reduced data downlink
- Technical Approach
 - On-board data processor using COTS parts
 - Processor includes a network of Xilinx Field Programmable Gate Arrays (FPGAs)
 - FPGAs allow post-launch reconfiguration to meet new and changing program requirements
 - Tailor processing application to each theater of interest
 - Algorithm swap time <1 min
- Payload Description
 - 4-Channel Software Radio
 - Tunable 100-500 MHz with 20 MHz bandwidth
 - Dual 12-bit ADC @ 100 MSPS
- Status
 - Operated for more than 3.5 years
 - Uploaded 50+ new experiments
 - Configured FPGAs 50K+ times



LANL Reconfigurable Computing History (2 of 3)

■ LANL TeraOps SDR

- Experimental payload on an operational spacecraft
- Project Objectives
 - Prove a number of new COTS parts for operational use in space by demonstrating their on-orbit reliability in a radiation environment
 - Test experimental radio applications for DOE treaty monitoring missions, as currently performed in the NDS payload on GPS
- Technical Approach
 - Real-time Signal Processor (RTSP) includes two Virtex-4 FPGAs
 - FPGAs allow post-launch reconfiguration to meet new and changing program requirements
 - Tailor processing application to each theater of interest
- Payload Description
 - Software-defined Radio (SDR)
 - 16-bit ADC @ 120 MSPS
- Status
 - Expected launch in 2011



LANL Reconfigurable Computing History (3 of 3)

■ FPGA Radiation Effects Research

- DOE/LANL has funded more than a decade of research through the CFE, TeraOps SDR, DAPS, SOPRANO and JAS programs
- LANL partnered with Xilinx to perform the first radiation effects experiments on commercial Xilinx FPGAs
- Founding member of the Xilinx Radiation Test Consortium (XRTC)
- Funded development at Brigham Young University (BYU) of BLTMR, an open-source TMR tool (<http://sourceforge.net/projects/byuediftools/> or <http://reliability.ee.byu.edu/>)
- Dozens of peer-reviewed journal articles, conference papers, invited talks, etc.
 - Cross-section Measurements
 - Fault-injection
 - Persistence
 - Multi-bit Upsets (MBUs)
 - Multiple Independent Upsets (MIUs)
 - SEU Mitigation Methods
 - TMR
 - Partial TMR
 - Duplication with Compare
 - Alternative approaches (Quadded Logic, State Machine Encoding, Temporal Redundancy)
 - Smart Models
 - etc.
 - High-speed Serial (MGT)
 - etc.

LANL CubeSat Reconfigurable Computer (1 of 2)

■ Project Objectives

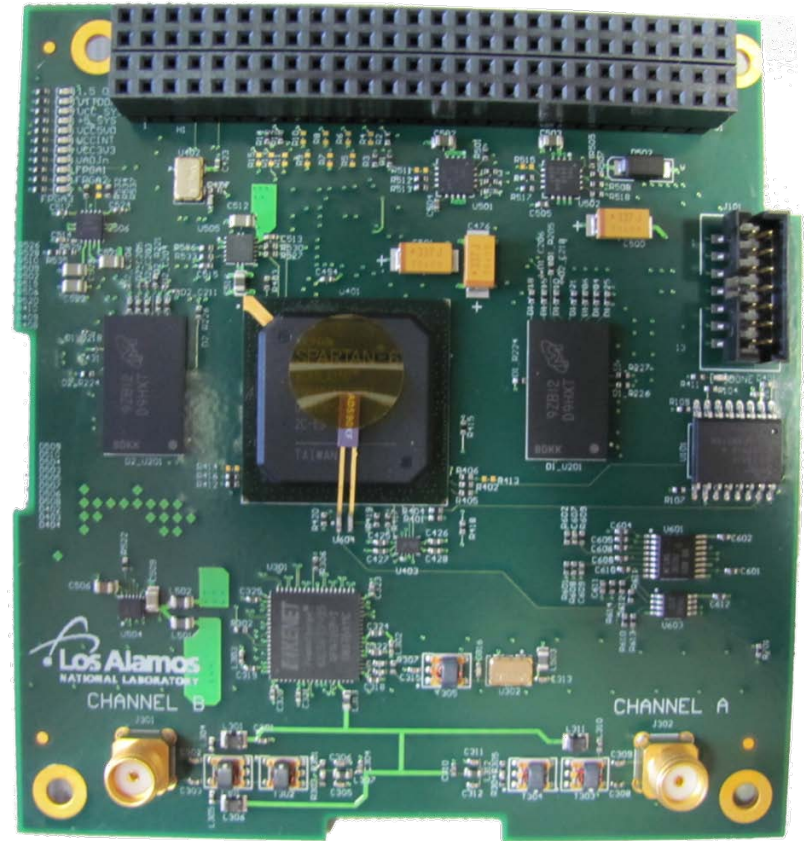
- IRAD for future LANL projects
- Demonstrate reconfigurable computing capability within the constraints of a CubeSat
- Reduce size, weight and power (SWAP) i.e. miniaturize CFE / TeraOps SDR

■ Technical Approach

- Single board with low-power/high-performance FPGA, memory and ADC
 - Xilinx Spartan-6 LX150 FPGA
 - 2x 2-Gbit Micron DDR3 SDRAM chips
 - 2 Channel ADC; 12-bit @ 250 MSPS
 - 102 pin connector to on-board computer; compatible with Pumpkin CubeSat Kit
 - 128-Mbit on-board Flash bitstream storage

■ Status

- Received CRC from manufacturing 7/26/2010
- Built-in self test (BIST) complete
- Demo application in progress



LANL CubeSat Reconfigurable Computer (2 of 2)

Comparison of CRC with CFE and TeraOps SDR

		CFE	TeraOps SDR	CRC
Size		16" x 8" x 12"	10.5" x 3.4" x 9"	4" x 4" x 1"
Weight		20 Kg	5.5 Kg	100 g
Power		100 W	25 W	10 W
# FPGAs		9	2	1
	Logic Cells	249K ¹	255K ¹	150K ²
	On-chip RAM	1 Mb	13.6 Mb	5 Mb
	DSP Slices	0	608	180
# ADCs		1	1	1
	Sample Rate	100 MSPS	120 MSPS	250 MSPS
	# bits	12	16	12
	# channels	2	1	2
System memory		.86 GB ³	.25 Gb ⁴	.5 GB ⁵

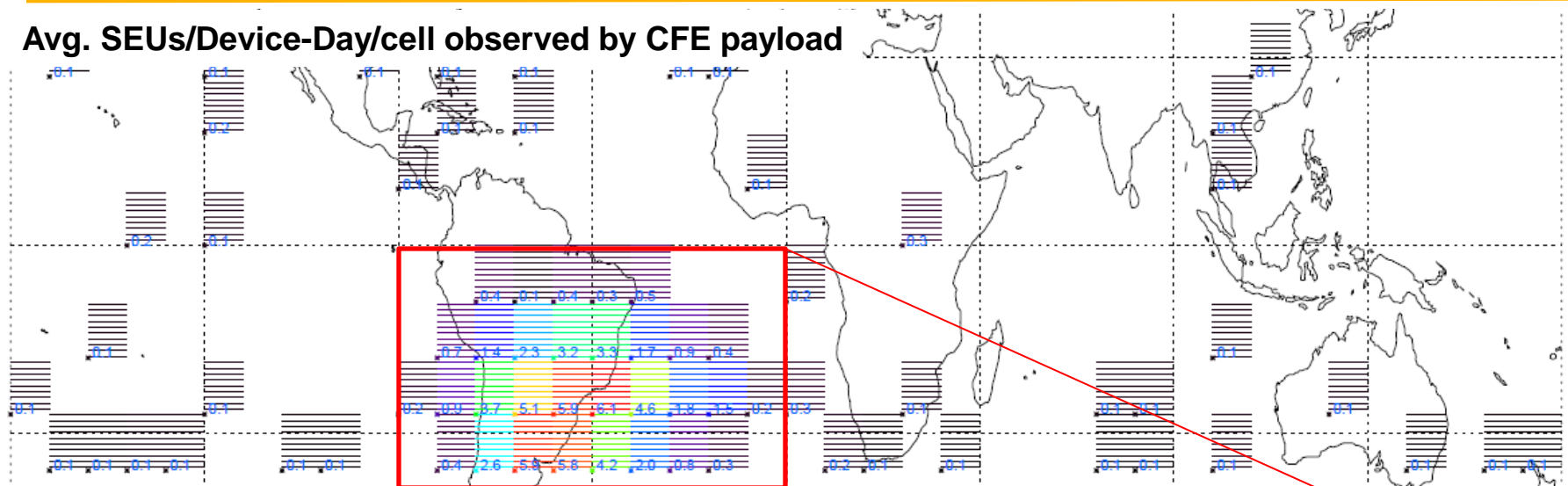
¹4-input LUT ²6-input LUT ³SDRAM ⁴QDR SRAM ⁵DDR3 SDRAM

Benefits of Reconfigurable Computing and CubeSats

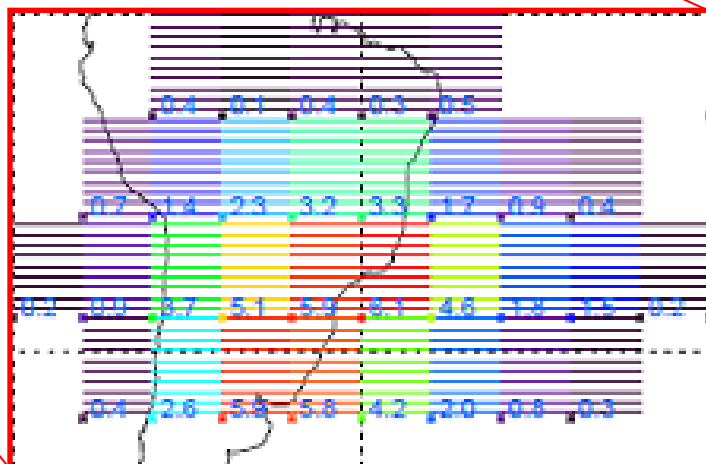
- **High performance, low-power computing in a small form factor**
- **Upgrade or add functionality after launch**
- **Hardware Reuse**
 - Enhances reliability
 - Decreases cost
 - Increases code base
 - Accelerates development time
- **Simplifies hardware design for CubeSat constellations**

Challenges of Reconfigurable Computing and CubeSats: Single Event Upsets (SEUs)

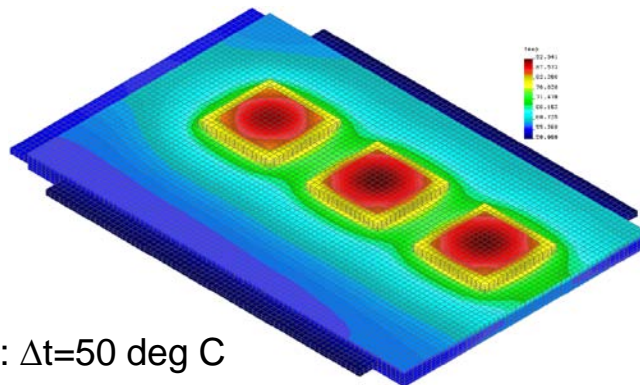
Avg. SEUs/Device-Day/cell observed by CFE payload



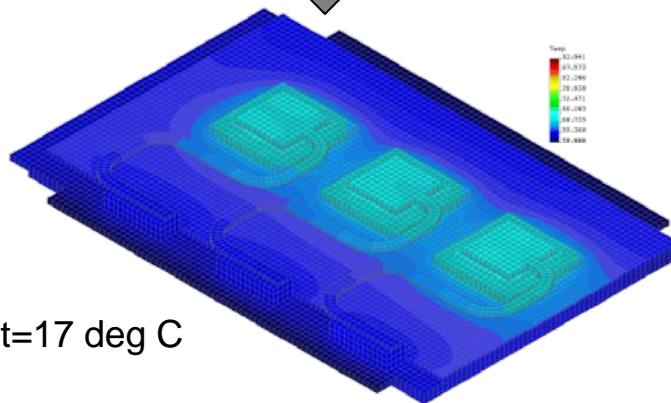
Avg. SEUs/Device-Day
observed by CFE payload:
0.25



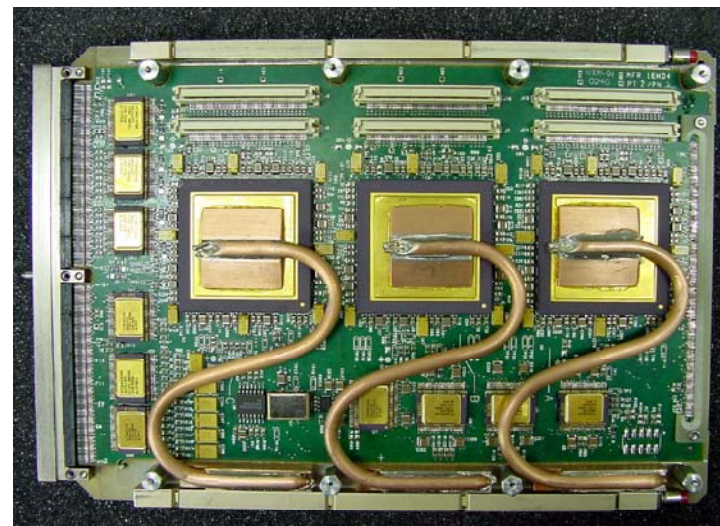
Challenges of Reconfigurable Computing and CubeSats: Thermal Management



Without heat pipes: $\Delta t = 50$ deg C

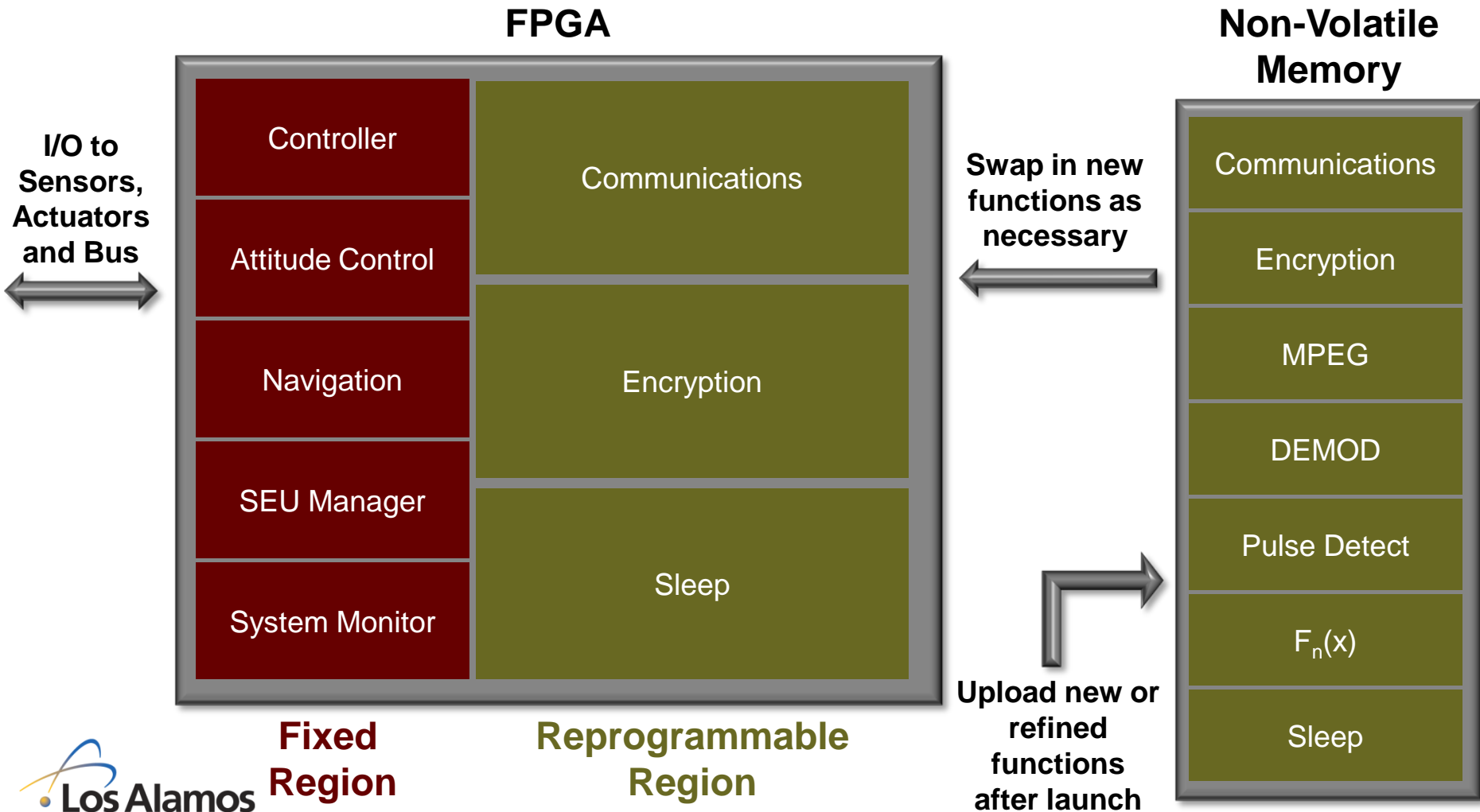


With heat pipes: $\Delta t = 17$ deg C



Proto-Flight CFE reconfigurable computing board with heat pipes

“Software-defined Satellite”



Future Work

■ Example Science Missions

- Wide band RF pulse detection
- Total Electron Content (TEC) in Ionosphere

■ Constellations

- Numerous inexpensive satellites replace larger expensive satellites
- Paradigm shift allows new functions to be performed
- Spatial separation
- Unit replacement
- True global and persistent observation

Summary

- **LANL has decades of experience with satellites/payloads and reconfigurable computing**
- **The LANL CFE and TeraOps SDR programs demonstrated the feasibility of reconfigurable computing in space**
- **LANL CubeSat Reconfigurable Computer (CRC)**
 - High performance, low-power reconfigurable computing in a small form factor
 - Upgrade or add functionality after launch
 - Hardware Reuse
- **SEU and thermal challenges are manageable**
- **Technology enables inexpensive & interesting science missions and constellations for true global persistent surveillance**