Introducing the HyperX Manycore Processor for Space Applications

for
MAPLD
02 Nov 2010

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Coherent Logix™

Photo Courtesy NASA

Corporate Profile

- Coherent Logix is the industry's innovation leader and producer of low-power, high performance, high-reliability C-programmable many-core processors for embedded systems
- HQ in Austin, TX
  - 80+ Employees
  - Engineering in Austin, TX and San Jose, CA
  - Processor, Systems and Applications expertise in-house
- Served Markets
  - Mil/Aero/Industrial/Commercial
  - Autonomous/Robotic Systems
  - Radio/Communications (SDR)
  - Image/Video Processing

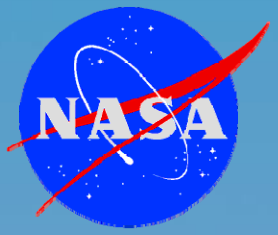





Product Portfolio

- Low-power, High-performance, High-reliability Processing Platform
  - Chips, Boards and Systems
    - HyperX Processors in Common or Custom Packaging
    - HyperX Development Systems
  - Application Development Tools
    - Fully featured and mature suite of modeling, design and testing tools
    - Covering the full development process from initial concept to system test
  - Application Software and Libraries
  - Reference Systems
    - Radio and Waveform Development System (RWDS)
    - Video and Imaging Development System (VIDS)
- Application Development Support Services
  - Expertise
    - Support - Training and Advice
    - Contract – Design, etc
  - IP Licensing (radio, video, etc)

HyperX Sponsors



- Military Waveforms – SRW, other
- SDR Waveform Development Platform
  - Libraries, OFDM, etc
- Cognitive/Adaptive Radio
- GPS Receiver
- Anti-Jam
- Surveillance

- Next Gen Processor

- Hyper Spectral Imaging
- Image Stabilization
- Super Resolution
- Video-Imaging Development System

- Acoustic Processing

- Radiation Hardening by Software

- SONAR Processing
- Other…

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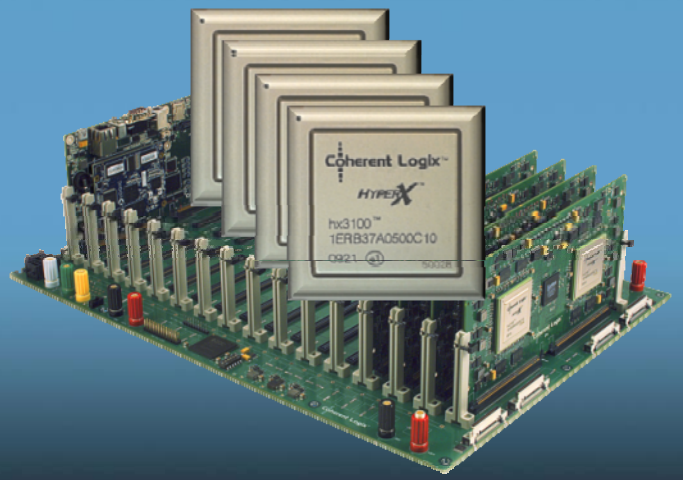
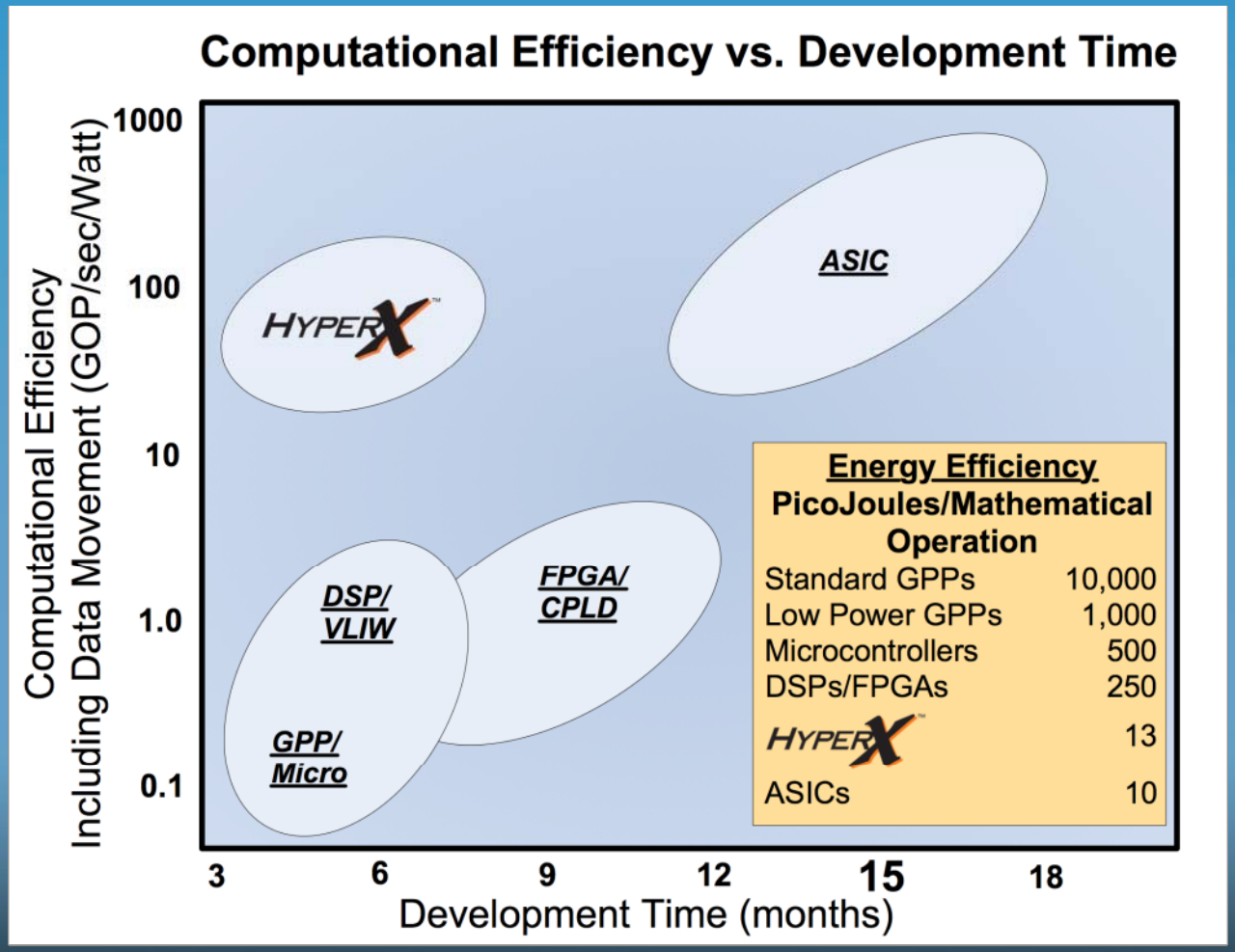
Why? What's the Point of Manycore Processors?

- Silicon limits – especially power density – naturally leads the industry toward manycore processors
- High performance without the power, size, cost, etc of an HPC system



Computational Efficiency vs Development Time



Comparison

Intel GPP: 10,000 pJ/op
ARM: 500-1000 pJ/op
DSP, FPGA: 250-350 pJ/op
ASICs: 10-20 pJ/op
HyperX: ~13 pJ/op

VLIV/DSP Architectural Barriers to power:

- Multilevel cache
- Buses
- Data Path Efficiency

FPGA' Architectural Barriers to power:

- Programmable Wire
- Fine grained parallel
- Forced distributed memory
- Timing closure

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The Ascent of Many-core Processors (MCP)

- MCPs have recently began making inroads into applications traditionally served by networks of FPGAs, CPUs/DSPs and full custom ASICs

- Range of applications served by MCPs today
  - Real-time Applications
    - Video & Image Processing
    - Radio (Digital Communications)
    - Robotics (and Autonomous systems, in general)
  - Post Processing
    - Server Farms (for Information Mining, etc)
    - … and more

Many-core Advantages and Challenges

- Advantages
  - Inherent redundancy (to be used for fault tolerance)
  - Reconfigurable and Adaptable computing platform
  - Computational density (compaction) / processing power
  - Integrated system development environment
- Challenges
  - Programming
    - Parallelism - tools & experience
    - Has been done for years in High Performance Computers
      - What can we learn from the HPC industry?
    - What can software designers learn from AISC development flows?
  - History and Perception of Risk
    - Shallow pedigree and lack of experience (unfamiliarity)
    - Cutting Edge means on the edge?
    - Early adopters have the competitive advantage?

Advantages - Disadvantages

- FPGA
  - A: Reprogramability and Time to market
  - D: Logic configuration is SRAM based → configuration upsets
  - D: Writing RTL in an HDL for a particular device is low-level, time-consuming work compared to writing in C
- ASIC
  - A: Most highly optimizable to the exact function desired
  - D: Expensive and Risky – with long development times and locked-in functionality
- HyperX Many-core Processor
  - D: Software programmable (instruction memory)
  - A: Software programmable with standard non-proprietary high-level language (rapid prototyping, evolving standards, feature improvements, in-field upgrades, etc)
  - A: Industry leading computational efficiency (GFLOPS/W or pJ/op)
  - A: Natural redundancy available – other error detection, correction, containment, mitigation and recovery features can be built in (as hardware features)

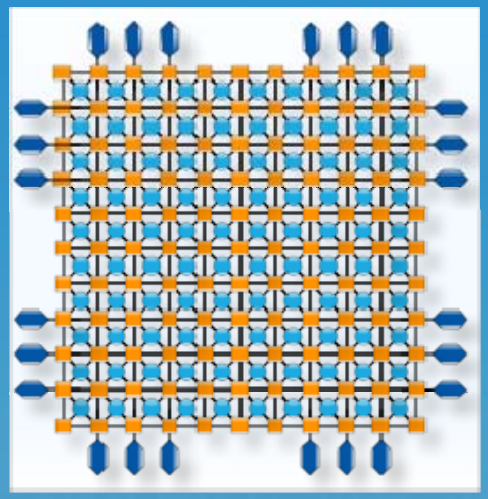
More Advantages

- A: Scalability
  - Not trading off clock speed and performance when additional resources are needed (like you would be with a lesser processor)
  - The number of cores is a design variable – you can use 1 or 8 or 16 or 25 or 400 (or more) – depending on your application – and this can be a dynamic variable
- A: Power Efficiency
  - Requires less communications infrastructure
  - Designed (not retrofitted) to only use power when required, like the combustion engine in a hybrid car

Risk Management – Risk vs Reward

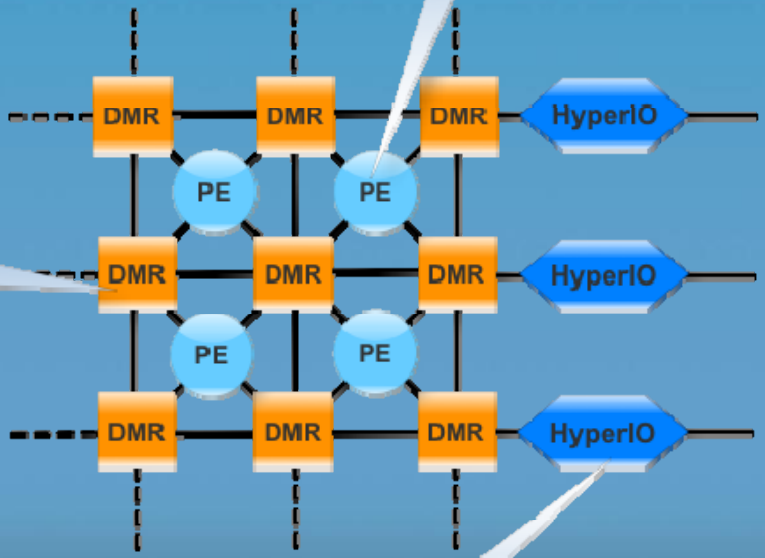
- Ok, many-core processors sure sound like fun to me, but do I dare to bring one home to mama? What if it is
  - Too hard to handle → short relationship
  - Too needy → short relationship
  - Too embarrassing → short relationship
  - Too flakey (unpredictable and undependable) → short relationship
  - Too exotic and different than previous (unfamiliar) → uncertain
  - Too noisy → ok, that's irrelevant
- Making mama happy – the HyperX Manycore Processor
  - Integrated Development Environment (C programmed) → encourages and supports productivity
  - LOW power → long battery life and, therefore, much less system mass
  - Natural Reconfigurability → much less work and less pain
  - HIGH performance → doing more with less
  - HIGH reliability → no worries
  - Familiarity → become comfortable quickly

hx3100 Many-Core Processor



100 Processor Elements
4 kB program memory per PE
500 MHz variable clock
8, 16, n x 16 integer
32 bit floating point
50,000 MIPS, 50 GMACS 16 bit
32 bit Floating Point, 25 GFLOPs

121 Data Memory Routers
8 kB data memory per DMR
8 independent DMA Engines
986 kB total configurable on chip memory
Real time algorithm topology switching
High Speed neighbor communications
High speed cross-chip communications
Autonomous Data Movement



Low Power
75 mW to 3.5 W typical core power
Automatic resource power management
Chip power-off by quadrant
16 GFLOP/s/W (16 bit)
>75 GOP/s/W (16 bit)
>1.2 TOP/s/W (16 bit RISC equivalent)

High Speed I/O Routers
16 HyperIO Channels, 16 bit wide (24 ch)
DDR2: 4 channels, 32 Gbps (8 ch, 64 Gbps)
LVDS: 8 channels, 64 Gbps (12 ch, 96 Gbps)
CMOS: 6 channels, 12 Gbps (12 ch, 24 Gbps)
104 Gbps simultaneous (168 Gbps)
Access to 64 Gbps off-chip memory

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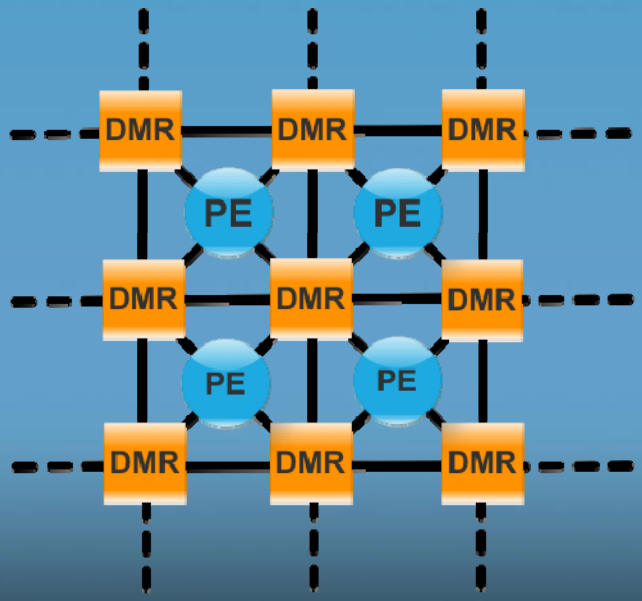
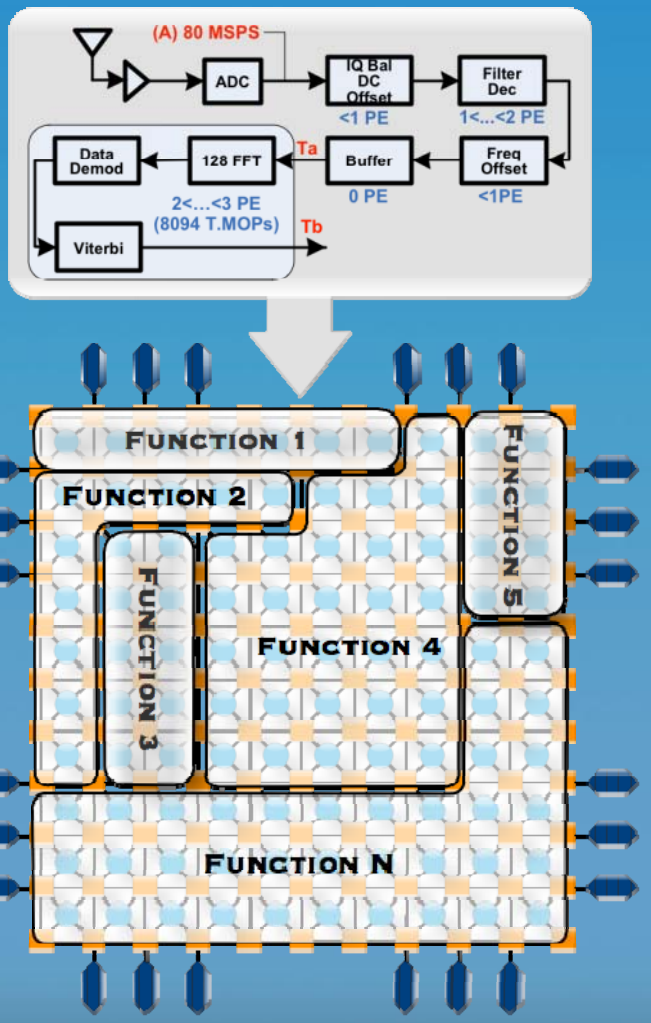
Functions to Fabric

- A compute fabric of 100 processors within a network of 121 data memory routers
- User configurable, adaptable in real time
- Supported by high bandwidth intercommunications for efficient data movement
- Each DMR contains 8 kB data memory + 8 DMA engines for neighborhood or cross chip data transfer





- Allows the appropriate topology to be created to support the natural parallelism of the algorithm / system
- without stalling resources in use
- and only clocking or powering what is needed
- … thus creating a highly efficient, low power system

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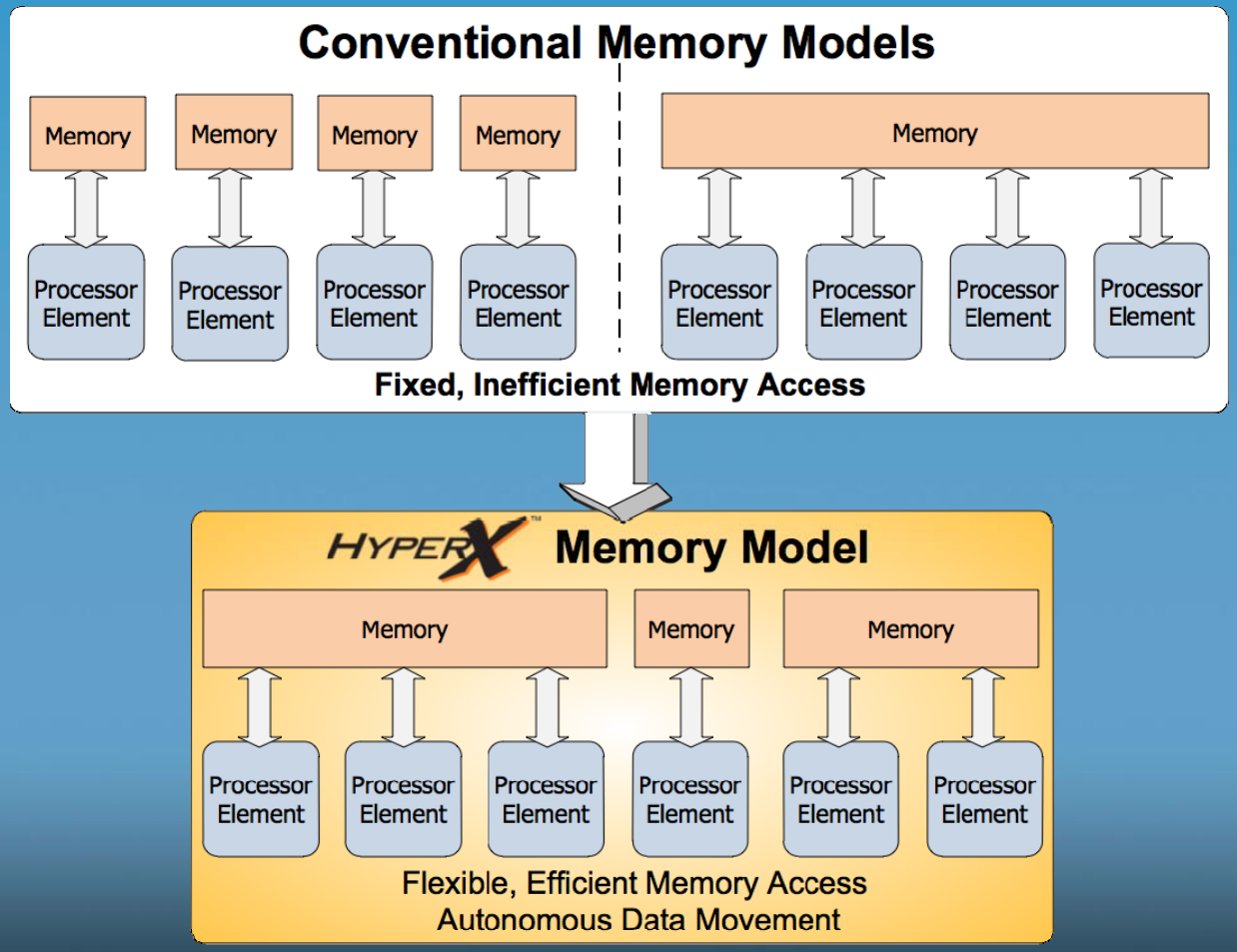
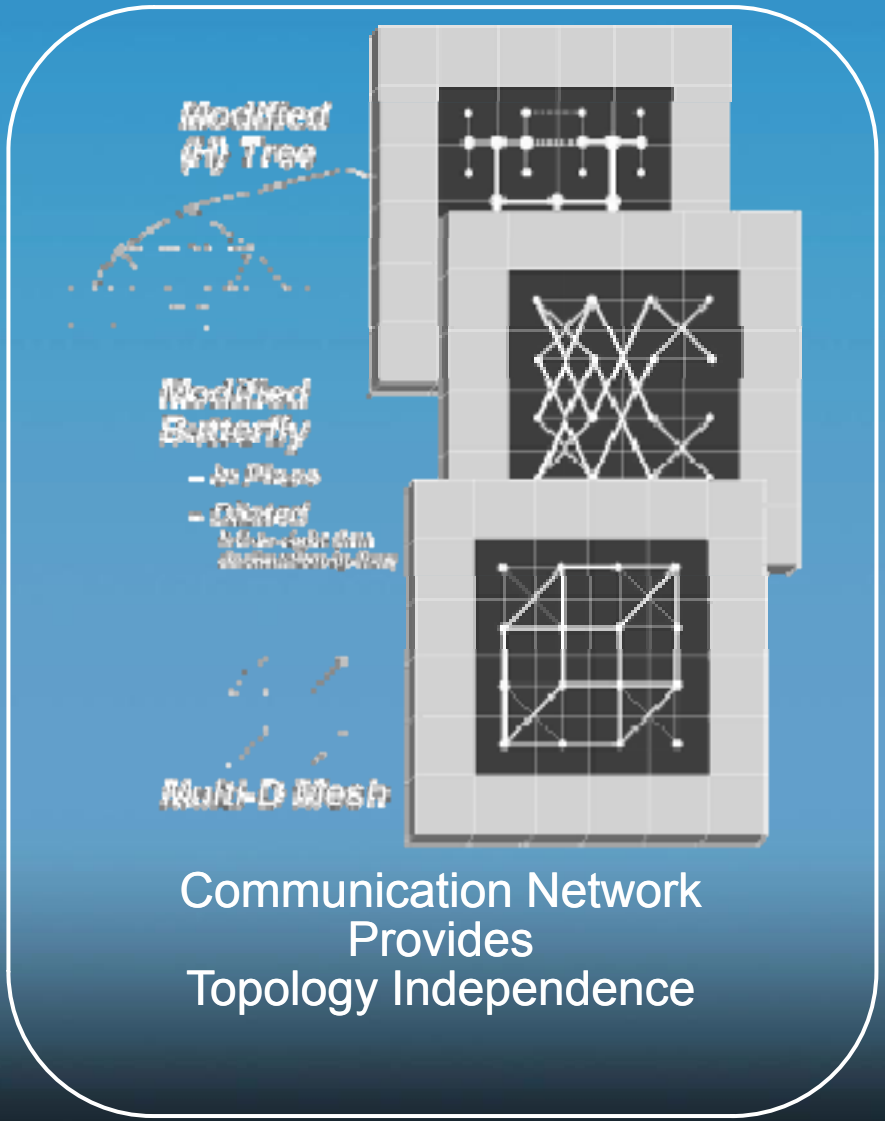
Supports Multiple Memory Architectures

- Supports a mixed memory programming model
  - vs. fully distributed or fully shared
- Adaptable and reconfigurable in real-time



Supports Multiple Communication Topologies

- Communication network is topology independent
- Adaptable and reconfigurable in real time
- Allows the appropriate hardware topology to be created to support the natural parallelism of the algorithm / system …
- … thus not constraining the algorithm / system to a particular topology



Communication Network
Provides
Topology Independence

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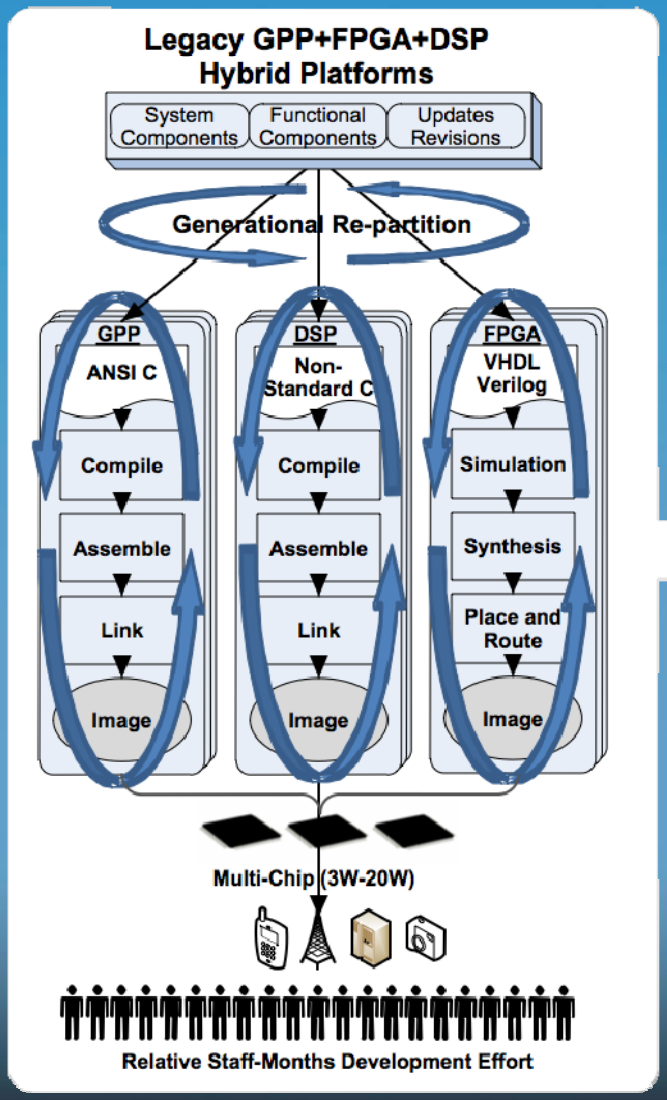
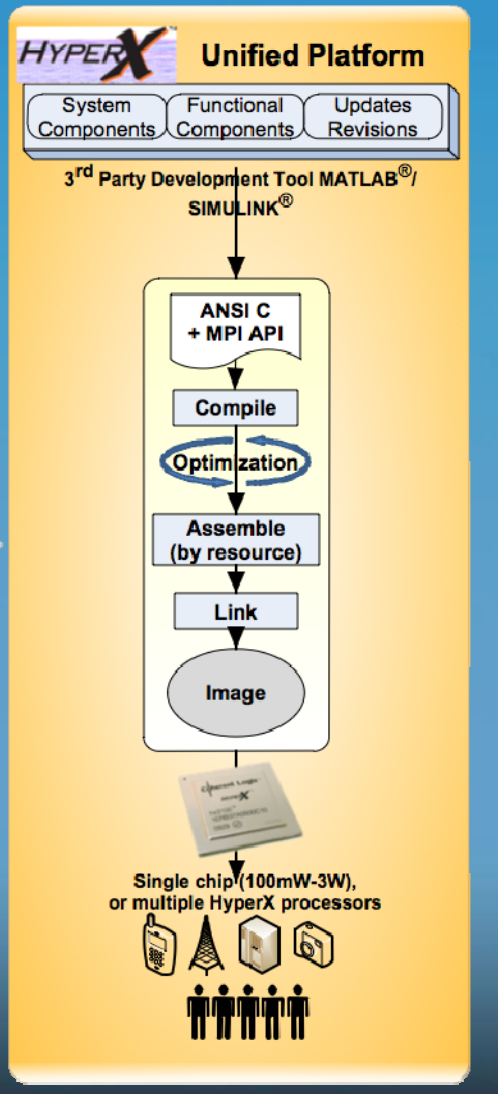
HyperX System Design

Software System-on-a-Chip vs. Hybrid Architectures:

- 1/10th the power
- 1/5th the design time
- Ease of IP re-use
- No generation re-partition





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hx3100 Benchmarks

Radio Processing

- 1024 FFT, 16 bit Fixed Point, 500 MHz
  - Using 1 Processor Element
    - Streaming 88 us per FFT; 11,363 FFTs per second
  - Using 80 Processor Elements
    - Streaming 1.3 us per FFT; 769,230 FFTs per second
- 32K FFT 500 MHz
  - Fixed-point (16-bit), streaming 65 us per FFT, 15,258 FFTs per second.
  - Floating-point (32-bit single precision) streaming, 316 us per FFT, 3170 FFTs per second

Video/Image Processing

- Hyper Spectral Image Fusion and Target Detect
  - Data Cube: 512V*512H*32 wavelengths *16-bits = 64 MB, where 1 MB = 220*8-bits
  - Uses Spectral Angle Correlation Methods, 4,505,600 Cycles per HSI Data Cube 56.82 Gbps Aggregate Data Input (Dominated)
  - ~1000 Operations per Pixel30 cubes/second,
  - uses approximately 50% of the processing resources on the h3100, ~2W core power
- Image Stabilization
  - 600 x 800 image, full color, 12 bits per pixel
  - 30 fps Bayer2RGB / Yuv <1.2 frame latency
  - 11x11 DOG filter Corner detection and 200 point tracking / matching RANSAC model fitting 4x4 Bicubic interpolation Uses
  - ~90% of the processing resources, ~3W core power
  - 10x performance over Intel solution<1/10 of power
- 2k-x-2k JPEG Encoder
  - Performs @ > 45 fps (~1.51 Gbps input data rate) on hx2100
  - Performs @ > 90 fps (~3.02 Gbps input data rate) on hx3100

Solving the Parallel Programming Mystery: FAST Design Flow

Functional

- Capture the logical functionality of the system
- Capture representative precision
- Capture dynamic range
- Determine the theoretical mathematical operations for each function

Architectural

- Specify the performance constraints in the form of input / output data rate(s)
- Specify any latency requirements to the functionality defined in previous step.

System Design

- Analyze the functional and architectural constraints
- Optimize the design to meet functional and architectural requirements on the target hardware
- Develop an ANSI C program using standard coding techniques employing a representative natural hierarchy derived from the functional and architectural analysis process

Transformation to Hardware

- Automated mapping of the ANSI C program to the target hardware by the HyperX ISDE suite.

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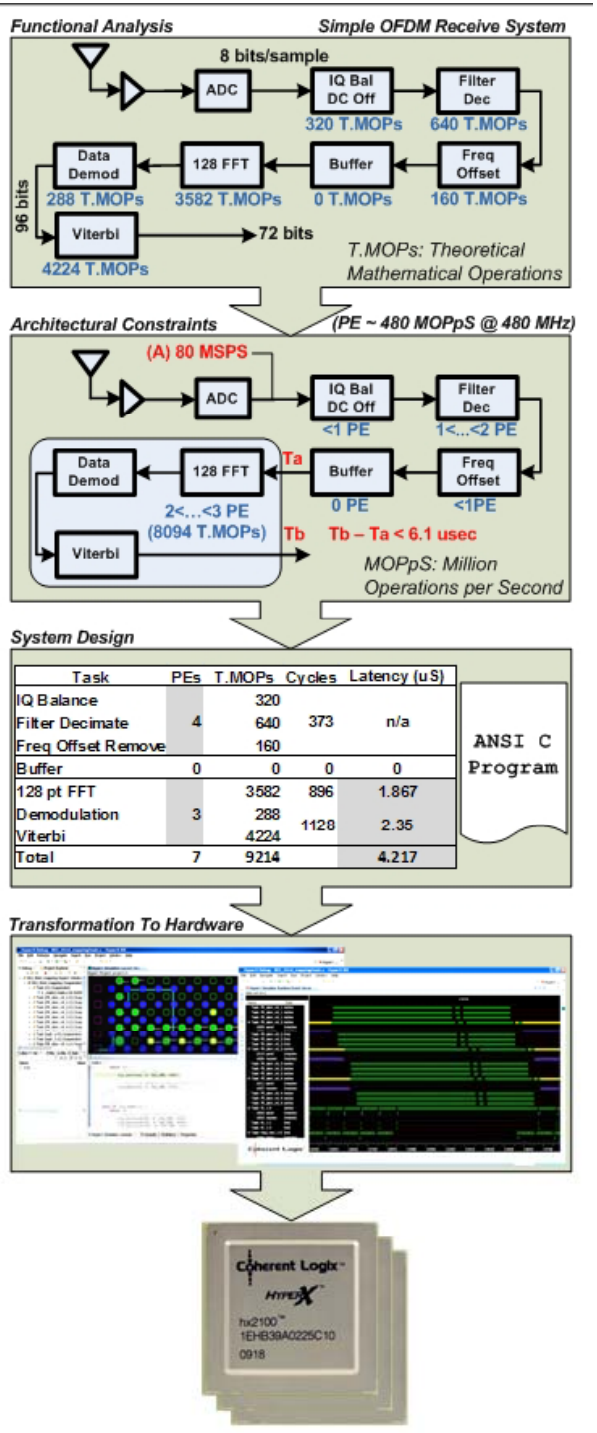

Back-up Slides

HyperX Processors

hx3100 and beyond

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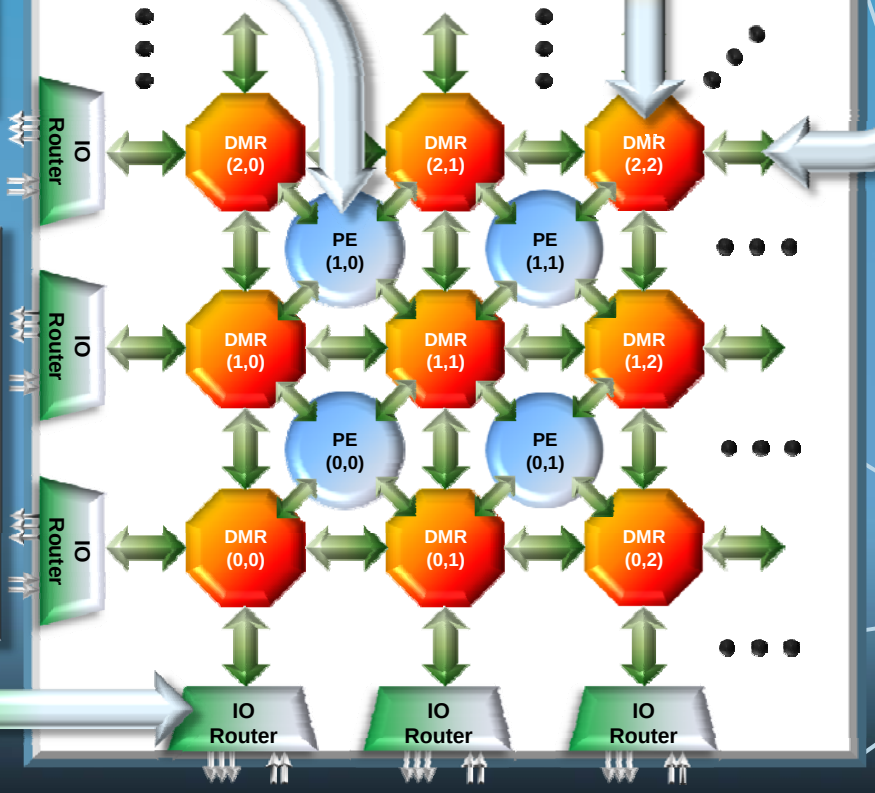
The Engine – What is the HyperX™ Processor: hx3100™

121 Data-Memory-Routers (DMRs)
- Memory Embedded in Network or Network Embedded in Memory Architecture
  - Hierarchical, Multi-Dimensional Communications
  - Physically Flat Memory
- 968KB of total on-chip data memory
  - 8KB data memory per DMR

100 Processing Resources (PEs)
- GPP/DSP w/ Variable clock to 600MHz
- Supports data types: 8, 16, Nx16-bit integer, & 32-bit floating point
- 400KB of total on-chip program memory
  - Each PE supported directly by 4KB
- @ 500MHz
  - 50,000 MIPS
  - 50 16-bit GMACS
  - 100 8-bit GMACS
  - 25 GFLOPS

Dynamic On-chip Memory-Network
- Autonomous data movement
- Instantaneous bandwidth on demand
- Real-time adaptable to support multiple memory and communication topologies



Performance
- 32 16-bit GMAC/s/W
- 64 8-bit GMAC/s/W
- 16 GFLOP/s/W

IO Routers
- 16 Multi-function General Purpose IO Channels
  - Physically Programmable
    - LVDS (EIA-644) and CMOS
  - Logically Programmable
    - GPIO, SYNC, ASYNC, & Multi-chip provides seamless chip-to-chip support *without* glue logic that would compromise performance or break the programming model
- 8 High-Speed External Memory IO Channels
  - 8 Programmable Controllers
  - Supports DDR2
  - Access up to 64 GB of total off-chip memory
- 24 programmable timers

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The hx3100 Processor

- Performance Throughput
  - @ 500 MHz
  - 50,000 MIPS
  - 50 16-bit GMACS
  - 100 8-bit GMACS
  - 25 GFLOPS (32-bit)

- DIE IO Bandwidth:
  - 96 Gbps of LVDS IO
  - 24 Gbps of CMOS IO
  - 64 Gbps of DDR2 IO

- General Purpose Package IO Bandwidth:
  - 64 Gbps of LVDS IO
  - 12 Gbps of CMOS IO
  - 32 Gbps of DDR2 IO

Scalability
Performance
Power
Programmability™
50 mW to 3.5 W
(algorithm dependent)

- Performance Efficiency
  - @ 500 MHz
  - 32 16-bit GMAC/s/W
  - 64 8-bit GMAC/s/W
  - 16 GFLOP/s/W (32-bit)
  - > 1.2 TOP/s/W (16-bit RISC equivalent)

(*) General Purpose Use Package Shown. Die Intended To Be Packaged To Application.

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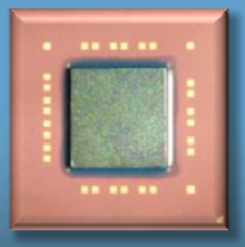
HyperX Silicon Roadmap

Performance (GMACS)

400+
50+
25
15
7.5

2006 2007 2008 2009 2010 2011 2012+

hx1060
60 cores
130nm



hx2100
100 cores
90nm
250MHz
200mW to 3.0W

hx3100
100 cores
65nm
500MHz
75mW to 3.5W
38mm x 38mm package

hx31xx
Small Package

TBD

Optimized ASIC
xx cores
GPP, other

hx4400

400 cores
32nm
1000MHz
Instruction Optimization
25mW to 1.0W

hx3100-RH
100+ cores
45nm
625MHz
50mW to 2W

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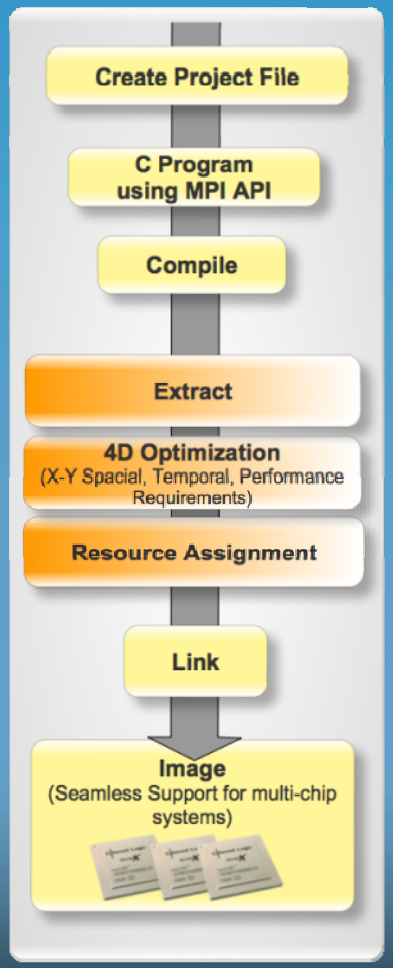
HyperX Integrated System Development Environment

HyperX ISDE

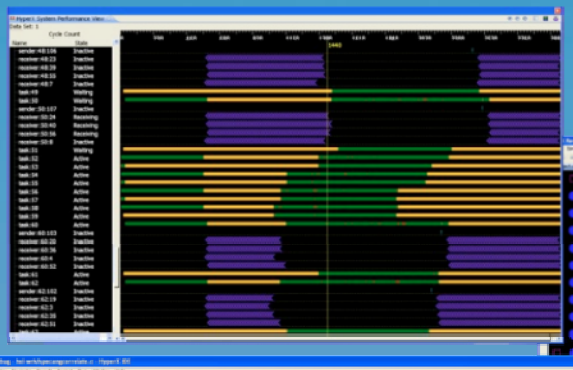
HyperX hxISDE

- Integrated System Development Environment
  - Multiple System Views
  - Integrated Edit, Compile and Make system
  - Source level debugging (C and assembly level)
  - Graphical representation of the program execution in function of the hardware layout (grid viewer) and flow (event viewer)
  - Graphical representation of memory and register content
  - Step, step-over, run for, breakpoint …
  - Watch variables and expressions
  - Various reporting
  - …

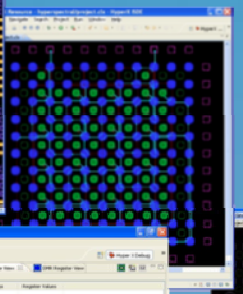
HyperX Integrated System Development Environment (hxISDE)



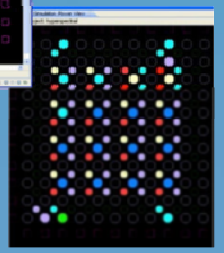
System Performance View
Task Breakdown
Critical Path Analysis
Latency, Power, and Resource Trade-offs

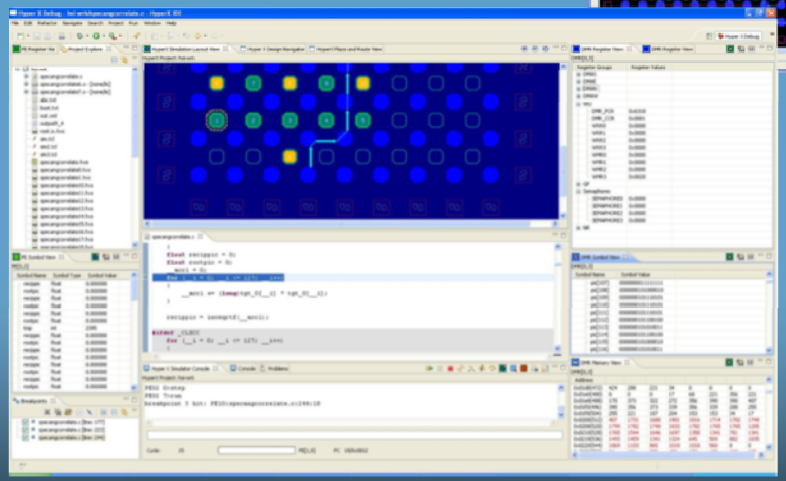


System Communication View
Task Activity on Hardware
Data Routing



System Energy View
Resource Power
Power Optimization





System Centric View
Common Debugger
Cycle Accurate Simulator
Source Code, Variables
Breakpoint
Low level optimization

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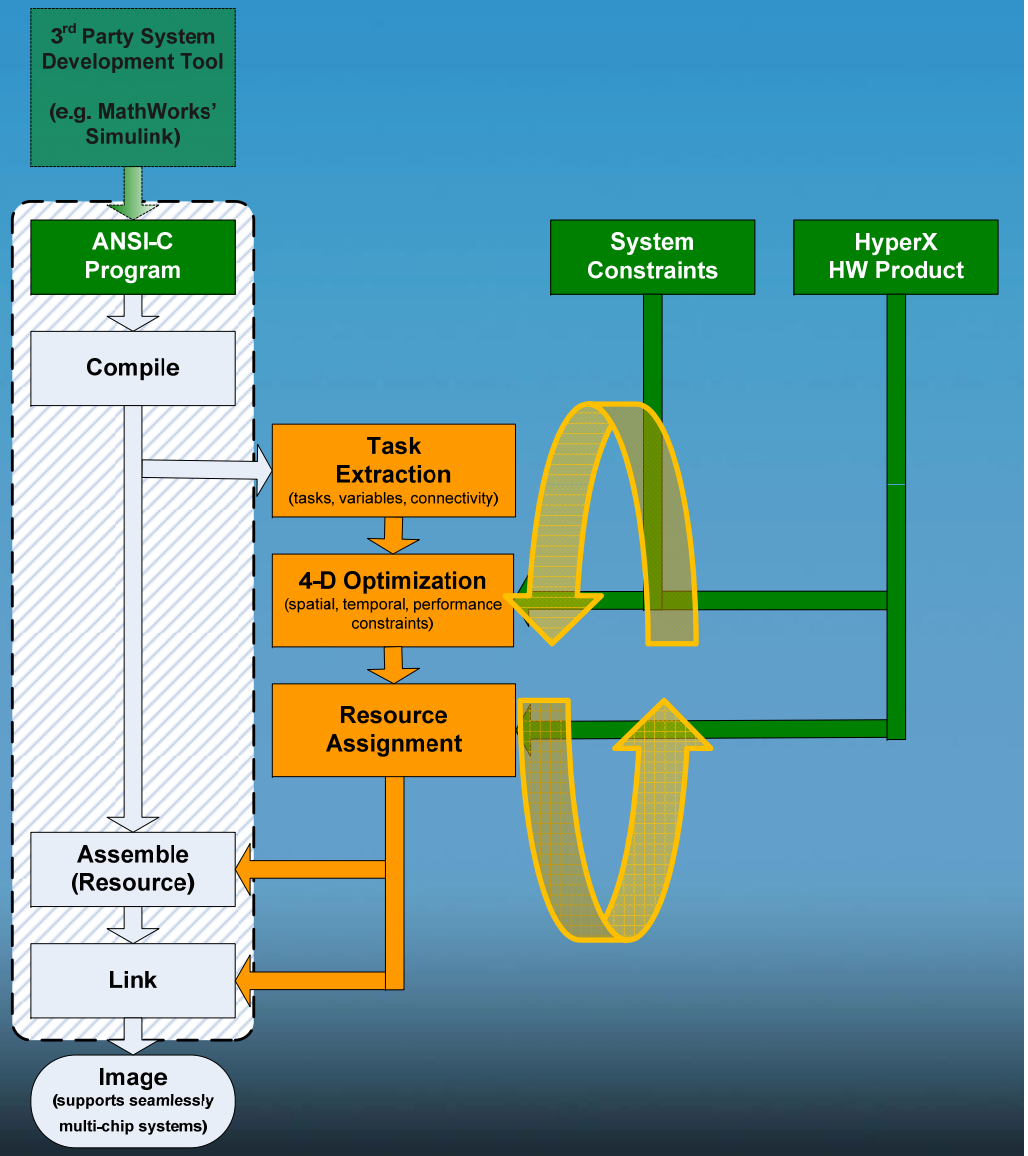
HyperX Development Flow

- ANSI C
- Design re-use through hierarchical library – we call it a “cell”
- Task Extraction
  - Data flow
  - Variables
  - Connectivity
- Optimization and Automated Mapping of Software to Hardware Resources
- Link image for deployment

Perform optimizations (iterations) without changing a line of C code



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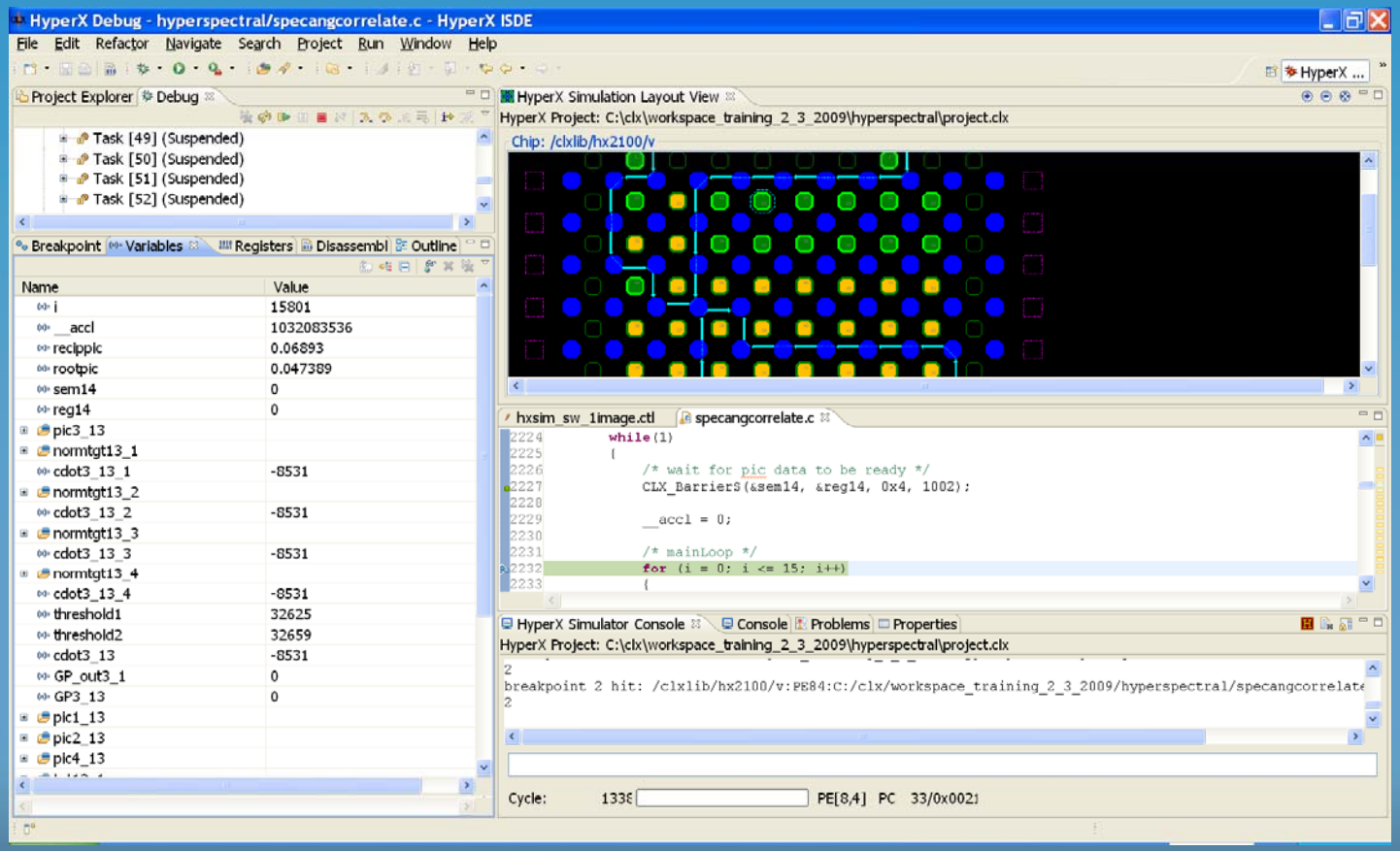
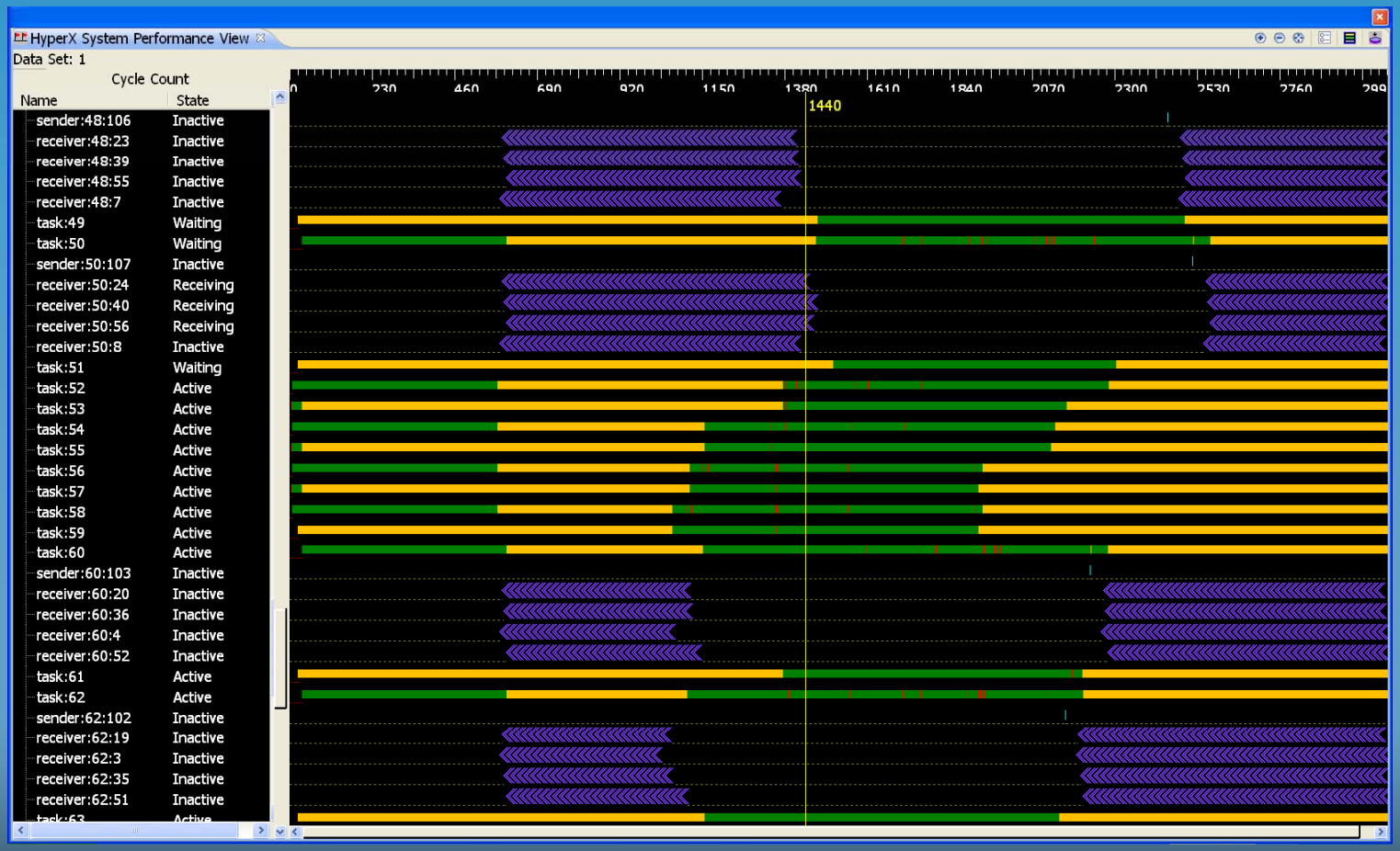
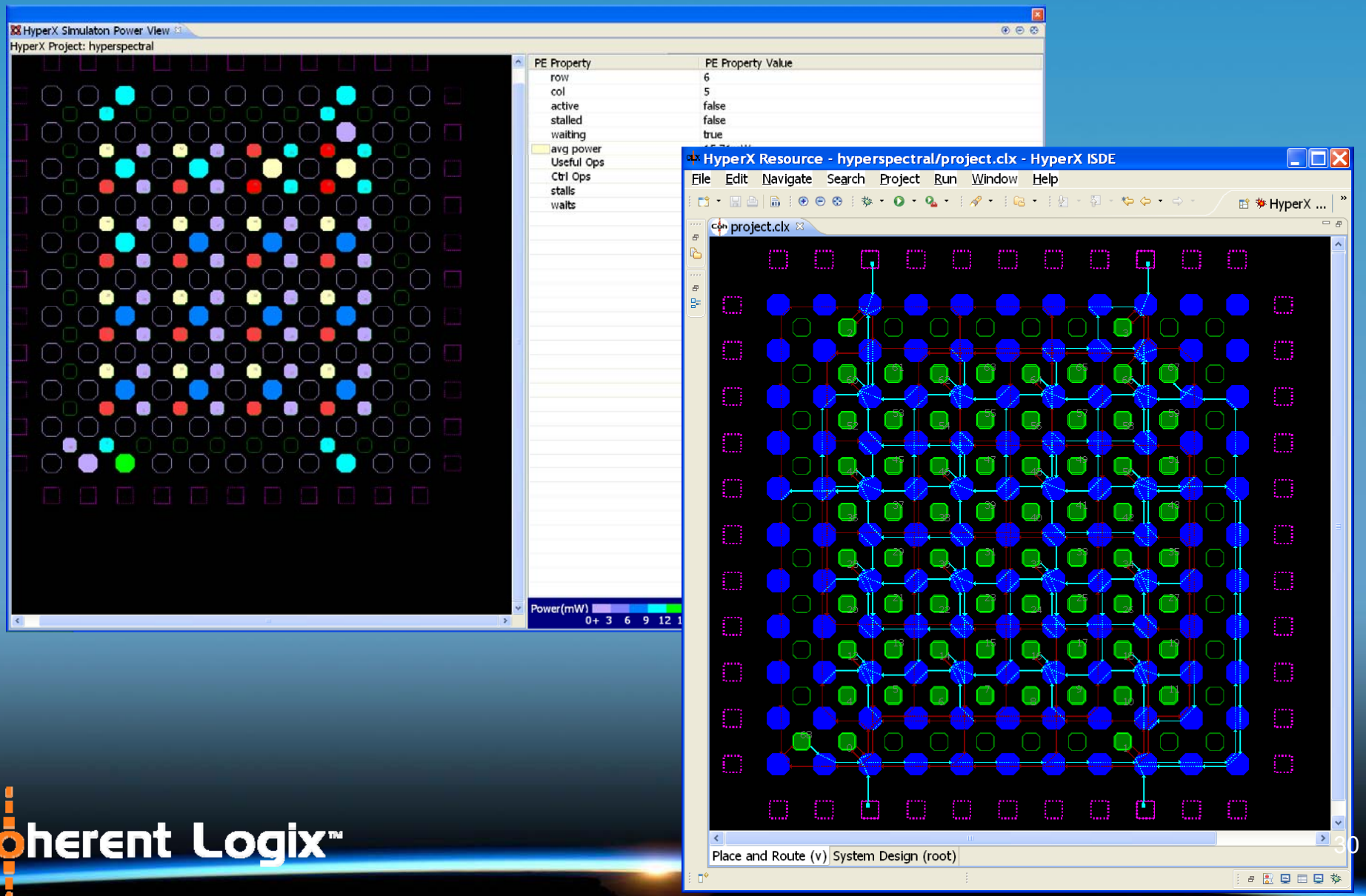
HyperX hxISDE – Screen Shots



HyperX hxISDE – Screen Shots



HyperX hxISDE – Screen Shots



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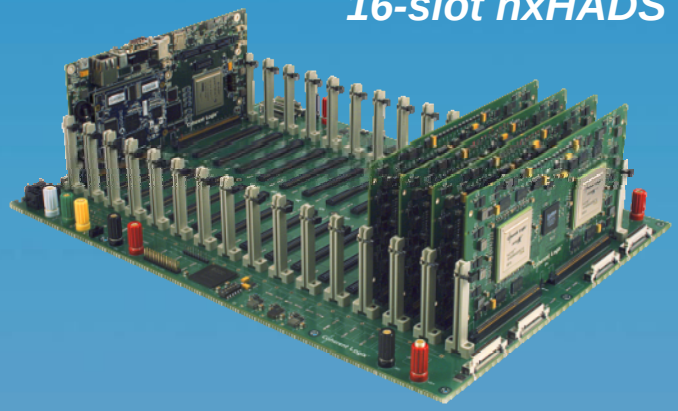
HyperX Hardware Application Development Systems

hxHADS

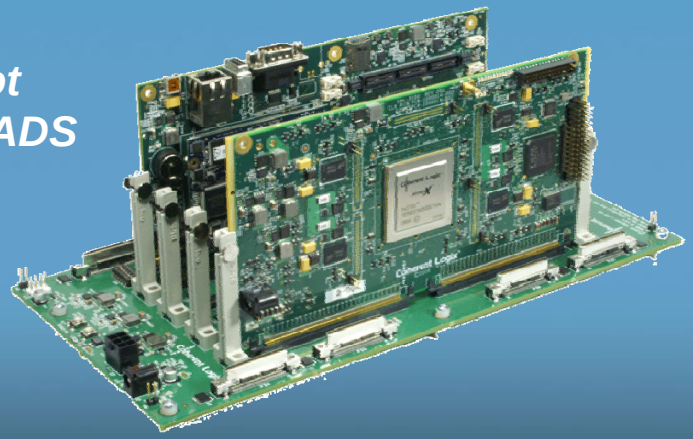
System Application Development – hxHADS2

- Provides full system development, verification, and test solution
- Available Application Specific Configurations
  - Radio Waveform Development System (RWDS)
  - Video Application Development System (VADS)
- Supports Multiple Modules in any configuration
  - 2hx Module
  - 1hx Module
  - GPP-IOI Module
  - IOI Module
- Full configuration under SW Control through hxISDE
  - Zero jumpers and switches
  - Plug-n-Play Modules
- 0.8 TMACs (hx2100 & 16 slot)
- 1.6 TMACs (hx3100 & 16 slot)

16-slot hxHADS



4-slot hxHADS



hxHADS Baseline Platform – Includes the slotted system motherboard, GPP-IO module, and hx3100 processor module

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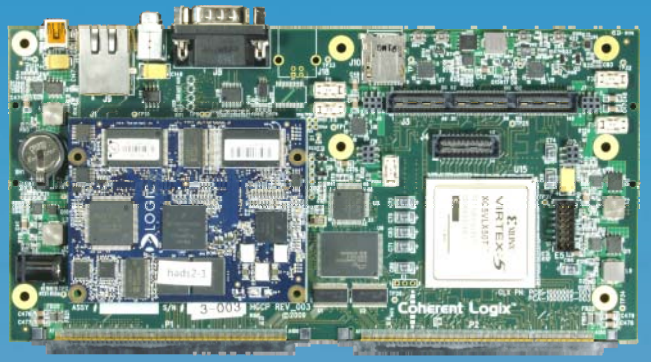
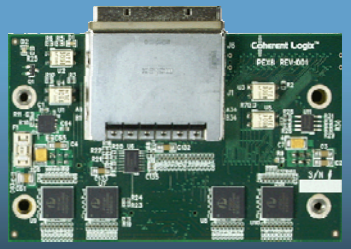
hxHADS2 Hardware

HyperX hx3100 Processor Module: Contains one or two HyperX processors connected in multi-dimensional fashion.

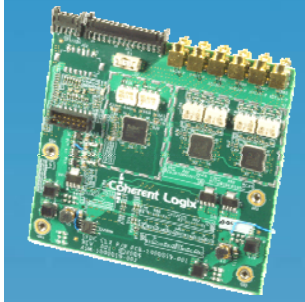


GPP-IO Module: General Purpose Processor and I/O Interface, supports off-the-shelf processor daughter cards and allows for programmable I/O interface to A/D converters, PCI express (PCIe), Gigabit Ethernet (1 GigE), USB, VGA, DVI, etc.



PEX-8 Card: PCI-Express x8 plug-in card to the GPP-IO module, enables high speed interface.

HADS2 Hardware – Con't:

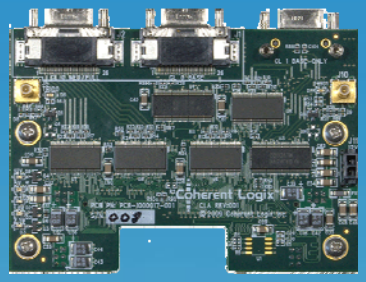


Data ConverterCard

•Two dual channel 14-bit, 150 MHz ADCs (AD9640s)
•One dual channel 14-bit, 300 MHz DAC (AD9781)
•Differential and single-ended IQ data connection to GPP-IO Module of HADS and RF Module via MCX connectors
•RF module control via I2C and SPI bus
•Supports connectivity to third-party RF Modules

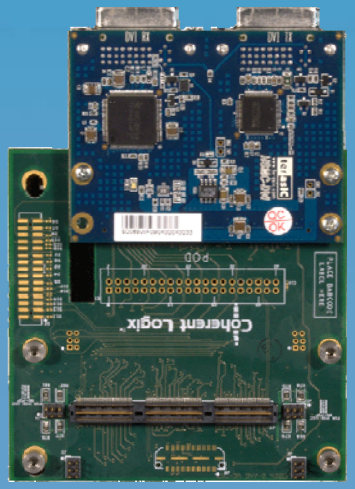
RFFront End

•RF tuning range: 100 MHz to 1 GHz; future support up to 3 GHz
•Minimum Frequency Tuning Step: 0.5 MHz
•1 dB Pass band Bandwidth: 24 MHz
•Pass band Gain Flatness: 1 dB
•RX Max Gain: 64 dB
•Gain Control Range: 75 dB
•Noise Figure: 4 dB
•Phase Noise
ol kHz: 75dBc/Hz
o10 kHz: -90 dBc/Hz
o100 kHz: -105 dBc/Hz
•Image Rejection: >80 dB
•IQ Balance: 40 dB
•External PA able to provide 20 dB additional gain



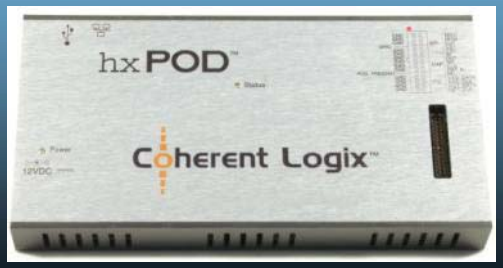
Camera LinkCard

•Two independent Camera Link channels, one Base and one Base, Medium, or Full, up to 85MHz clock
•Up to 935 Mbytes/sec. input data rate into HyperX parallel, LVDS I/O
•Flexible external trigger for each channel driven by interface FPGA / HyperX
•Serial communication to cameras via GPP or HyperX
•12 volt power available for camera



DVI Transmit / ReceiveCard

•Oneeach DVI compliant transmitter and receiver
•Supports resolutions from VGA to UXGA (25 – 165 MHz pixel rate
•Universal Graphics Controller Interface
•24 Bits/pixel color, 16.7M Colors
•Programmable I^2C interface
•3.3 V supply



hxPOD

•Emulation module for customer designed hardware

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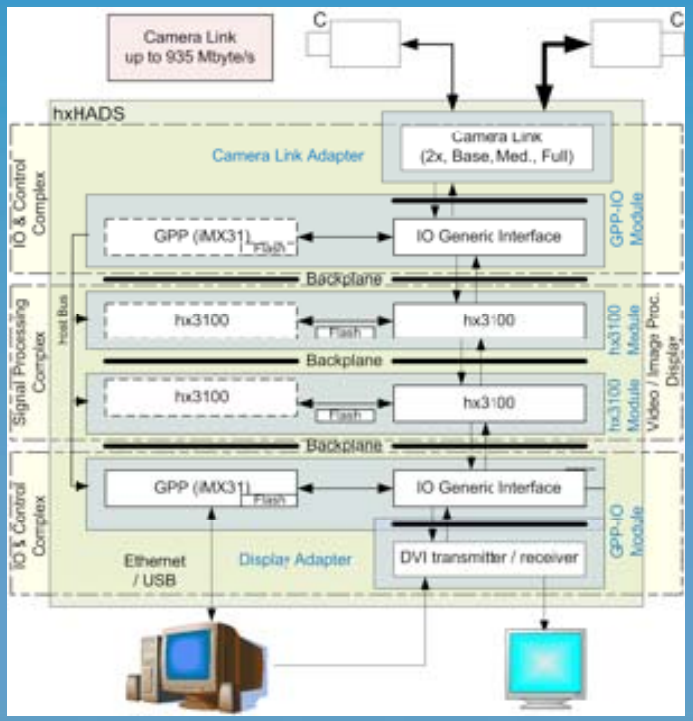
Video Applications Development System Hardware



hx3100 Module: Serving as the main building block for image and video processing, it consists of a 100 core, low power hx3100™ processor and instrumentation for measuring core power and IO power. It supports seamless extension of HyperX processor fabric via multiple hx3100 modules.

•GPP-IO Module: The GPP (General Purpose Processing)-IO Module includes the ARM based iMX31 processor, allowing applications to control system configuration options while providing direct access to the hardware through software control. The IO portion of the module supports a programmable interface to peripherals including A/D converters, Gbit Ethernet, USB, VGA, DVI, etc.

•CameraLinkCard: This module connects to hxHADS GPP-IO module as a daughter card. It hosts two independent Camera Link channels, frame trigger, and 12 volt power to cameras.

•DVI Display Card: This module connects to the hxHADS GPP-IO module and provides an interface to both DVI transmit and receive functions.

•SystemModule: As the motherboard of the system, it supports any combination of modules with plug and play capability. It exists in 4 and 16 slot configurations.

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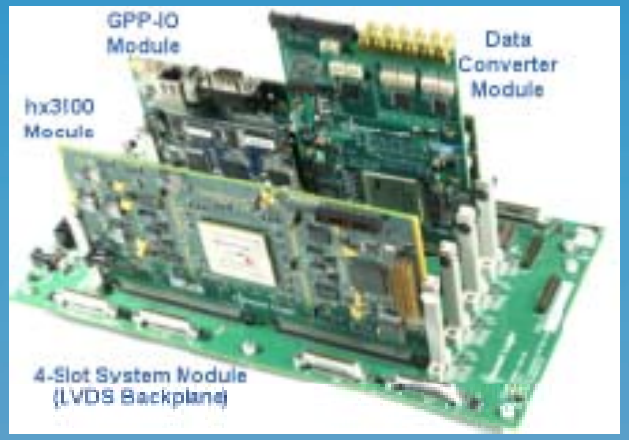
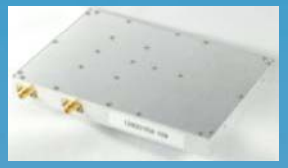
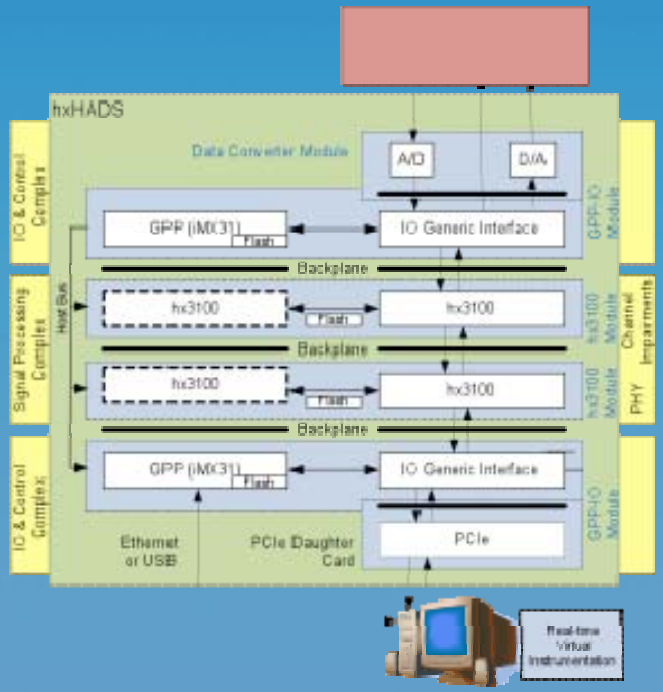
Radio Waveform Development System Hardware







- **hx3100 Module:** Serving as the main building block for waveform signal processing, it consists of a 100 core, low power hx3100™ processor and instrumentation for measuring core power and IO power. It supports seamless extension of HyperX processor fabric via multiple hx3100 modules
- **GPP-IO Module**: The GPP (General Purpose Processing)-IO Module includes the ARM based iMX31 processor, allowing applications to control system configuration options while providing direct access to the hardware through software control. The IO portion of the module supports a programmable interface to peripherals including A/D converters, Gbit Ethernet, USB, VGA, DVI, etc.
- **DataConverter Card:** This module connects to hxHADS GPP-IO module as a daughter card. It hosts two dual channel 14 bit, 150 MHz ADCs and one 14-bit 300 MHz dual channel DAC. It supports 2x2 MIMO configuration.
- **RFFront End:**This wideband tunable RF transceiver supports carrier frequencies from 100 MHz to 1 GHz in 0.5 MHz steps while providing up-down conversion from-to IF.
- **System Module:** As the motherboard of the system, it supports any combination of modules with plug and play capability in a 4 slot configuration.

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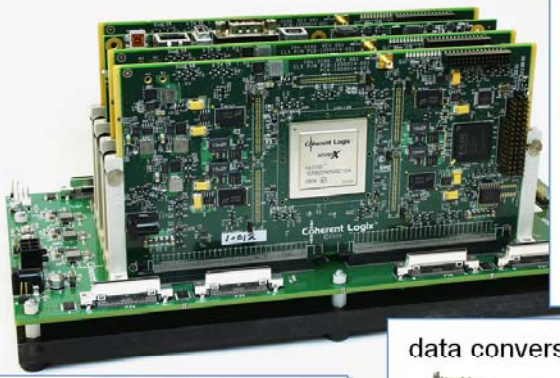
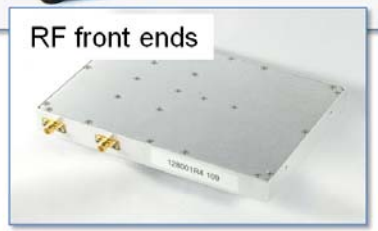
Reference System – Radio and Waveform Development System (RWDS)

hxHADS



RF front ends



data conversi

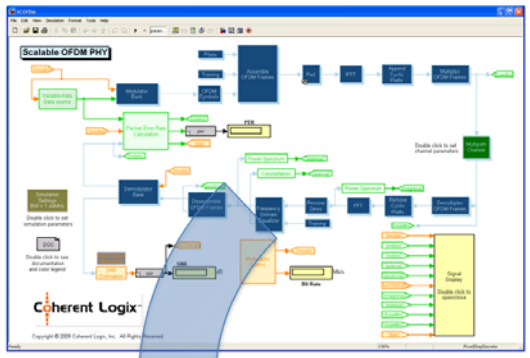
Fully modular and customizable

Plug-and-play capability with the HyperX ISDE

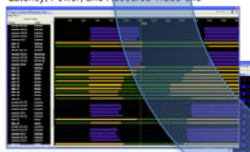
Clear path to form factor product

Supports

- PCIexpress
- Data conversion
- RF front ends

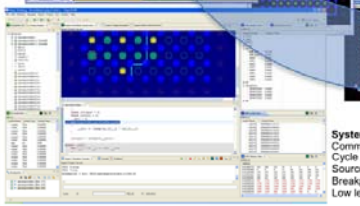


System Performance View
Task Breakdown
Critical Path Analysis
Latency, Power, and Resource Trade-offs



System Communication View
Task Activity on Hardware
Data Routing

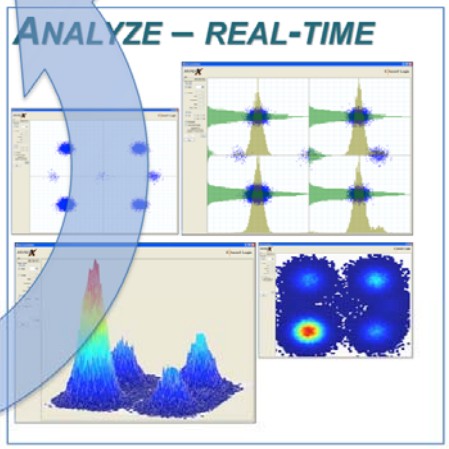
System Energy View
Resource Power
Power Optimization



System Centric View
Common Debugger
Cycle Accurate Simulator
Source Code, Variables
Breakpoint
Low level optimization

Solving the mystery of parallel programming.

- Built on proven HyperX ISDE
  - ANSI-C
  - Source code platform independent until compile time
  - > 5x reduction in development time over current (DSP/FPGA)



- Unified development and verification flow
- Design optimizations (e.g., trading performance, power, and latency) performed without changing C code

- Model based design flow

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Action Items & Next Steps

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