Space-Qualified Ultra-High Speed Plug-and-Play SERDES

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Abstract

Serializer and Deserializer (SerDes) chip sets and systems-on-chip are among the most important parts of digital processing and interconnect systems. High data rates critical for modern electronics cannot be achieved without development of advanced SerDes products. Apart from high data rate and low power consumption, the new parts for space applications need to demonstrate a high level of adaptation to different operational requirements and tolerance to harsh external conditions. Internal reconfiguration process must be either automatic or externally controllable through standard digital interfaces in order to satisfy Plug-and-Play requirements. Development of such parts requires utilization of advanced design techniques and fabrication technologies.

This paper presents a design concept for an ultra-high speed SerDes that satisfies all of the above requirements. This chipset is an upgrade of the previously developed Space-qualified digital SerDes that is based on a unique silicon-verified library of radiation-hard cells and functional blocks designed within a commercial SiGe BiCMOS technology. The high tolerance of this library to total ionizing dose (TID) and latch-up conditions has been proven by a set of tests performed on several parts developed within this library. New improved functional blocks have been added to the original SerDes design in order to support such important features as high-speed data-to-clock alignment, low-speed data drift accommodation, high-speed input duty cycle control and adjustment, high-speed output amplitude adjustment, and possibility of external synchronization of multiple similar parts.

All additional blocks have been verified through fabrication within other products and can be inserted into the new SerDes with minor insignificant adjustments. The presented chipset is currently in the final stage of design process and is planned for fabrication in 2011. Application of this chipset will not only improve the performance and reliability of space-oriented electronics, but will also support a true Plug-and-Play functionality of the corresponding systems.

I. Introduction

Serializers and Deserializers (SerDes) are complex mixed-signal devices that convert low-speed parallel digital data into high-speed serial data streams, and back. They can be designed as chipsets including two separate devices, or as systems-on-chip that combine both functions in one integrated circuit (IC). SerDes ICs are among the most important parts of modern digital processing and interconnect systems where they create an interface between front-end electronics (opto-electrical and electro-optical converters, analog-to-digital converters, etc.) and digital signal processors usually implemented as field-programmable gate arrays (FPGA). SerDes devices operate in two significantly different frequency domains, which makes their optimization not straight forward. Their parameters, such as maximum serial data rate and total power consumption, often define the performance characteristics of a complete system. The demand for higher data rates in modern processing and communication systems cannot be satisfied without development of advanced SerDes products. Apart from high data rate and low power consumption, the SerDes parts for space applications need to demonstrate a high level of adaptation to different operational requirements and tolerance to harsh external conditions. Those

conditions include high total ionizing doses (TID) or radiation and presence of energetic particles that cause various single-event effects (SEE). Adaptation is achieved through reconfiguration of SerDes internal structure. The reconfiguration process must be either automatic or externally controllable through standard digital interfaces in order to satisfy Plug-and-Play requirements.

Development of such parts requires utilization of advanced design techniques and fabrication technologies. While low-speed circuitry with frequencies up to several *GHz* can be designed in the standard single-ended CMOS architecture, the high-speed blocks with frequencies in excess of 10*GHz* can be more optimally implemented in differential current-mode logic (CML). CML cells utilize hetero-junction bipolar transistors (HBTs) as active components and operate as tail current switches exhibiting very high switching speeds or low power consumption at average speeds. Differential signaling makes them more tolerant to a noisy and radiation high environment and provides aligned positive and negative pulses with a 50% duty cycle, which are hard to achieve in CMOS logic. Emitter followers used as buffers significantly increase the capacitive load driving capabilities of the cells. CML logic is also inherently suitable for the implementation of complex logic functions as can be seen in Fig. 1

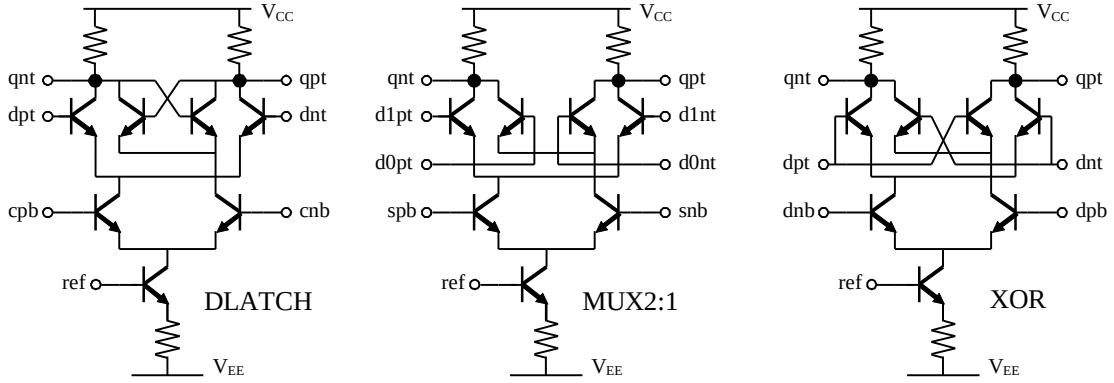


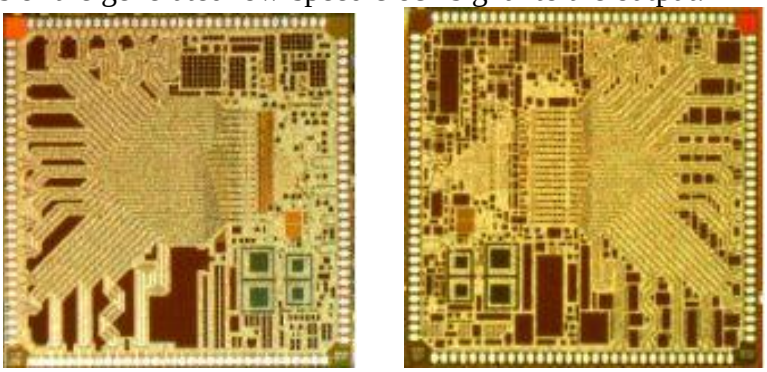
Fig. 1. Two-level CML Cells.

HBTs can operate in a wide temperature range extending to extra-low temperatures [1-3] and are inherently tolerant to TID and latch-up conditions [4-6], which makes such circuits ideally suitable for space applications.

The Advanced Science and Novel Technology company (ADSANTEC) has successfully developed a SerDes chip set based on the company's proprietary CML library for the SiGe120 technology from Tower/Jazz. The parts have been tested for functionality and radiation hardness. Based on the successful test results, they have been qualified for space applications and selected by NASA for the utilization within the payload of LADEE mission scheduled for 2011.

The serializer IC shown in Fig. 2a includes a 16-to-1 multiplexer with a proprietary LVDS-compatible low-speed clock and parallel data input interface and CML-compatible high-speed clock and serial data output interface, a timing block with selectable clock

division or clock multiplication operational modes, and a clock processor that delivers different phases of the generated low-speed clock signal to the output.



a. b.

Fig. 2. Microphotographs of Serializer (a), and Deserializer (b)

The universal clock and data input buffers (UIB) can accept differential signals with any common-mode voltage between negative and positive supply rails [7]. The performance of the buffer shown in Fig. 3 has been demonstrated by a test chip fabricated in the same technology.

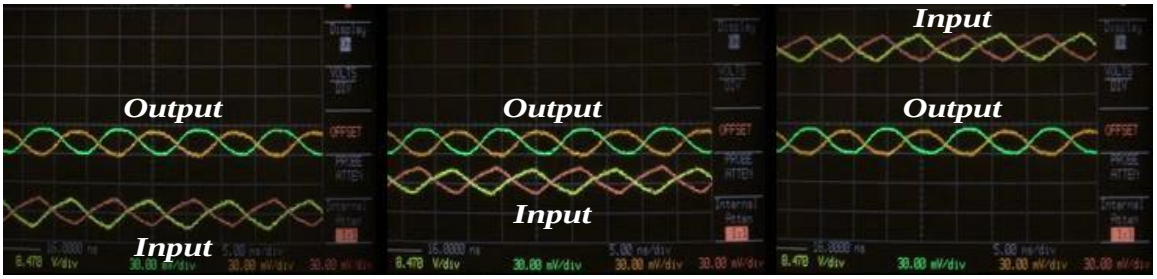


Fig. 3. UIB Performance at Different Input Common-Mode Voltages.

The deserializer IC shown in Fig. 2b includes a 1-to-16 demultiplexer with a proprietary LVDS-compatible low-power clock and parallel data output interface [8] and CML-compatible high-speed clock and serial data input interface, a selectable clock and data recovery (CDR) block, and a clock processor that delivers different phases of the generated low-speed clock signal to the output. The performance of the true LVDS output buffer with a current consumption below 6*mA* is illustrated in Fig. 4.

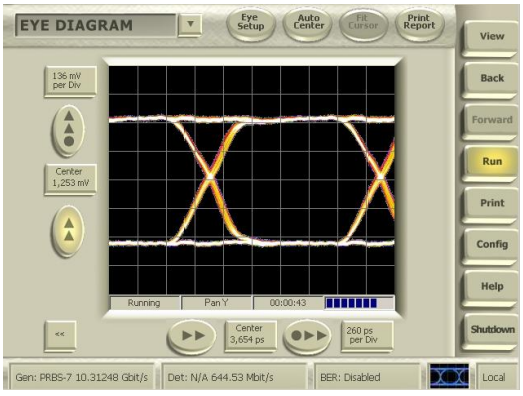


Fig. 4. LVDS Output Buffer Eye at 645Mb/s.

II. Improved Serializer Design Concept

The serializer described above was used for the design of an improved device version with additional functions, such as low-speed data drift accommodation, high-speed output amplitude adjustment, and possibility of external synchronization of multiple parallel serializers. Implementation of those functions requires insertion of new blocks that are marked by yellow shading in Fig. 5 in addition to the blocks of initial design that are marked by grey shading.

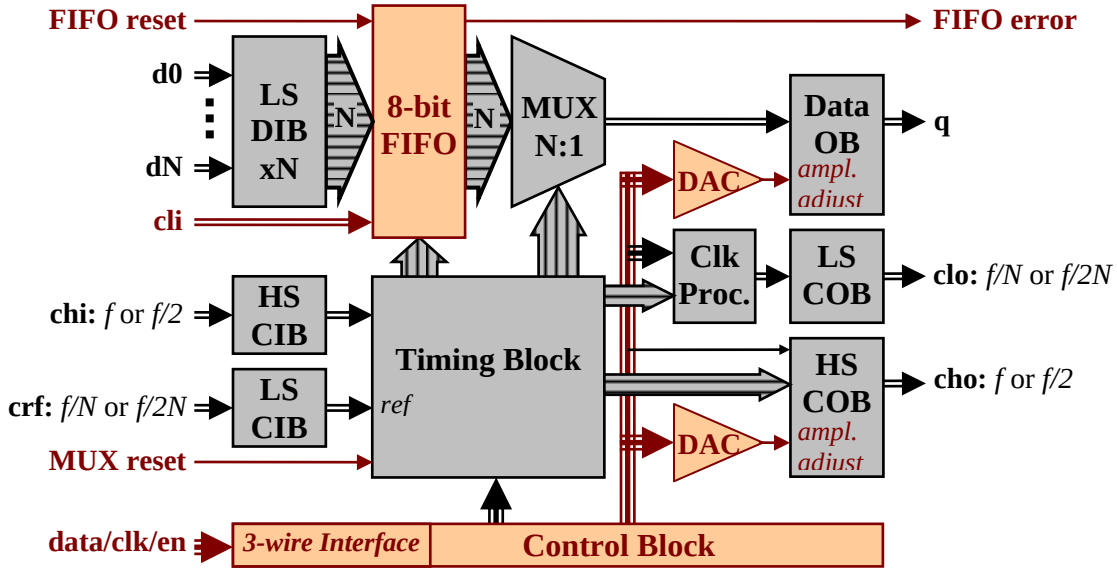


Fig. 5. Serializer Block Diagram.

The initial blocks include the multiplexer N-to-1 (MUX N:1), the low-speed N-bit wide parallel data input interface (LS DIB xN), the high-speed clock input buffer (HS CIB), the low-speed reference clock input buffer (LS CIB), the Timing Block, the serial data output buffer (Data OB), the clock processor (Clk Proc.), the low-speed clock output buffer (LS COB), and the high-speed clock output buffer (HS COB). The initial control functions include: frequency selection for high-speed clock input "chi" and low-speed reference clock "crf", frequency selection for high-speed clock output "cho", and frequency and phase selection for low-speed clock output "clo". All those functions were activated by external binary control signals.

The improved version of the chip includes input parallel 8-bit deep FIFO for the input data realignment from input low-speed clock "cli" to internal clock of the same frequency *f/N*. The FIFO generates "FIFO error" binary signal in case of underflow or overflow and can be re-centered by external "FIFO reset" binary signal.

Amplitude adjustment functions under control of low-speed digital-to-analog converters (DAC) have been added to Data OB and HS COB. Both initial and new digital control signals are now generated by internal Control Block with a standard 3-wire interface.

Operation of the serializer can be synchronized through the reset of the Timing Block by means of additional binary signal “MUX reset”.

All new blocks are designed in the same CML library and have been silicon-verified within different test chips and commercial products developed by ADSANTEC.

As can be seen, the designed serializer can be adapted to multiple operational conditions including different clock frequencies and amplitudes, as well as clock-to-data phase variation. The reconfiguration can be performed through the standard serial interface. The device can be easily integrated into more complex systems due to the possibility of external synchronization.

III. Improved Deserializer Design Concept

The deserializer described in Section I was used for the design of an improved device version with additional functions, such as high-speed data input threshold adjustment, high-speed input clock duty cycle control and adjustment, high-speed output amplitude adjustment, manual or automatic high-speed clock-to-data alignment, and possibility of external synchronization of multiple parallel serializers. Implementation of those functions requires insertion of new blocks that are marked by yellow shading in Fig. 6 in addition to the blocks of initial design that are marked by grey shading.

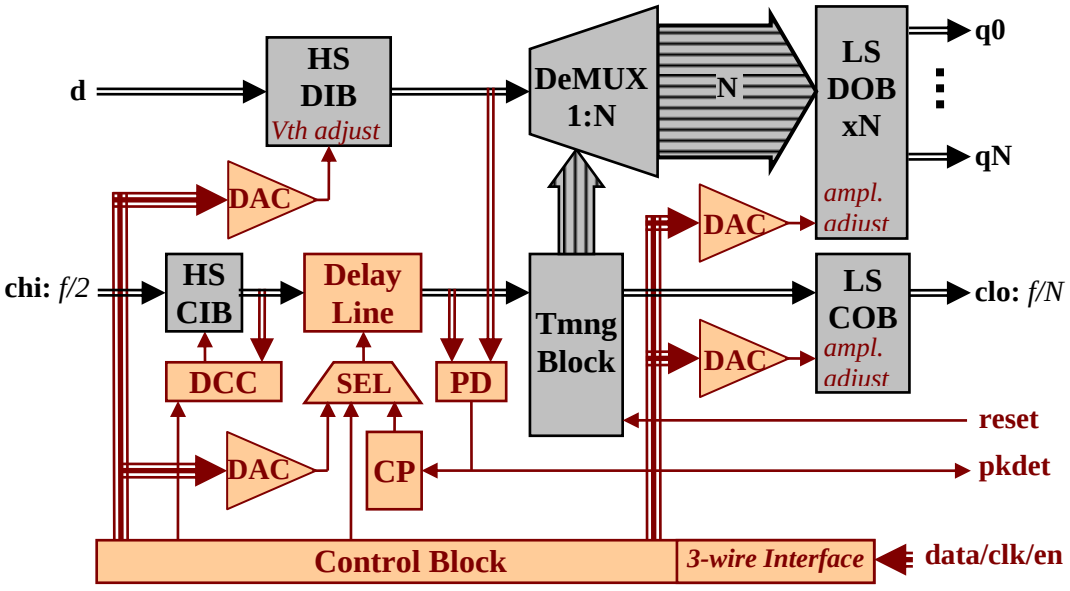


Fig. 6. Deserializer Block Diagram.

The initial blocks include the demultiplexer 1-to-N (DeMUX 1:N), the serial data input buffer (HS DIB), the high-speed clock input buffer (HS CIB), the low-speed N-bit wide parallel data output interface (LS DOB xN), the low-speed clock output buffer (LS COB), and the timing block (Tmng Block).

The improved version of the chip incorporates a selectable automatic duty cycle control for half-rate input clock “chi”. A threshold voltage adjust (Vth adjust) function has been utilized in HS DIB for correct detection of serial data bits (“d”) in single-ended mode.

Amplitude adjustment functions under control of low-speed DACs have been added to LS DOB and LS COB. All digital control signals are generated by internal Control Block with a standard 3-wire interface.

For correct sampling of the input data, a delay-locked loop (DLL) has been implemented in the chip. It includes a phase detector (PD) that generates an analog voltage proportional to clock-to-data phase error, a charge pump with internal integrator (CP), and a proprietary variable Delay Line that can be controlled either by the CP output signal or from Control Block. Similar delay lines are used in multiple commercial products developed by ADSANTEC.

Operation of the deserializer can be synchronized through the reset of the Timing Block by means of additional binary signal "reset".

All new blocks are designed in the same CML library and have been silicon-verified within different test chips and commercial products developed by ADSANTEC.

As can be seen, the designed deserializer can be adapted to multiple operational conditions including differential or single-ended input data modes, duty cycle distortion of the input clock signal, different clock and data output amplitudes, as well as unpredictable input clock-to-data phase variation. The reconfiguration can be performed through the standard serial interface. The device can be easily integrated into more complex systems due to the possibility of external synchronization.

IV. Conclusions

The presented design concepts offer a significant improvement of the existing space-qualified SerDes chipset. The implemented additional functions allow for a more reliable data transfer through the serial interface within different operational conditions. This is achieved by FIFO block in the serializer and DLL in the deserializer, as well as control and adjustment of frequency, phase, amplitude, and duty cycle of appropriate clock and data signals.

Both devices are suitable for Plug-and-Play operation due to insertion of standard serial interfaces that control internal DAC blocks.

The new designs are based on the existing silicon-verified blocks from the company's proprietary radiation-hard CML library, which guarantees their correct functionality and high tolerance to harsh environmental conditions associated with space missions.

V. References

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