Fault Tolerant Computing in Space-Based Reconfigurable Systems at Los Alamos

Heather Quinn
Los Alamos National Laboratory

Paul Graham, Keith Morgan, Michael Caffrey, Jim Krone, James Moore
ISR-3, Space Data Systems Los Alamos National Laboratory

Michael Wirthlin, Brian Pratt, Kevin Lundgreen
Electrical and Computer Engineering Department
Brigham Young University

Introduction

- The LANL Approach
  - Rapid Static Testing
  - Multi-Tiered Application Testing
  - Low Cost Mitigation Schemes
- Future Challenges/Directions

The LANL Approach:

Advantages

- Experimental satellites allow us to do research on
  - Static and application testing approaches
  - Mitigation approaches
  - On-Orbit testing
- New approaches to risk assessment
  - COTS parts vs. mil/aero parts
  - Full mitigation vs. partial mitigation
- Several of us are FPGA researchers and tool designers
  - Originally, outsiders in the radiation community
  - Allow us to leverage what we know about the devices

The LANL Approach:

Disadvantages or Advantages?

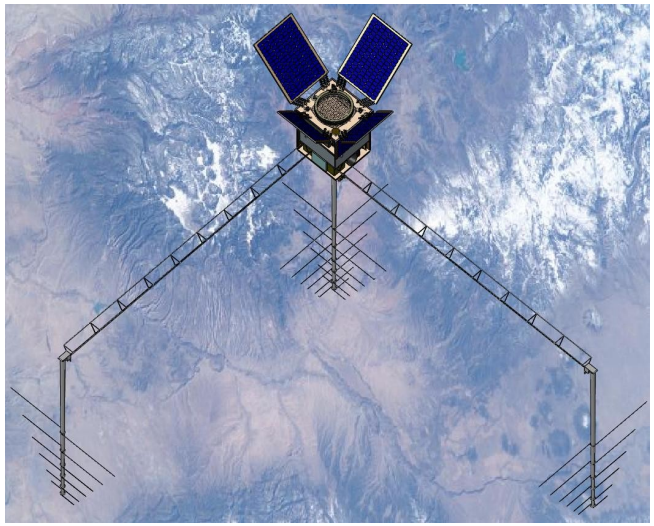
- Operating in a vacuum from other radiation researchers
  - Far ahead in some areas (MBUs, angles)
  - Far behind in others (SEL, Prompt, SET)
- Shoestring budget
  - Specialize in Xilinx devices
  - New approaches to testing to overcome budget issues
  - Interesting hardware test fixtures, beefy software analysis
- Extensive collaboration to push program goals forward
  - Aerospace, XRTC and GSFC for beam time
  - GSFC, JPL, Aerospace for physicists and statisticians
  - GSFC and Vandy for simulation

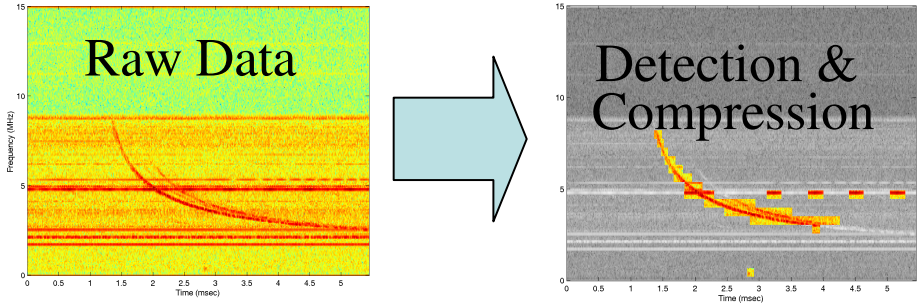
Cibola Flight Experiment (CFE):

A First Attempt

- The little satellite that could:
  - Started in 1998 as an experimental payload...
  - ...Then it became two payloads
  - ...Then it became an entire satellite
  - Launching in the next month
- Based on Virtex-I technology
- Small team of researchers and implementors

Fast On-board Processor with COTS FPGAs





- Description:
  - Software Radio:
    - Four channels, 20 MHz bandwidth each
    - Tunable from 100 to 500 MHz,
    - 300 Gop/sec Re-Configurable Computer (RCC)
    - 4-element antenna array
- Objectives:
  - Demonstrate responsive, flexible, multi-mission RF payload with continuous data processing
    - Detect, geolocate, characterize VHF/UHF EMP & lightning signals
    - Compression & immediate distribution of data products
    - Adaptability: Re-configurable on-orbit
  - Validate LANL developed SEU mitigation techniques enabling use of COTS parts

MRM:

On-Orbit Radiation Testing

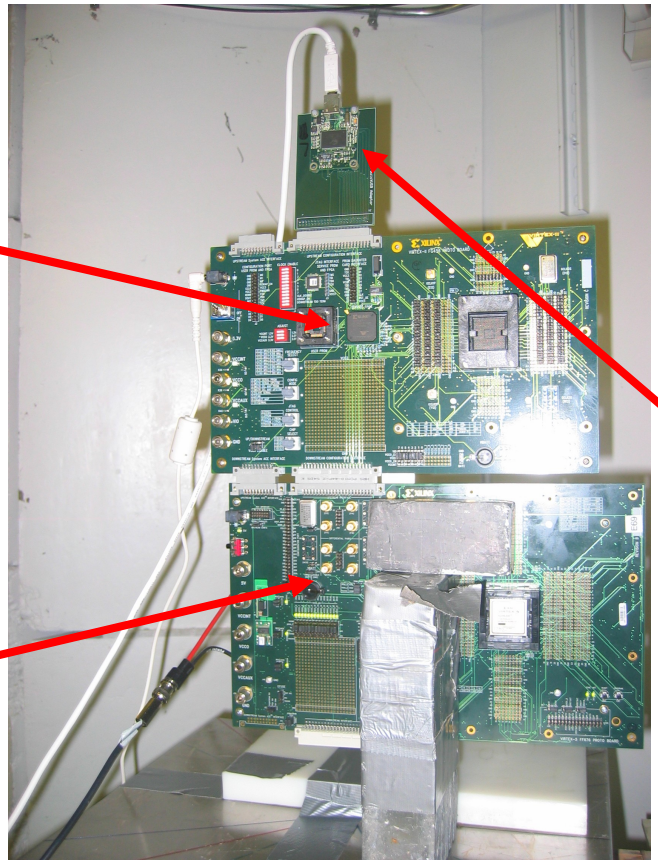
- Latest small satellite
- Paid for by DoE and DoD funding
  - Clients are tired of paying for ground-based testing and having failures
  - Essential testing of device pre-launch (SEL, SEU)
  - On-orbit testing of COTS parts
  - Piggy-backing off of the NextGen chassis

Rapid Static Testing

- Minimize beam time by rapidly obtaining sample data
- Simple static test fixture
  - Commercially available hardware
  - Custom software
  - Easily redeployed to newer devices (1 week at NSREC for the V5)
  - Can hack into a low data rate fault injector and a dynamic test fixture
- Data analysis done off line

Virtex-5 Hardware Test Fixture

Virtex-II AFX Board



USB 2.0 Interface to Linux PC

Virtex-5 AFX Board

Software Test Fixture

- Text-based interface
  - SSH'd into the test machine
  - Instant access to incremental readback results
  - Easily translates to new tests that fit our test methodology
- Constantly readbacks and reconfigures device
  - Saves differential bitstream for upsets
  - Minimimal statistics (simple MBU and std deviation calcs)
  - Collect 1-5 differential bitstreams per second
  - Reconfigures with “partial” bitstream

Post-Test Data Analysis

- Remove the obvious SEFIs on the first pass
- Tally events by size, resource, bitflip, shape
  - Cluster upsets into 1-bit and MBU events
  - Remove suspiciously large MBUs
  - Coorelate upset location to resource
  - Determine if MBUs are spanning multiple resources
- Uniformity of upsets based on (x,y), (r,c)
- Outputs results to excel spreadsheets

Multi-Tiered Dynamic Application Test Approach

- Beam time is
  - Expensive,
  - Statistical
  - Too late
- Start analyzing/testing for SEUs during the design phase
  - Fault modeling through formal methods
  - Fault injection
- Go into the beam to validate results

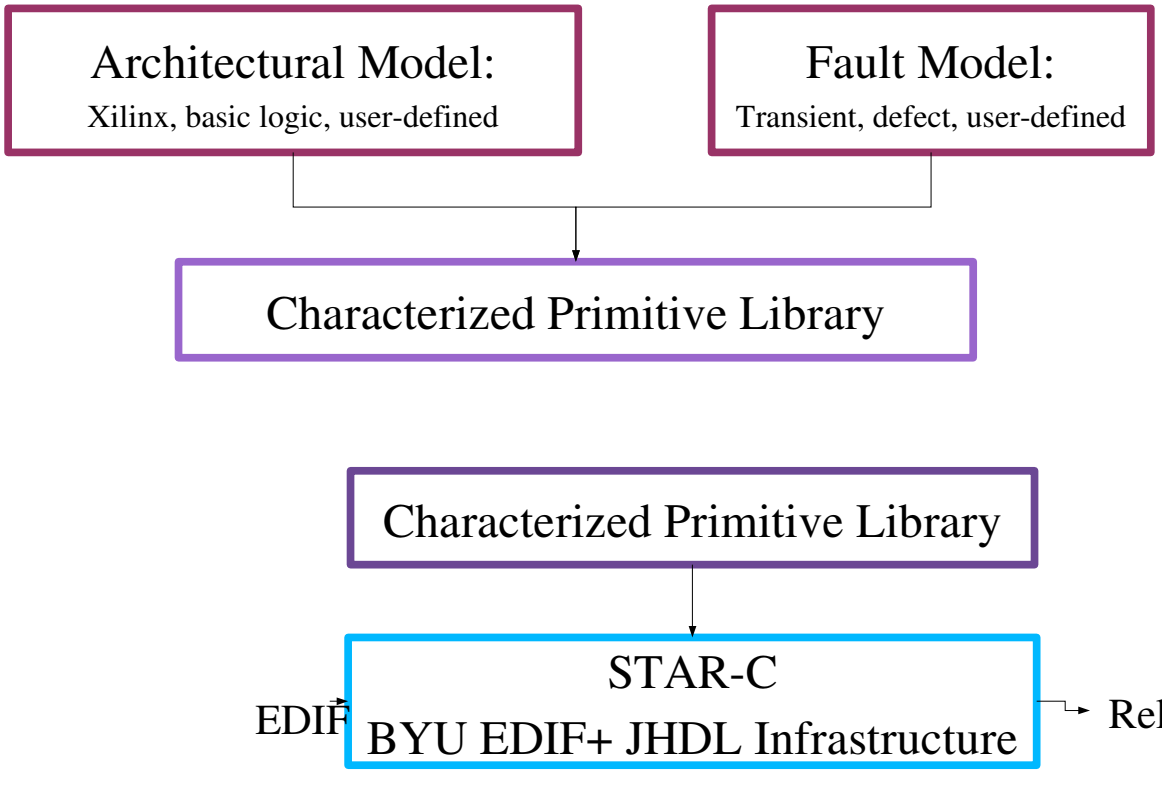
Scalable Tool for the Analysis of Reliable Circuits (STAR-C)

- Motivation: provide tools to system and circuit designers to quickly analyze reliability
  - Works with CAD design flow
  - Scales to realistic circuit size
  - Is extensible
  - Easier to use than traditional reliability analysis tools
- STAR-C Tool: determine unprotected cross-section or probability of failure

STAR-C:

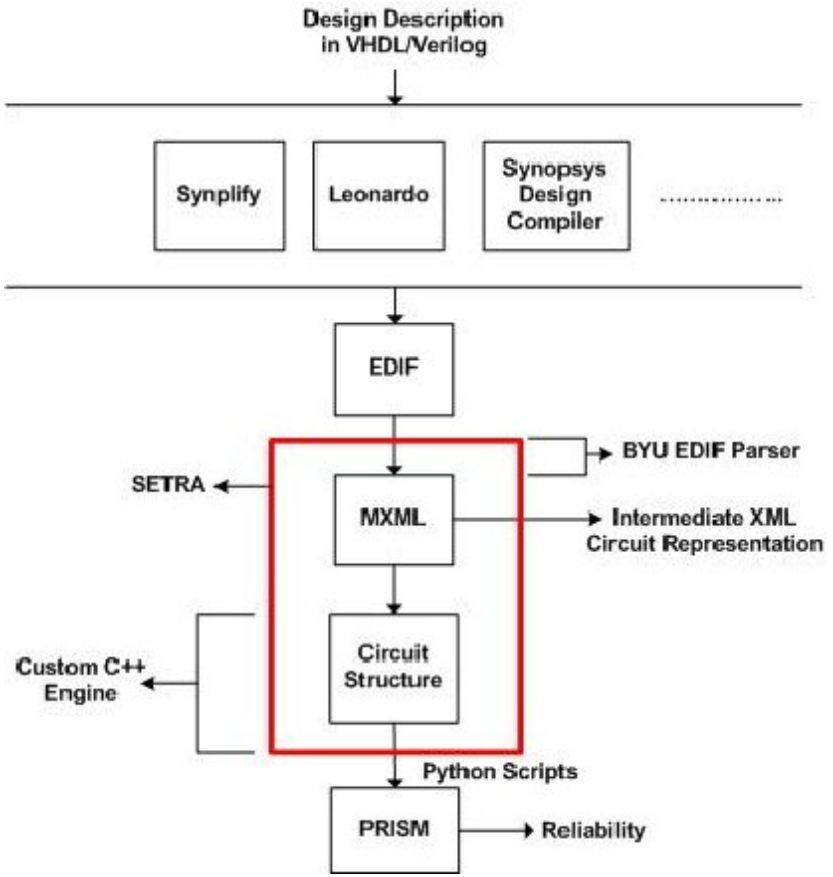
Reliability Analysis within the Design Flow

- No input models or vectors
  - Analysis based on EDIF output from CAD tools
  - No compensating failures
- Reliability defined through the architectural and fault models
- 50% agreement with fault injection
  - Routing network currently not implemented



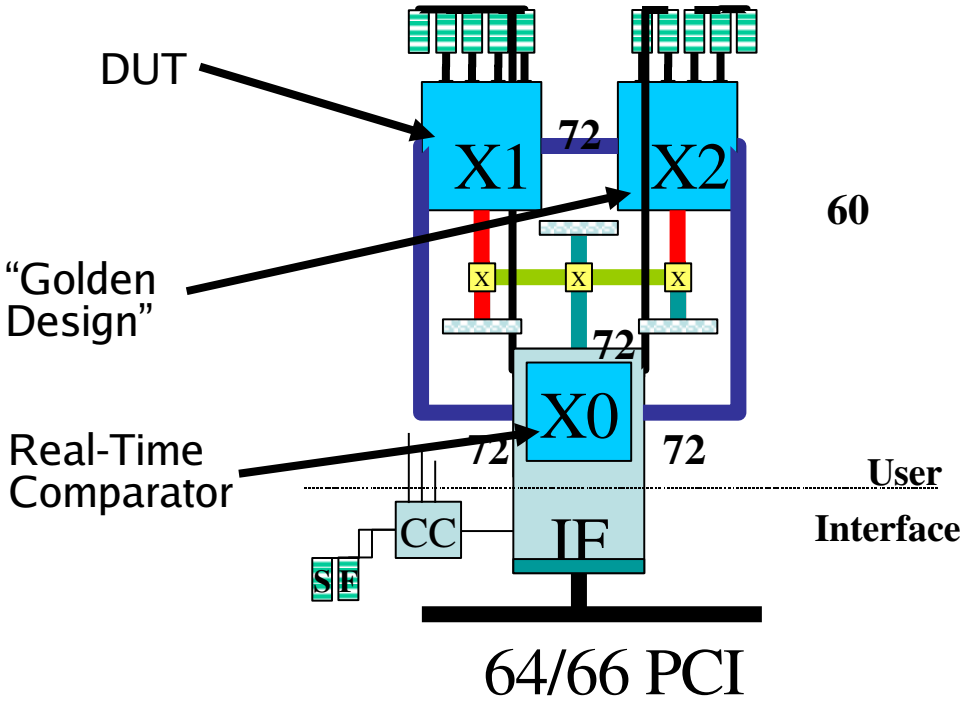
Scalable Extensible Tool for Reliability Analysis (SETRA)

- Probabilistic model checking techniques for evaluating reliability
  - Models are evaluated incrementally to make scalable
  - Handles logic masking of faults
  - Handles redundancy
- Retargetable to new device technologies through library approach
- Can handle EDIF netlists (extensible to other formats)



Bitstream SEU Emulation

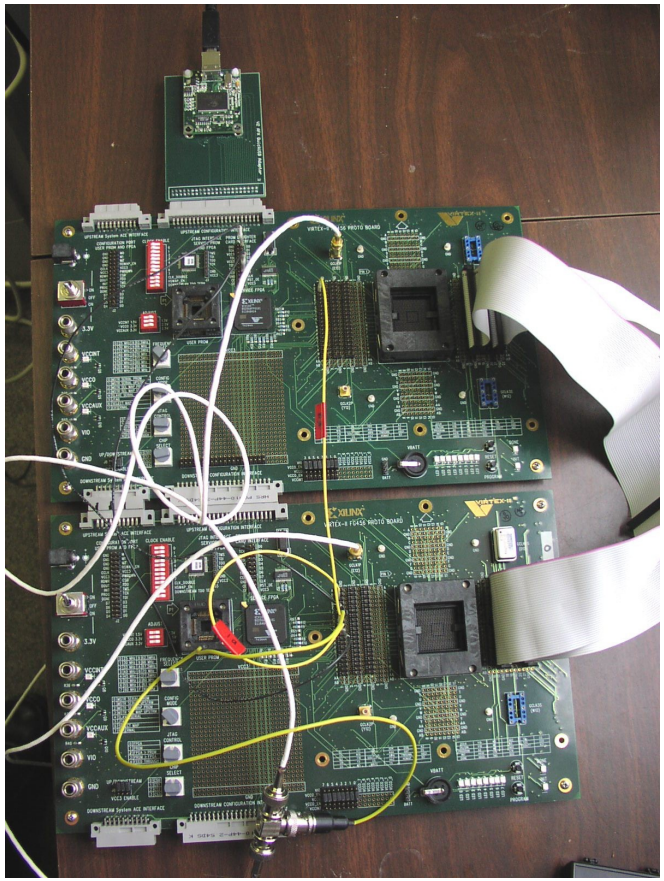
- Emulate configuration memory SEUs dynamically by *inserting* errors into the configuration bitstream
  - Toggle configuration bit within the bitstream
  - Watch the circuit to identify circuit failure
  - Repair configuration bitstream
  - Repeat for *all* or *random* configuration bits
- Injects both single-bit and multi-bit errors



Virtex SEU Emulator (LANL/BYU)

Benefits to the Multi-tiered Approach

- Accelerators: one app, 2 upsets/sec, Davis
  - V1000: 33.5 days, $403,000
  - 2V250: 11 days, $132,000
  - 4VSX35: 69 days, $828,000
  - 5VLX50: 86 days, $1,032,000
- SEU Emulators: one application
  - Cost: $6-12,000 (Boards and PC)
  - Time: .5-3 hours/run, multiple runs
  - >90% agreement with proton tests
- STAR-C/SETRA: one design
  - Cost: PC, no boards
  - Time: minutes-hour



Virtex-II SEU Emulator

On-Going Research

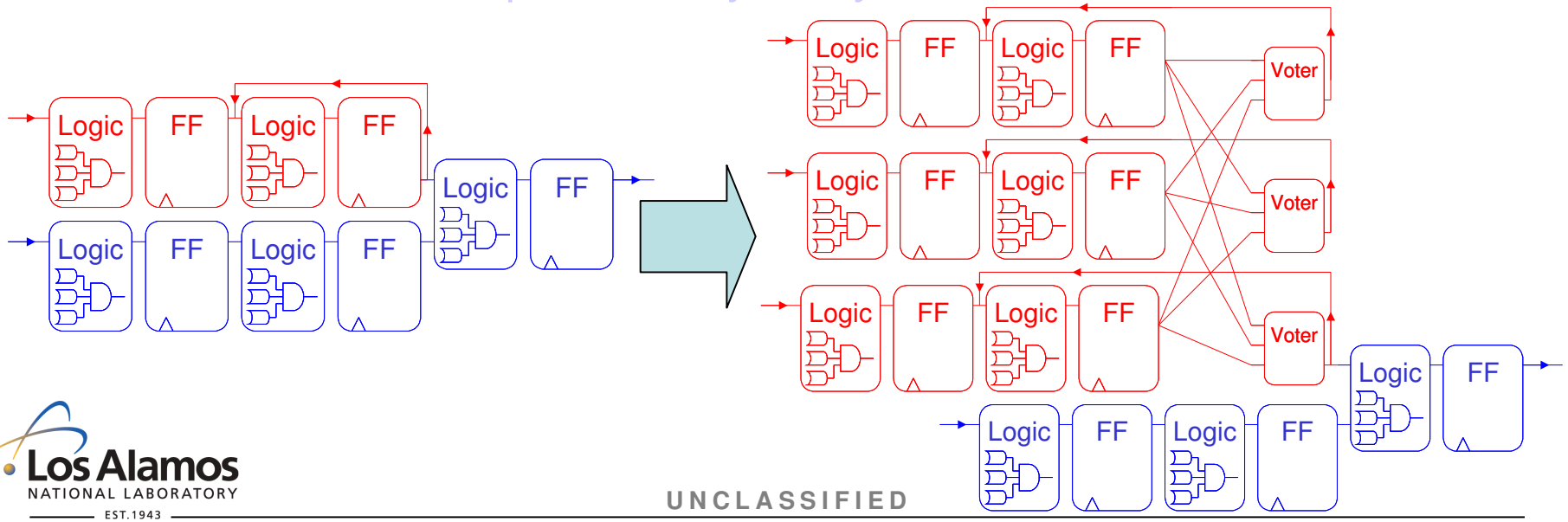
- A lot of active research in these tools, saving beam fees
- Fault injection
  - Recently expanded to test failures in full TMR
  - Need to expand to deal with robustness of multi-bit errors in newest Xilinx devices
    - MBUs make fault injection intractable
- STAR-C/SETRA
  - Needs routing network estimators
  - Needs to estimate complete TMR vulnerabilities in a full TMR-protected design

Mitigation Approaches:

Partial TMR

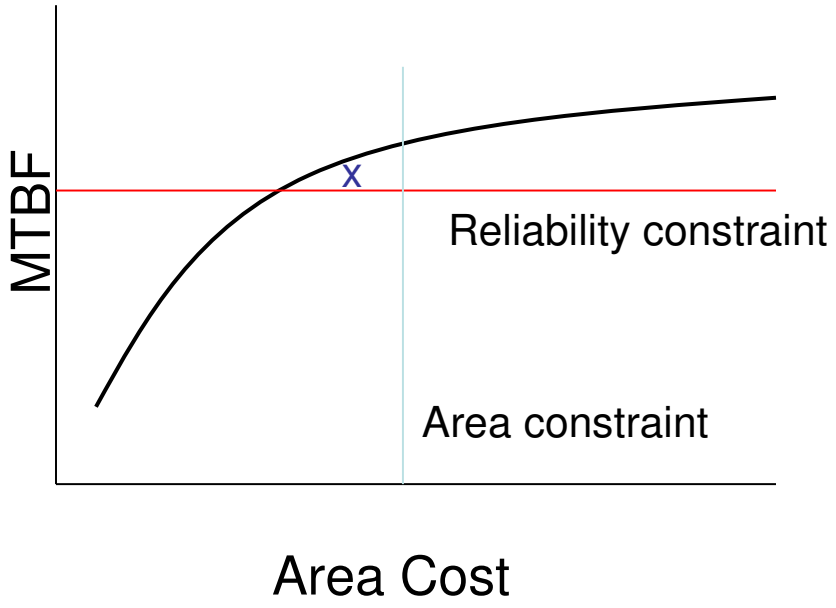
Automatic reliability improvement (mitigation)

- BYU-LANL BLTMR
  - Automated TMR tool
  - “Selectable” reliability and availability
  - Information at http://reliability.ee.byu.edu



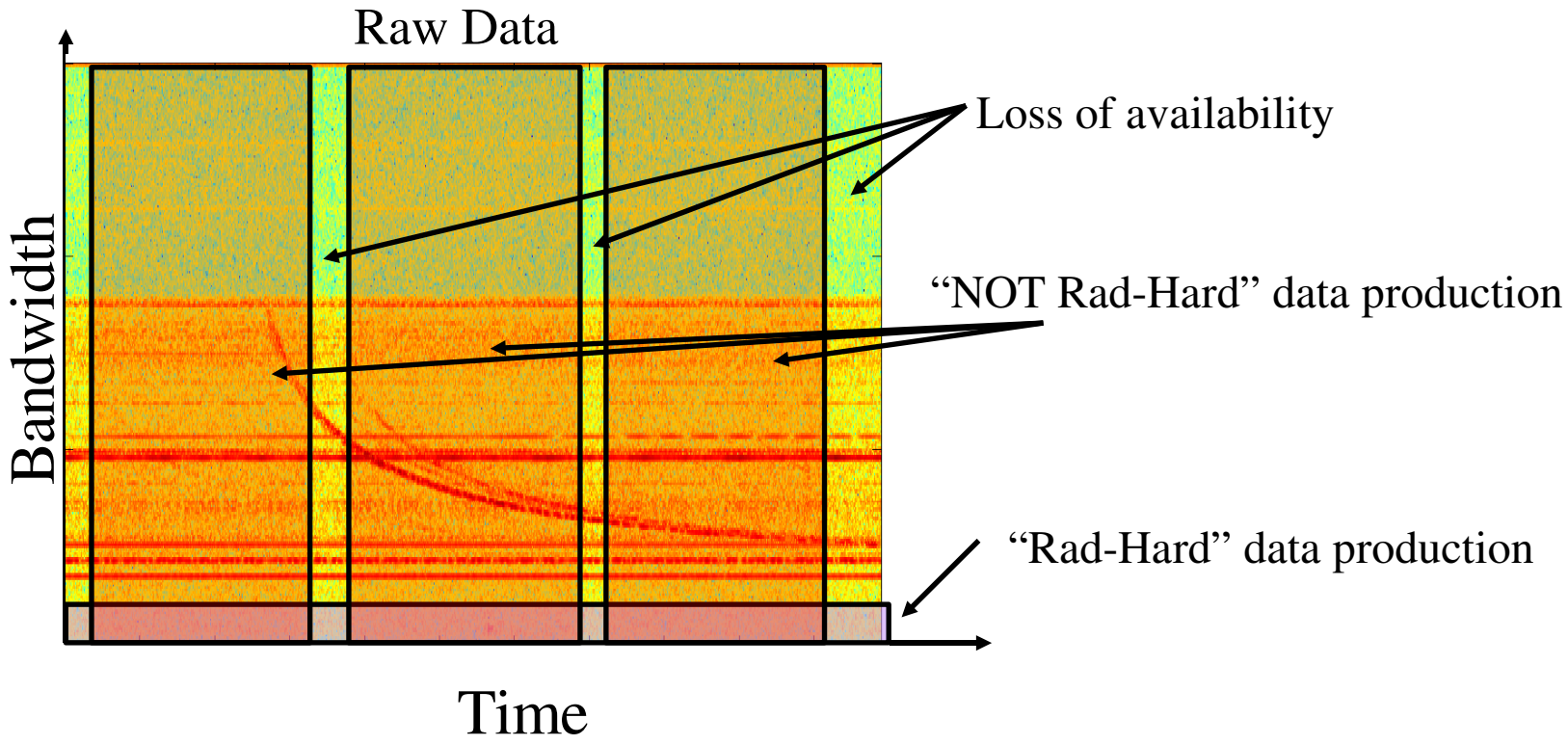
Motivation for Partial TMR

- Factors of fault-tolerant computing:
  - Availability
  - Reliability
  - Mitigation Cost
- Full TMR
  - Expensive in terms of power, speed, area, etc.
  - Worthwhile if affordable!



Advantages/Disadvantages of Partial TMR

Lower cost / bit



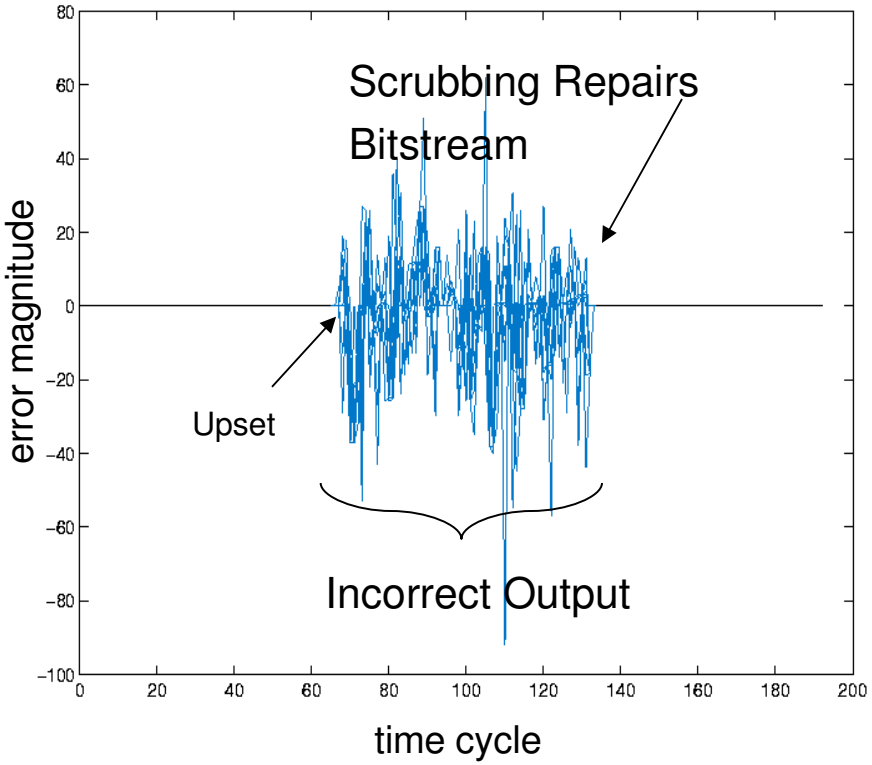
Downsides:

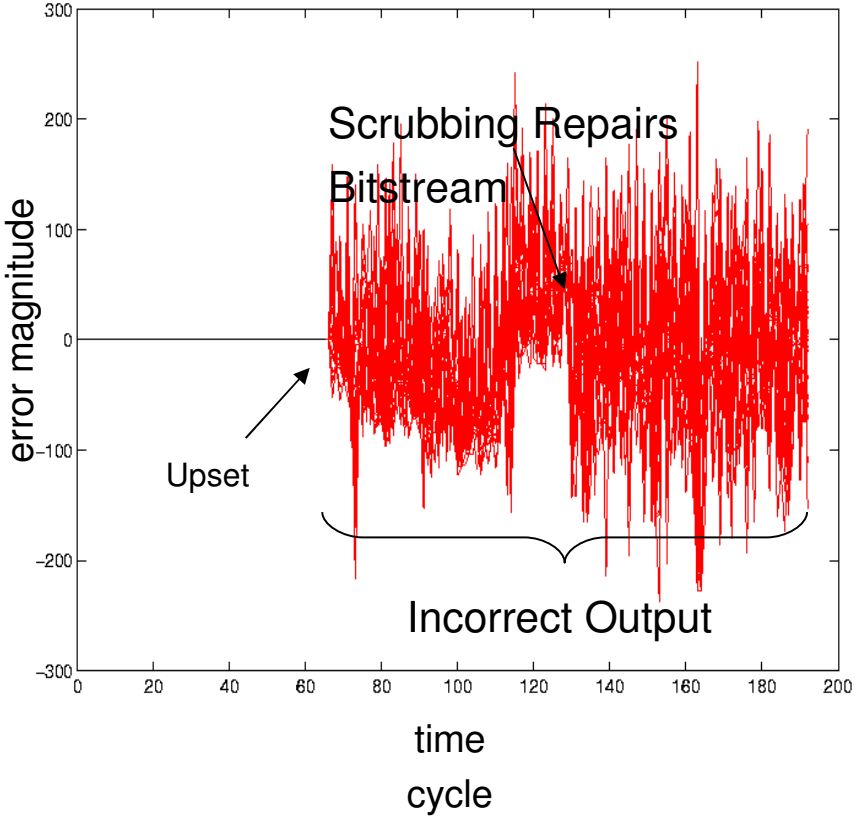
loss of predictability, complexity, assurance, future screened part inventory

On-Orbit Mitigation Concerns:

Persistent Errors

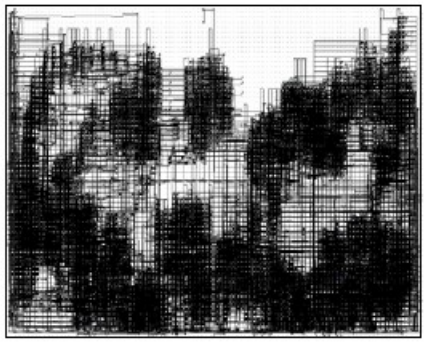
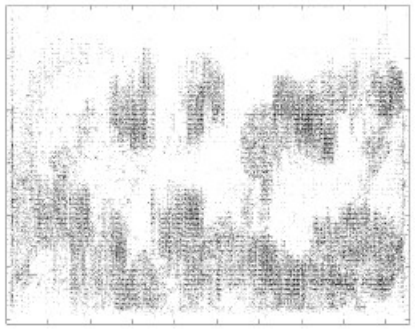
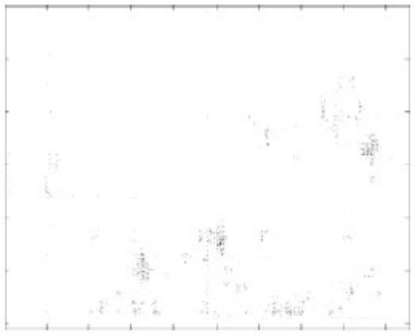
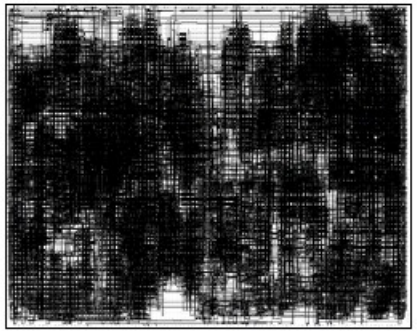
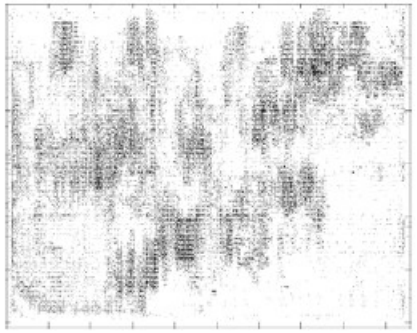
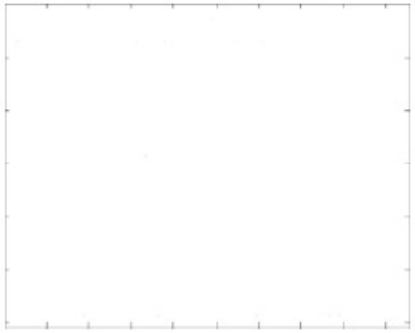
DSP Circuit Difference





Error = delta between outputs of a golden and DUT circuit

Proton Saturation Cross-Section Map

	FPGA Editor Layout	Dynamic X-section	Persistent X-section
Unmitigated			
	5,746 slices (46%)	1.29×10^{-8} cm^2	3.1×10^{-10} cm^2
Partial TMR applied to Feedback & Input to FB			
	8,036 slices (65%)	1.27×10^{-8} cm^2	3.4×10^{-12} cm^2

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Future Concerns/Directions (1 of 4)

- Multiple-bit upsets:
  - Very robust data set in newest devices
  - Hard to protect against
  - Can defeat TMR
  - New mitigation techniques? Or leverage partial TMR? Improve the floorplanning?
- Testing concerns:
  - 65-nm are showing the cracks in the RPP model
  - Angular testing is necessary, on-orbit radiation is isotropic
  - LET “boosting” from angular testing needs to be studied

Future Concerns/Directions (2 of 4)

- Mitigation concerns:
  - Is there something better than TMR?
  - BYU/LANL project recently determined that TMR really is the best
    - Quadded logic, ECC, and temporal redundancy less reliable than unprotected circuit
    - TMR the extra sensitive area is larger than TMR-protected circuit
  - Bit interleaving not helpful
    - MBUs are big, 2D: interleave 5 rows and 5 columns?
    - Is it better to lose a one redundant copy or little pieces of each one?

Future Concerns/Directions (3 of 4)

- Power vs. Area vs. Speed vs. TMR vs. MBUs
  - TMR is power hungry, space hungry, and slow
  - Tools will help you make timing, make place and route, optimize your power...at a price:
    - Wire is expensive (timing, spacing, power)
    - Shorten all of the routes to make time, area, power constraints
    - Wire is essential, spacing is essential to combat MBUs
    - Do you want to be fast or do you want to be correct?
  - Partial TMR might be helpful – get back space, speed, power to disentangle these issues

Future Concerns/Directions (4 of 4)

- On-Orbit Testing
  - Is is possible to accurately determine cross-sections while on-orbit?
  - Is it possible that on-orbit testing is more accurate for very high LETs and angular effects?
  - Can we save money by sending up experimental satellites instead of extensive accelerator testing?
- Low Cost Space-based Radiation Detection
  - Newest Xilinx devices are very soft with strong angular effects
  - Can we use the FPGA as both a processing tool and a radiation detector?