

**NEPP Electronic Technology Workshop**  
**June 22-24, 2010**

National Aeronautics  
and Space Administration



# **Evaluation of COTS SiGe, SOI, & Mixed Signal Electronic Parts for Extreme Temperature Use in NASA Missions**

**Richard L. Patterson**  
**NASA Glenn Research Center**

**Ahmad Hammoud**  
**ASRC Aerospace Corporation**



# Introduction

- ***Brief description of NEPP Task # 10-281 (Continuing)  
“Reliability of SiGe, SOI, and Advanced Mixed Signal  
Devices for Cryogenic Space Missions”***
- ***Goal, approach, schedule, and status of Task***
- ***Technical highlights***
- ***Plans***



# NEPP Task # 10-281 (Continuing)

## Reliability of SiGe, SOI, and Advanced Mixed Signal Devices for Cryogenic Space Missions

### Description:

*Space exploration missions require electronics that operate under extreme temperatures. SiGe devices utilize band gap engineering in their design to enable low temperature operation, and SOI parts offer good radiation tolerance and high temperature operation capability. This task focuses on establishing reliability of SiGe, SOI, and advanced mixed signal devices for use in extreme temperature space exploration missions. COTS parts and flight-like hardware will also be evaluated by determining their performance under extreme temperatures and thermal cycling. The generated data will establish safe operating areas and identify degradation modes, and the information will be disseminated to mission planners and system designers to establish risk factors associated with the use of such parts at extreme temperature in space applications.*

### FY10 Plans:

- *Identify and acquire COTS parts and flight-like hardware.*
- *Determine part/circuit operational requirements.*
- *Conduct screening tests at extreme temperatures.*
- *Perform combined thermal/electrical tests.*
- *Determine the effects of wide temperature thermal cycling.*
- *Publish reports and disseminate information.*

### Schedule:

	2009			2010								
	O	N	D	J	F	M	A	M	J	J	A	S
Acquire COTS & mission-related devices	█	█	█	█	█	█						
Screen devices at extreme temperatures	█	█	█	█	█	█	█					
Down-select promising devices				█	█	█	█	█				
Perform thorough characterization				█	█	█	█	█	█	█	█	
Perform thermal cycling on selected parts				█	█	█	█	█	█	█	█	
Analyze & document results				█	█	█	█	█	█	█	█	
Publish BOK reports & disseminate info.				◆			◆			◆	█	█
Propose 2011 follow-on task								◆				

### Deliverables:

- *Issue technical reports documenting reliability of selected SiGe, SOI, and advanced mixed signal devices for extreme temperature operation.*
- *Publish results on NEPP website and at professional conferences and disseminate information to mission planners and system designers.*
- *Submit quarterly progress reports.*



# Goals

- **Establish a technology base for the development of electronic systems, using COTS parts, capable of extreme temperature operation for space exploration missions**
- **Disseminate information and transfer technology to NASA mission groups and aerospace designers**



# Expected Impact to Community

## Traditional approach to extreme temp operation

- **Passive or active thermal control**
- **Warm electronic box**
- **Radioisotope heater units**

## Impact of “extreme temperature electronics”

- **Simplify thermal management**
- **Improve energy density and system efficiency**
- **Improve reliability**
- **Reduce overall system mass**
- **Reduce development and launch costs**



# Status/Schedule

	2009			2010								
	O	N	D	J	F	M	A	M	J	J	A	S
Acquire COTS & mission-related devices	████████████████████											
Screen devices at extreme temperatures	████████████████████			████████████████████								
Down-select promising devices				████████████████████								
Perform thorough characterization				██								
Perform thermal cycling on selected parts				██								
Analyze & document results				██								
Publish tech reports & disseminate info.				◆			◆			◆	→	◆
Propose 2011 follow-on task								◆				



# FY10 Highlights/Accomplishments

- **Submitted deliverable test report “Evaluation of a High Temperature SOI Half-Bridge MOSFET Driver, Type CHT-HYPERION”**
- **Submitted deliverable test report “Use of a Frequency Divider to Evaluate an SOI NAND Gate Device, Type CHT-7400, for Wide Temperature Applications”**
- **Submitted deliverable test report “Evaluation of a Programmable Voltage-Controlled MEMS Oscillator, Type SiT3701, over a Wide Temperature Range”**



## NASA Applications

Target	Temperature (°C)
Venus	+480
Lunar Surface	-230 → +120
Mars Surface	-125 → +20
Jupiter	-160 → +300
Europa (Jupiter)	-160 → -120
Titan (Saturn)	-180 → -150



## **Silicon Germanium (SiGe)**

**Utilize band-gap engineering to tailor properties such as preventing carrier freeze-out**

**e.g. Diodes, HBT's, Op Amps, VCO's**

## **Silicon-on-Insulator (SOI)**

**Offer reduced leakage current, high temperature capability, improved radiation tolerance, & less power consumption**

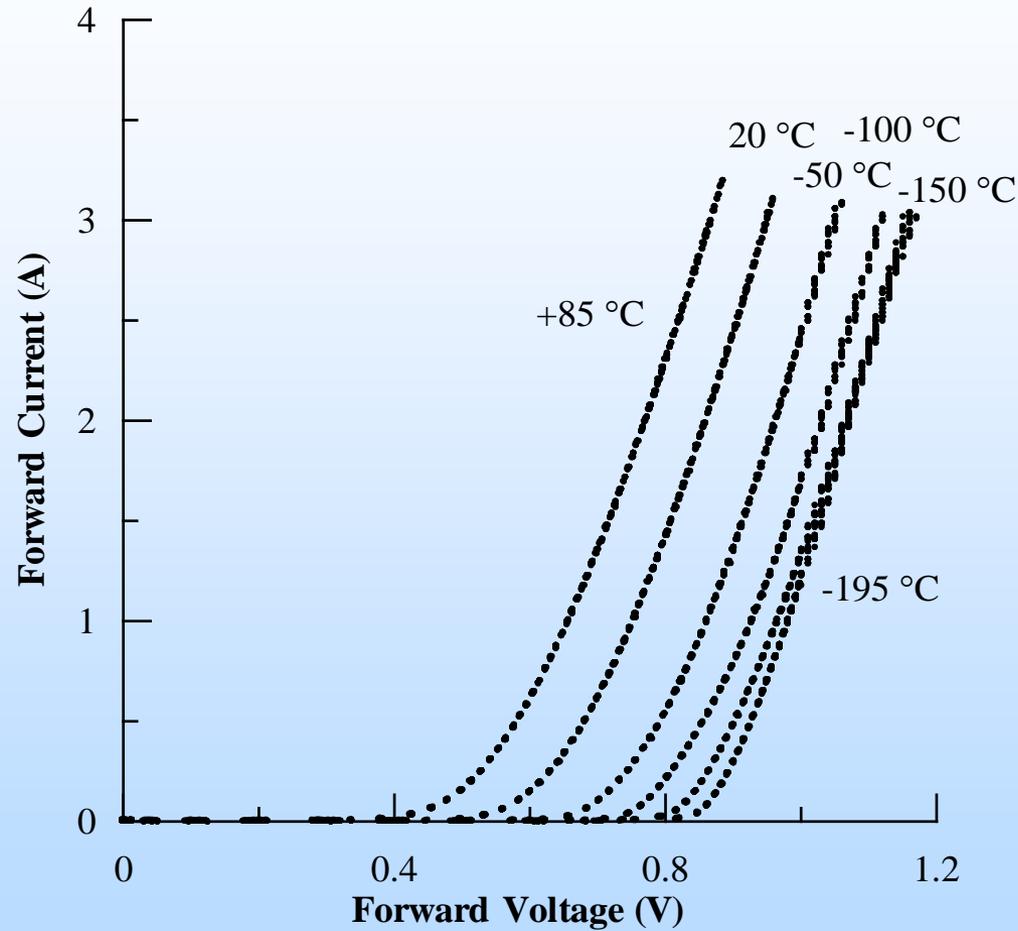
**e.g. Timers, Op Amps, Logic, MOSFET's, Drivers,  $V_{REF}$**

## **Advanced Mixed Signal**

**Employ new material & design technologies to enhance performance and improve reliability**

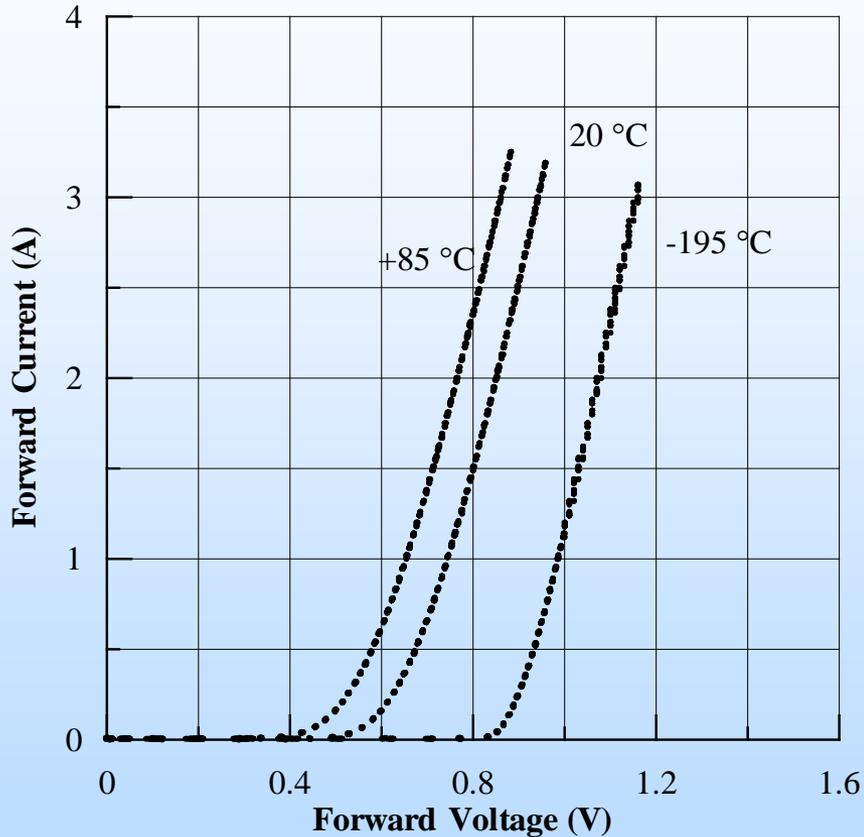
**e.g. MEMS Oscillators, VCO's, Converters,  $V_{REG}$**

## Forward V-I characteristics of a SiGe diode, type SG 21-41

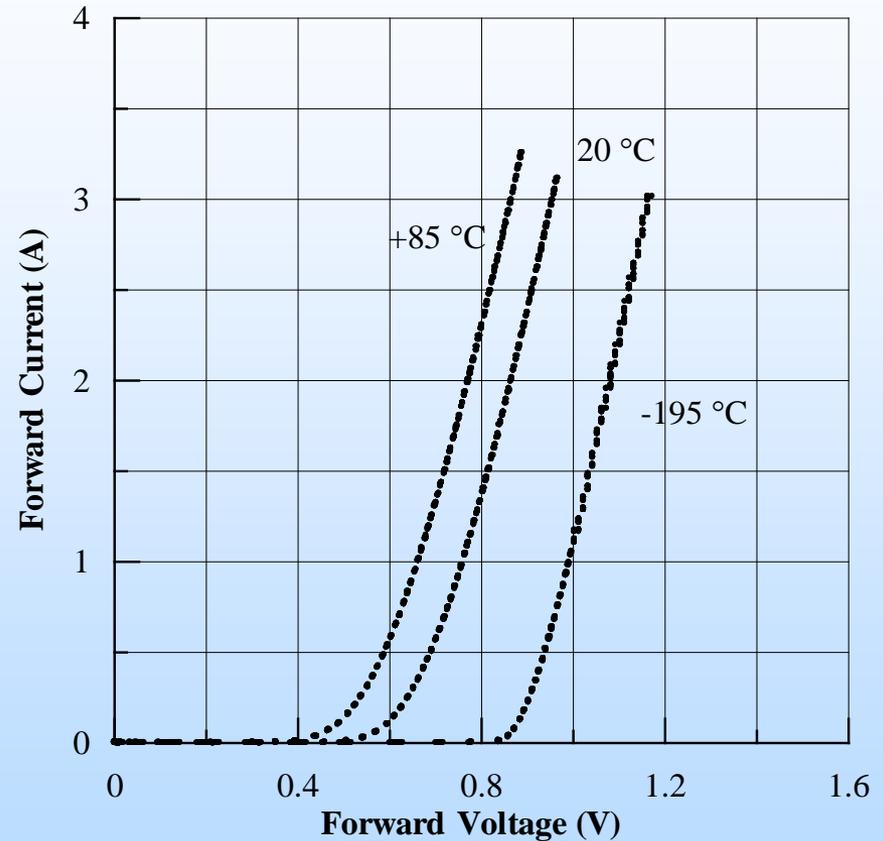


**SiGe diode operated successfully to -195 °C with increase in forward voltage drop.**

## SiGe power diode, type SGD-P51 (12 cycles; -195 °C to +85 °C)



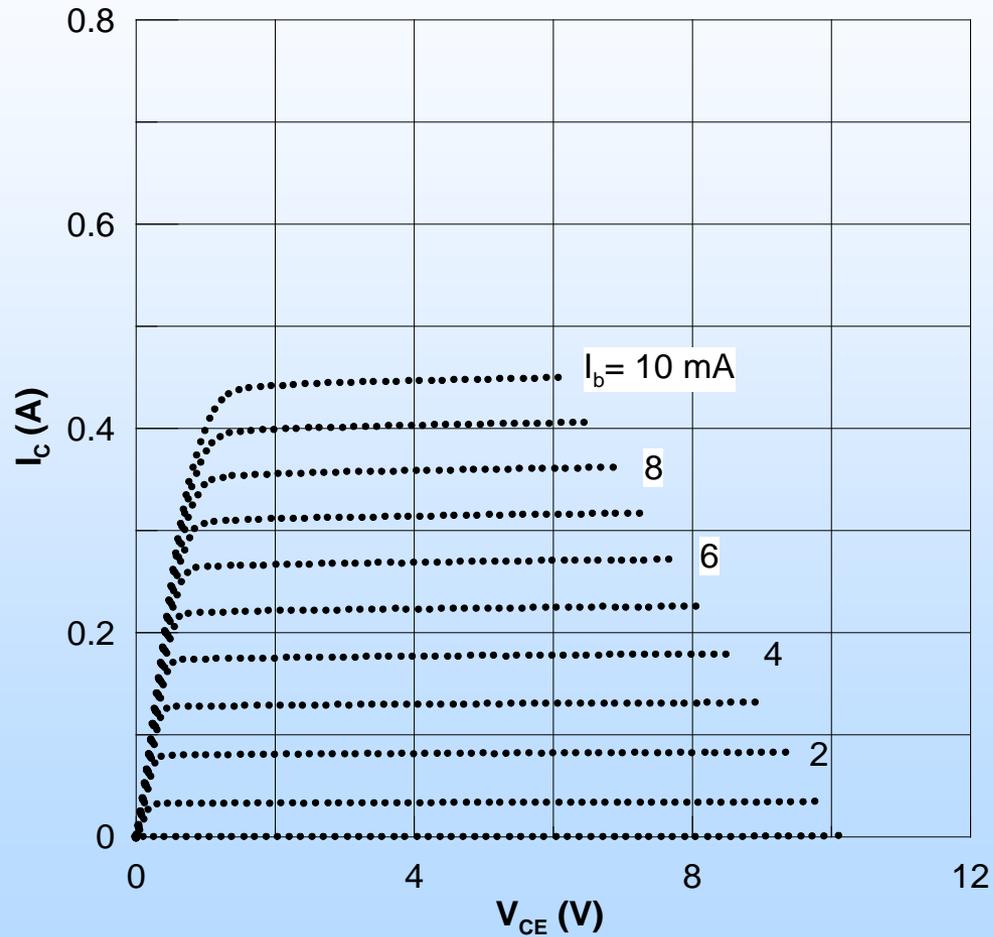
Pre-cycling



Post-cycling

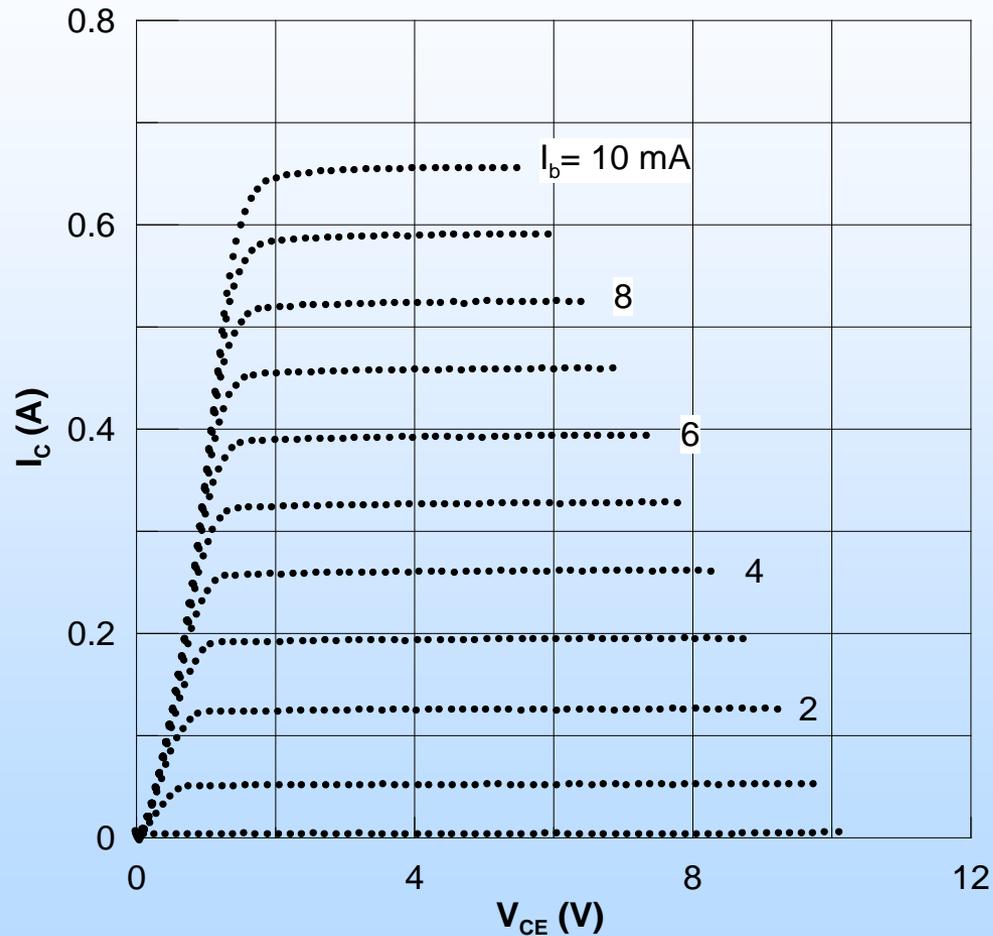
**Thermal cycling had little effect on operation of SiGe diode.**

## $I_C$ versus $V_{CE}$ of a SiGe HBT, type L2-32, at +20 °C



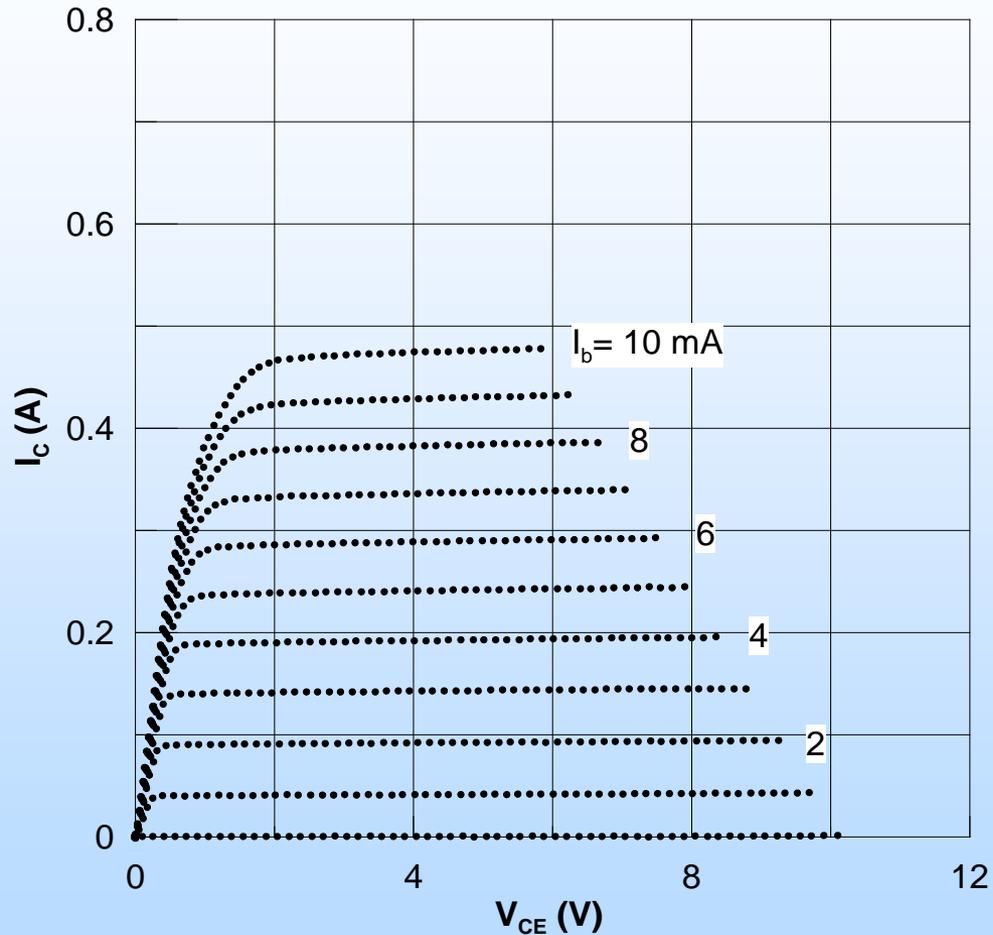
**Room temperature baseline info on a SiGe HBT.**

## $I_C$ versus $V_{CE}$ of a SiGe HBT, type L2-32, at $-195\text{ }^\circ\text{C}$



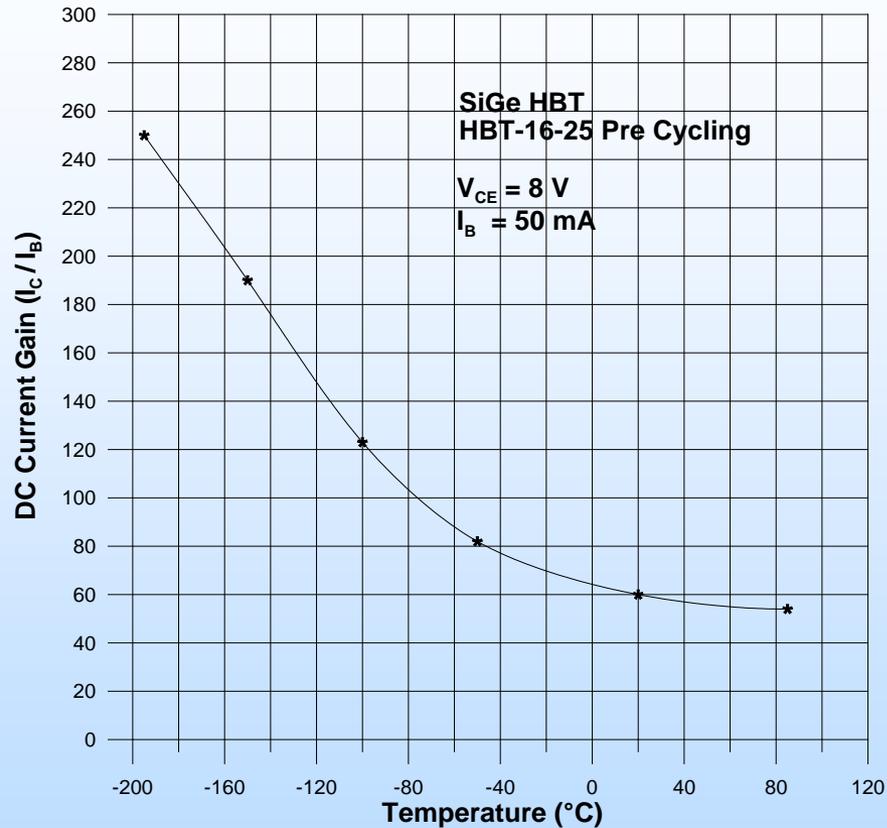
**Increased current gain at  $-195\text{ }^\circ\text{C}$  for same SiGe HBT device.**

## $I_C$ versus $V_{CE}$ of a SiGe HBT, type L2-32, at +85 °C



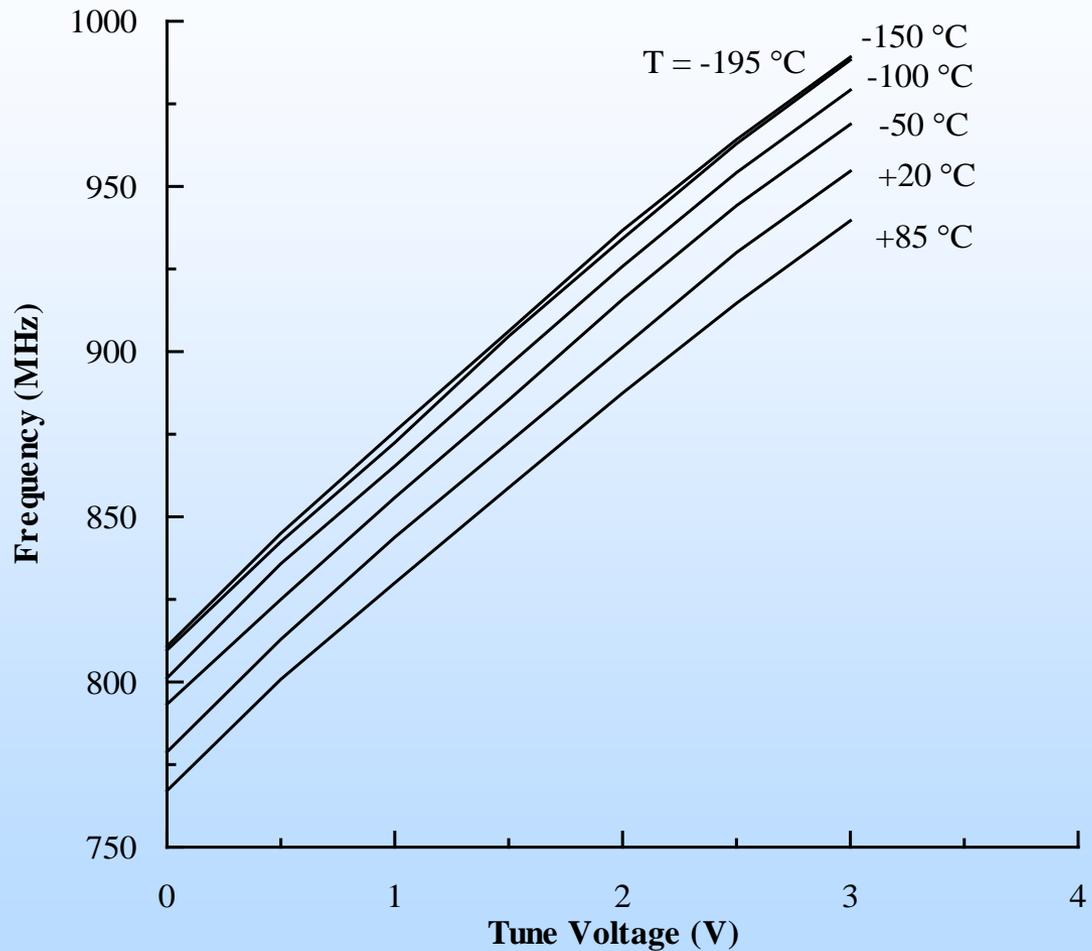
**Slightly increased current gain at +85 °C compared to room temp gain.**

## Current gain of a SiGe HBT, type GPD 16-25, power transistor



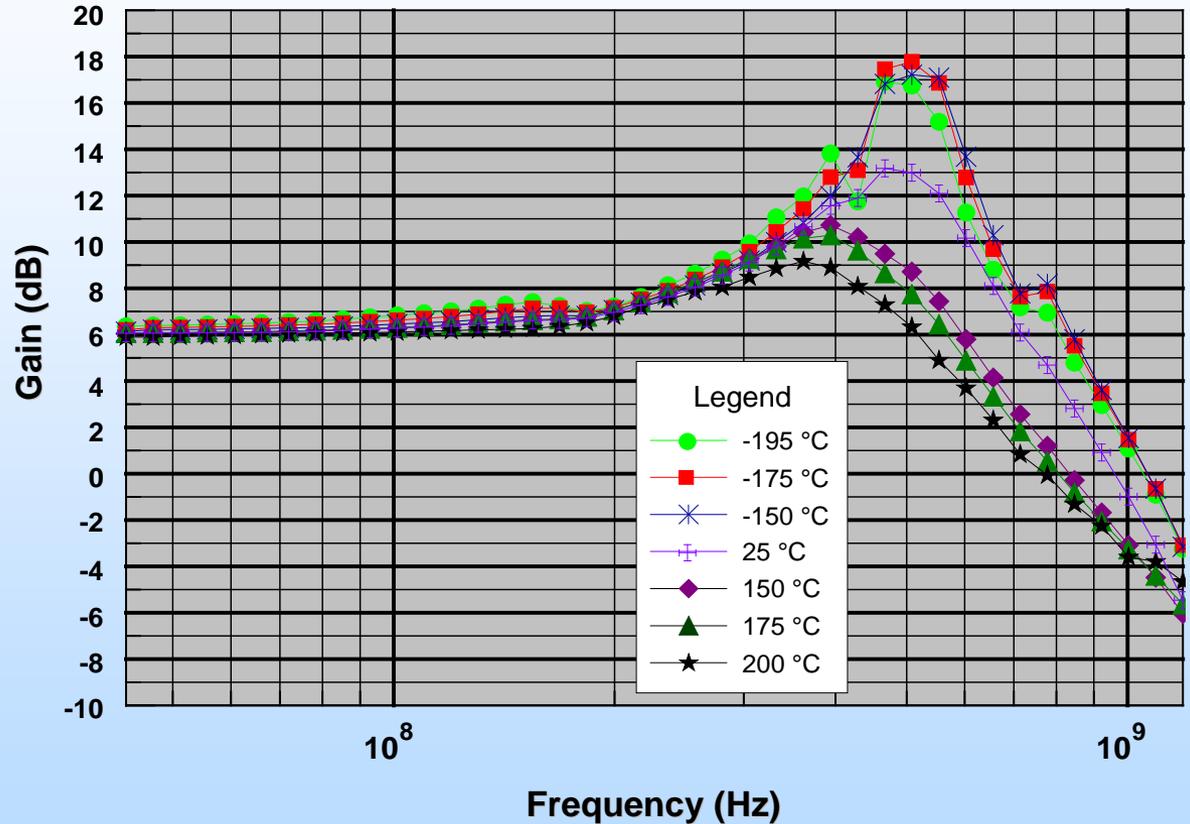
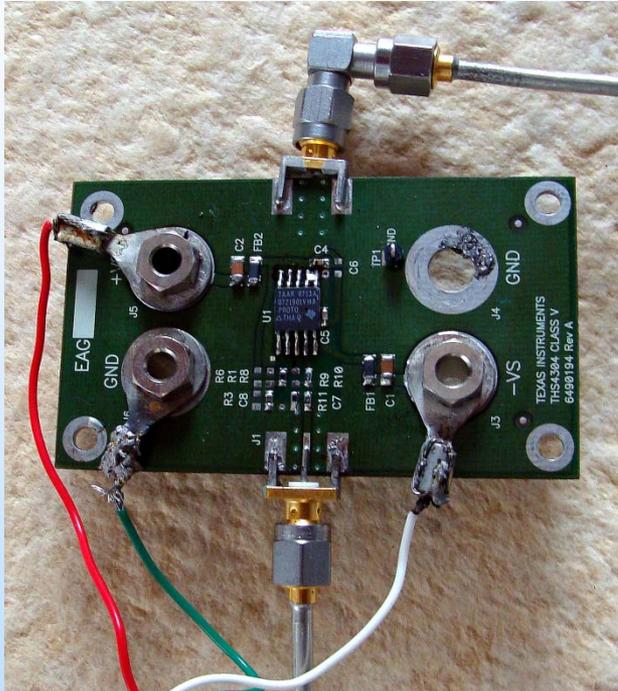
**Very large increase in DC current gain at low temperatures for SiGe HBT power transistor.**

## Output frequency of a SiGe VCO, type MAX2622



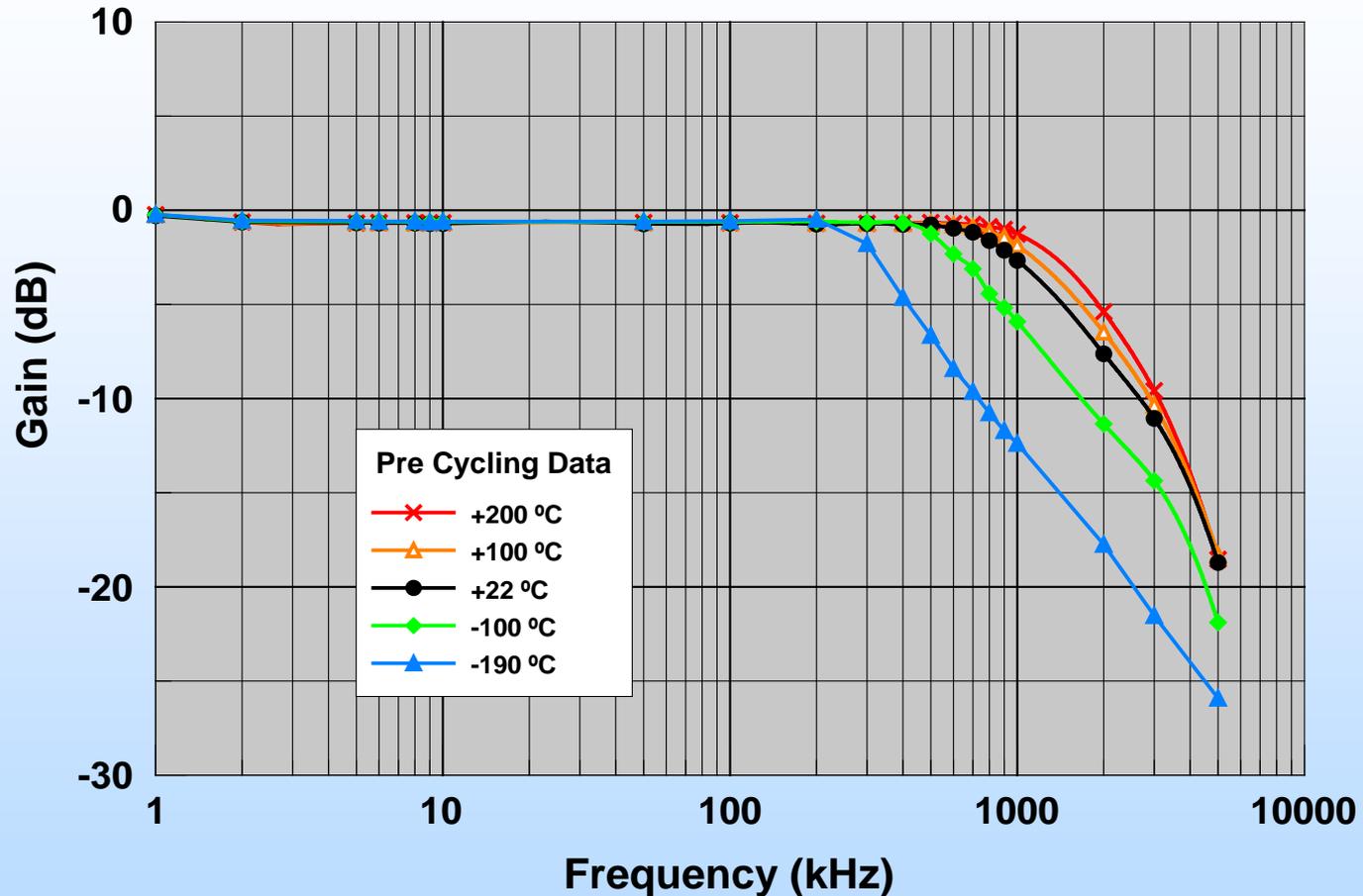
**SiGe voltage controlled oscillator operating over wide temperature range.**

# Class V rad-tolerant THS4304-SP silicon germanium amplifier



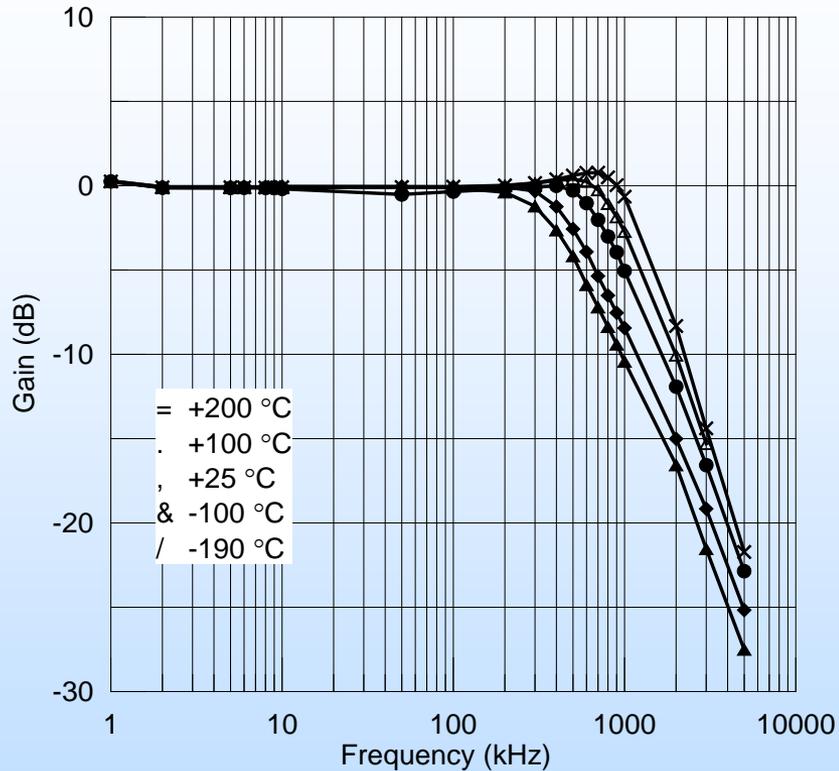
**Wide temperature range operation of Class V Rad-Tolerant SiGe amplifier.**

## SOI operational amplifier , type HTOP-01

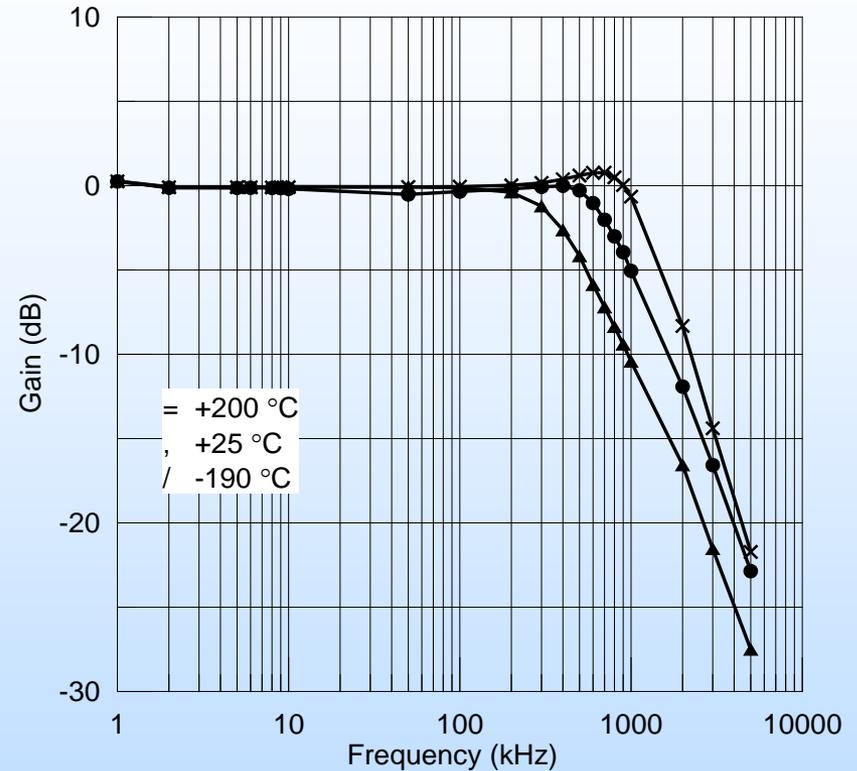


**Cryogenic operation of a 200 °C rated silicon-on-insulator op amp.**

## Gain of an SOI CHT-OPA operational amplifier



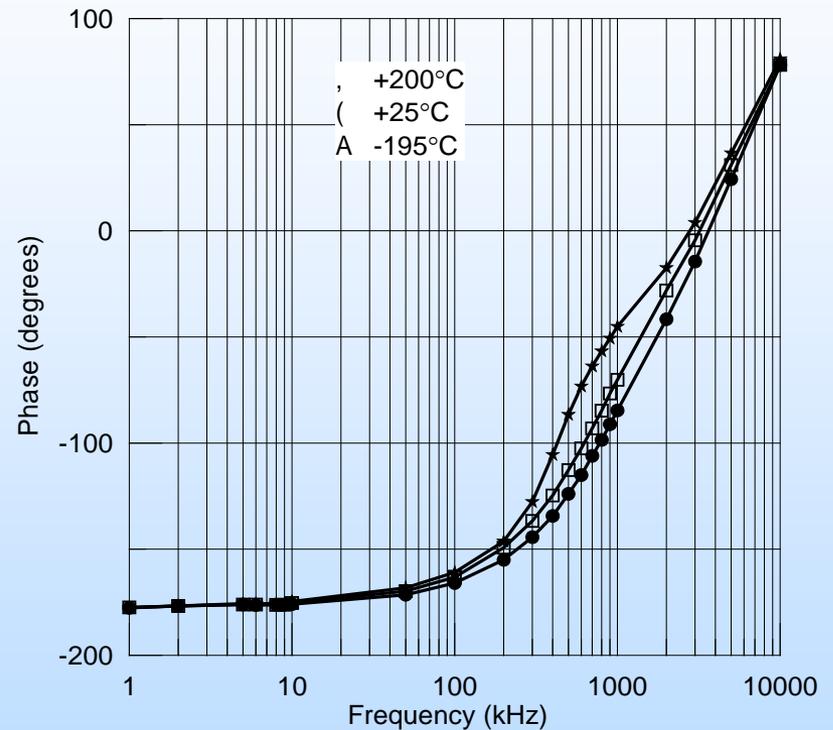
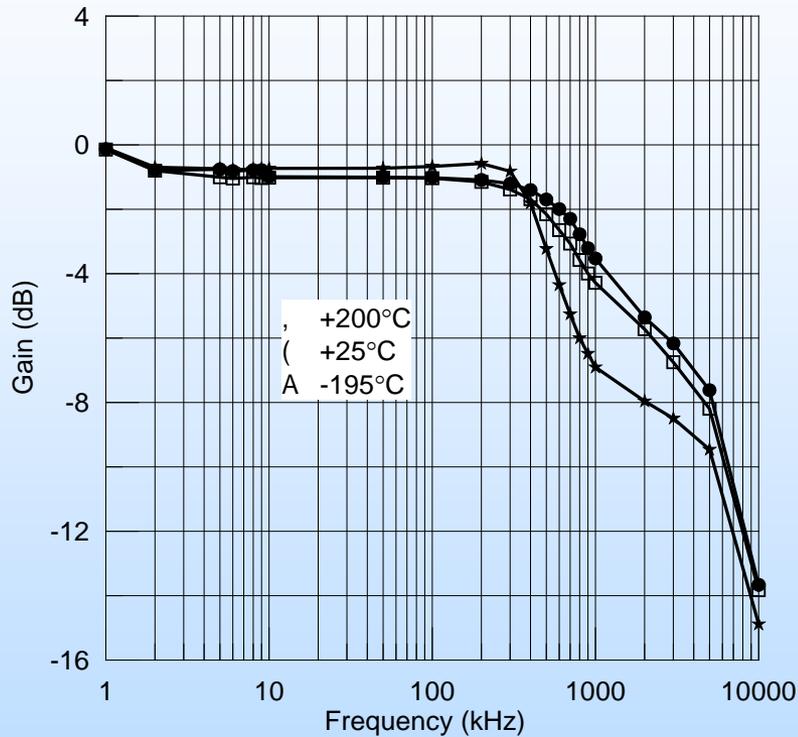
Before thermal cycling.



After thermal cycling.

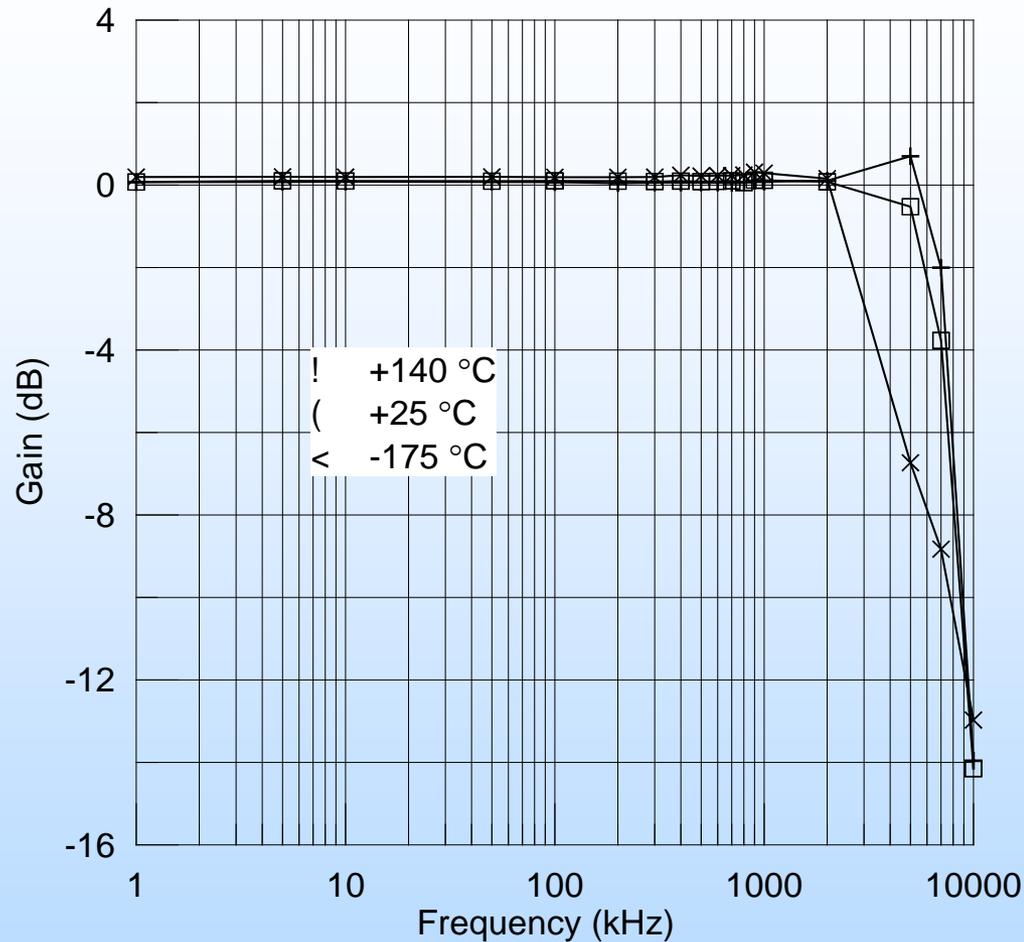
**Thermal cycling had little effect on operation of SOI operational amplifier.**

## Characteristics of an SOI HT-1104 operational amplifier after thermal cycling



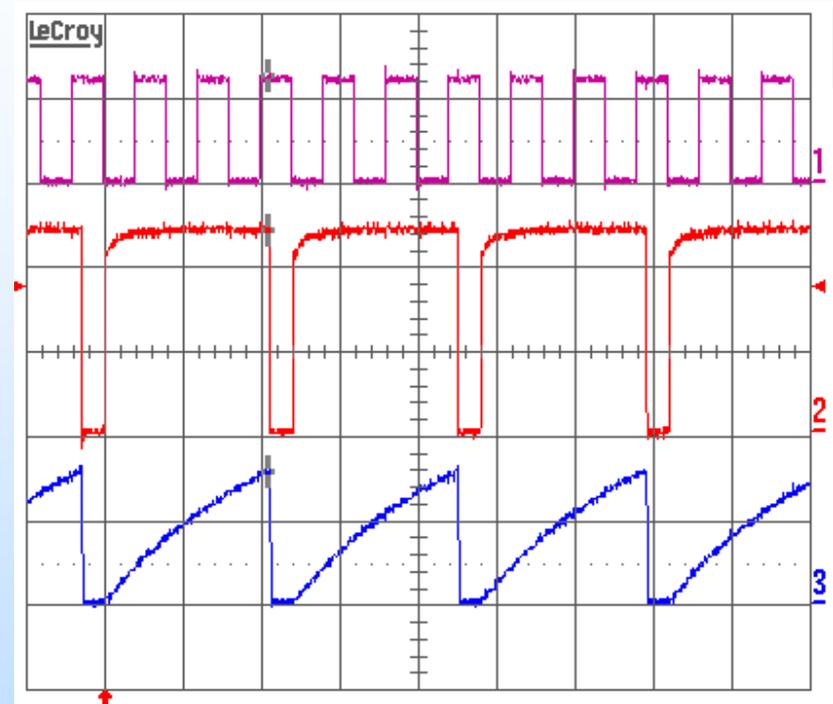
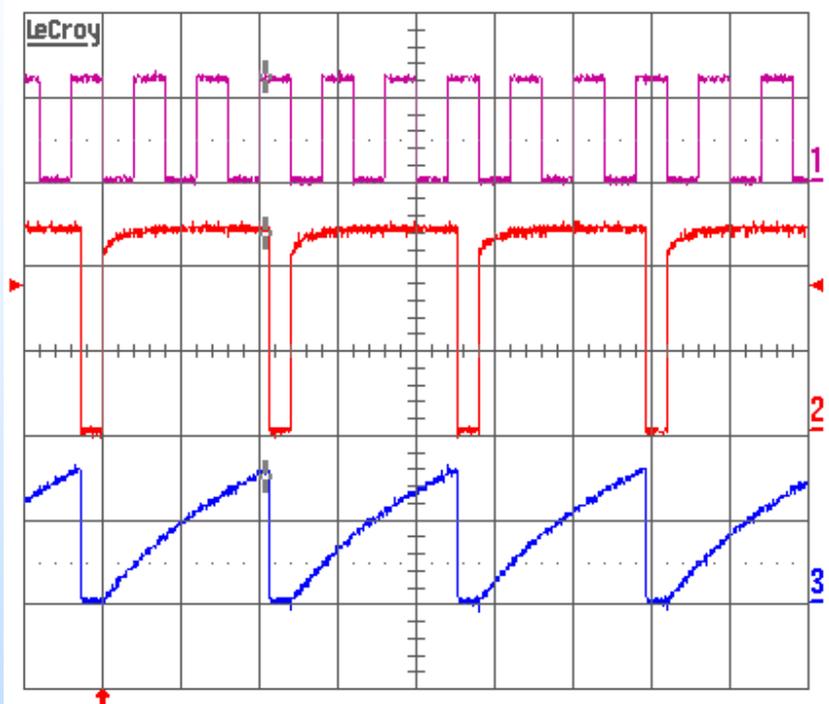
**Gain & Phase of an SOI HT-1104 Operational Amplifier**  
**Data taken Post Thermal Cycling between -195 °C & +200 °C**

## Gain of a SiGe/SOI , type OPA-211, operational amplifier



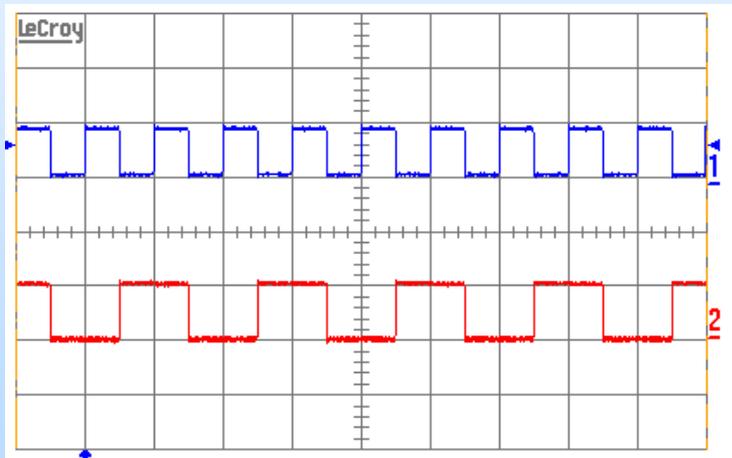
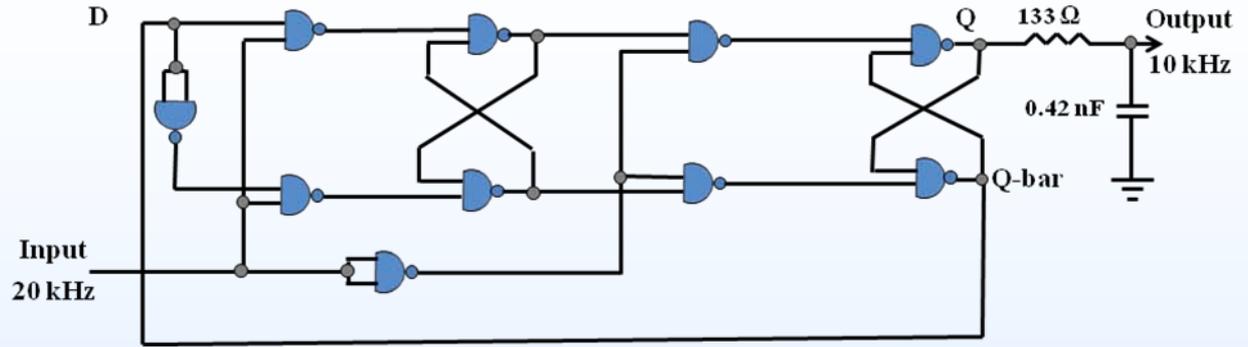
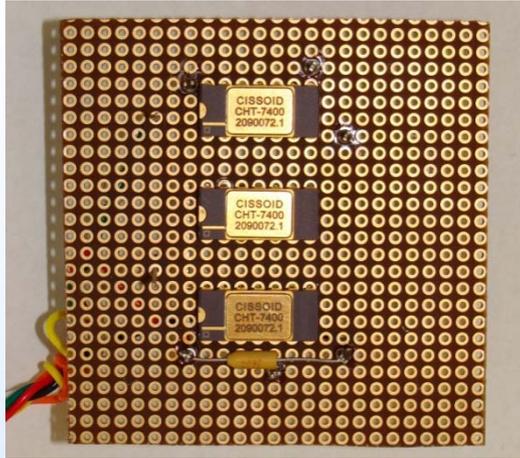
**Broad frequency range gain stability of a unique SiGe/SOI op amp over a wide temperature range.**

## Silicon-on-Insulator CHT-555 timer

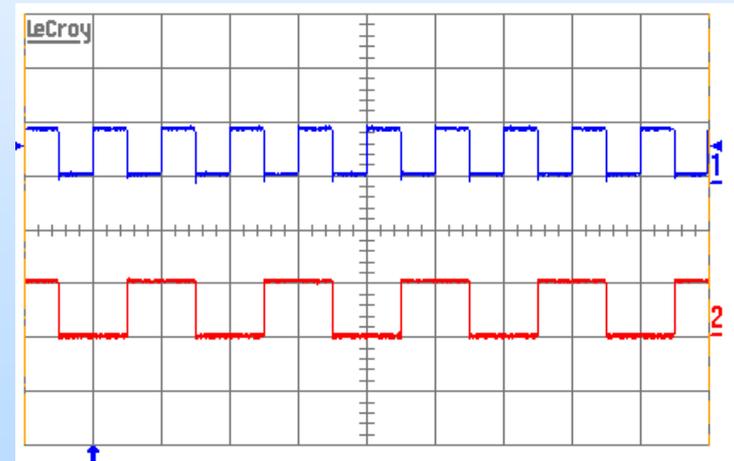


**Trigger (1), output (2), and threshold (3) signals of a high temperature SOI CHT-555 timer at room temperature and at -195 °C.**

# Divide-by-2 circuit using SOI quad NAND devices



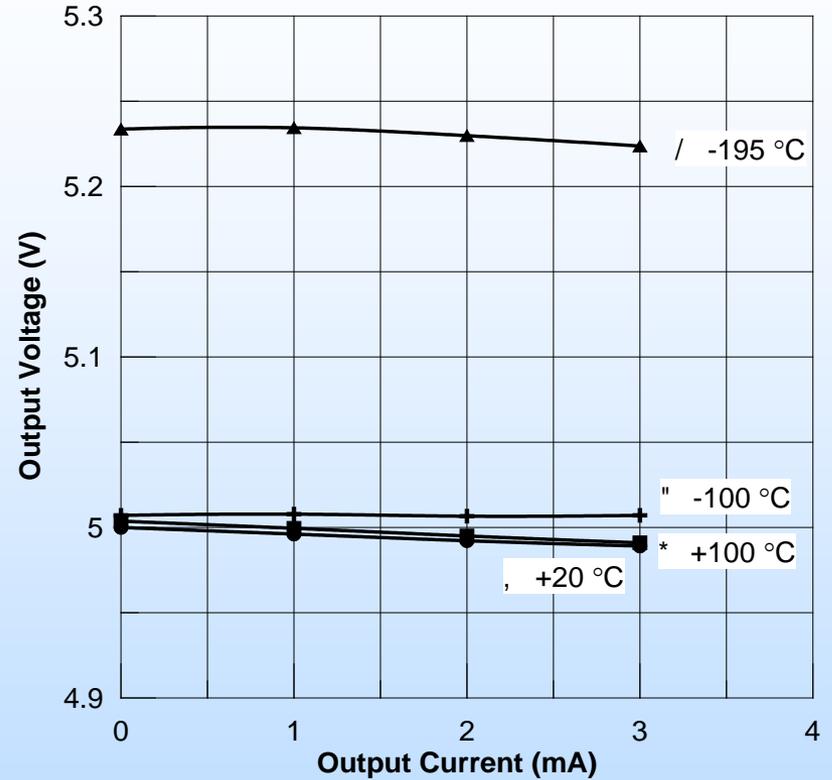
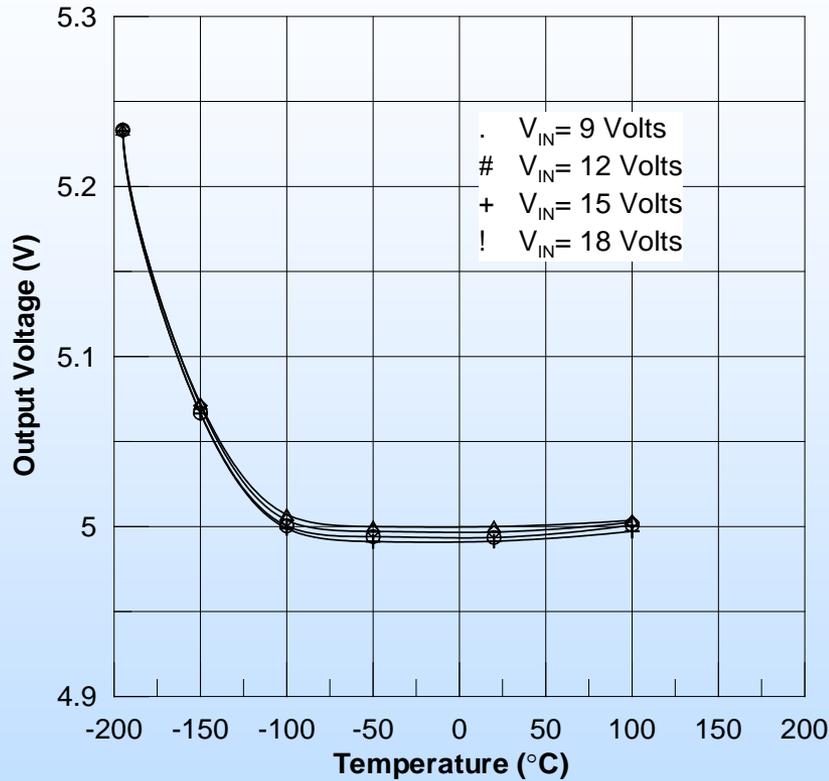
-192 °C



+225 °C

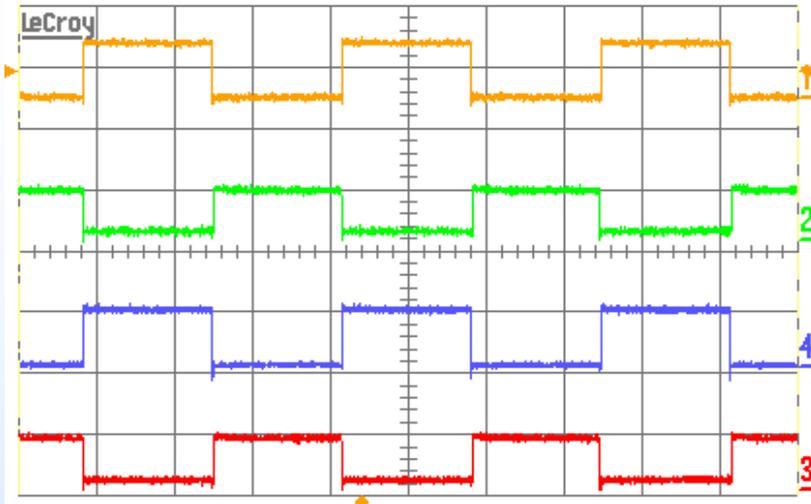
**Successful operation of SOI digital circuit over a very wide temperature range.**

# SOI CMOS voltage reference, type CHT-BG-050

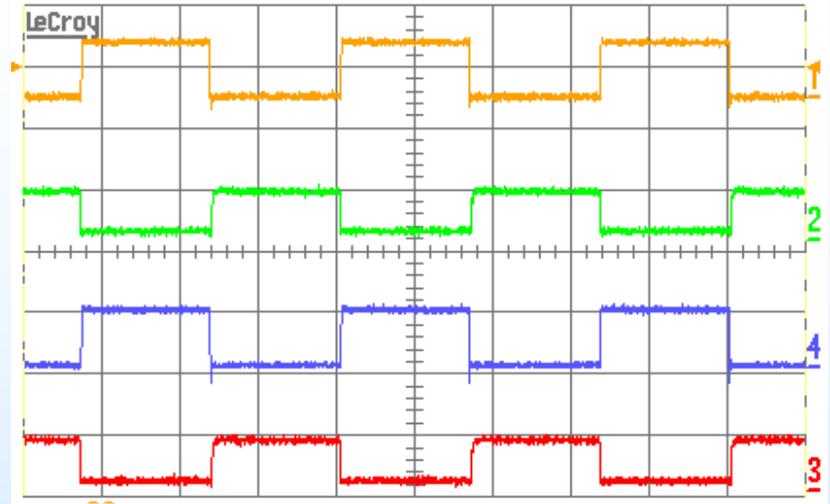


**Excellent stability of SOI CMOS voltage reference from -100 °C to +100 °C.**

# SOI full-bridge driver, type CHT-FBDR

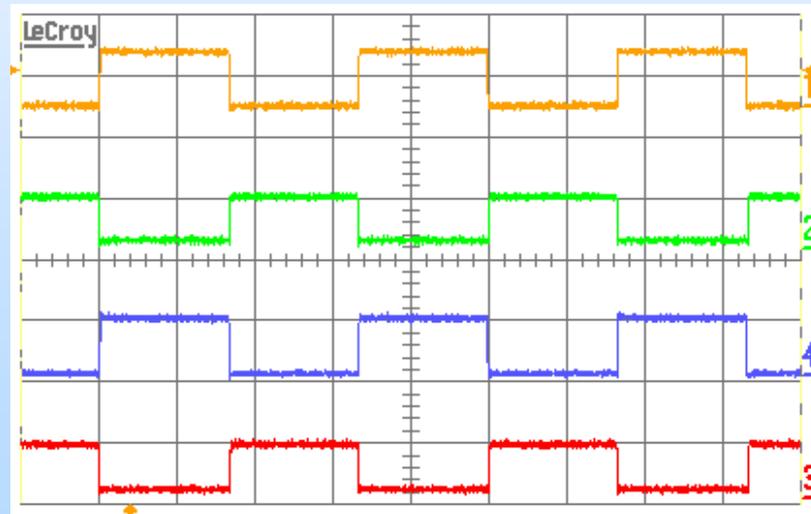


+25°C



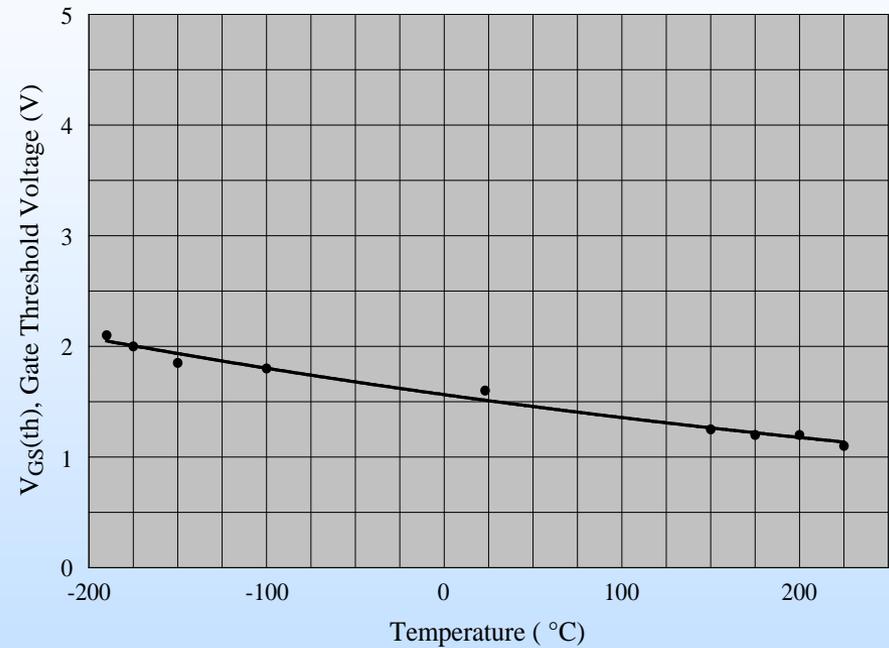
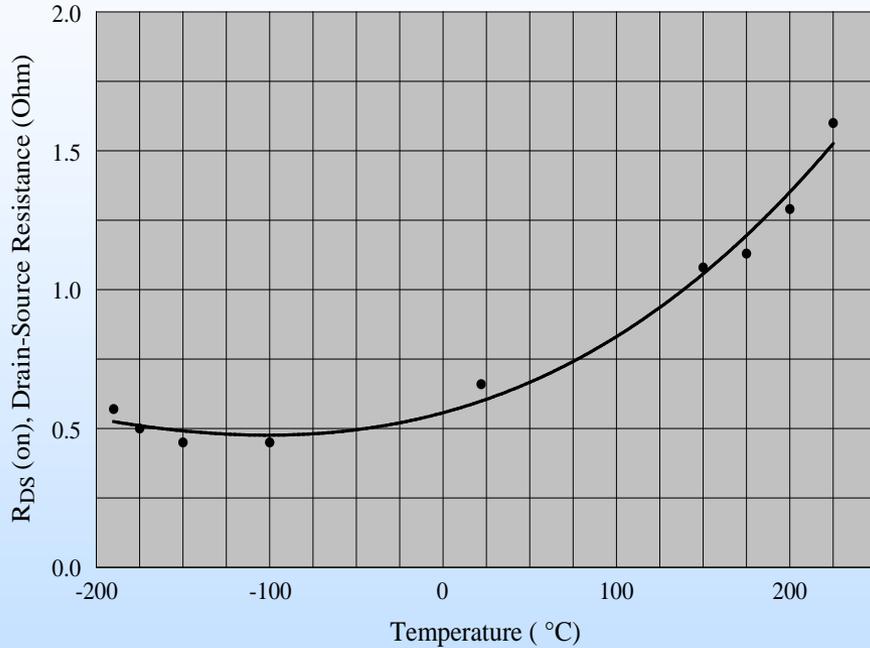
-190°C

+225°C



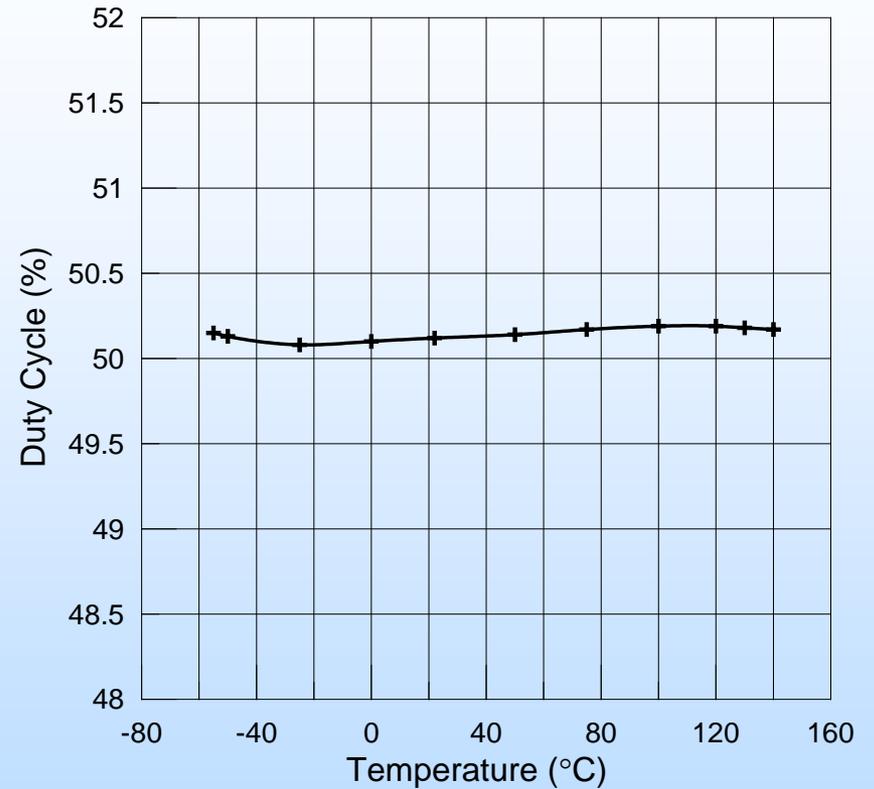
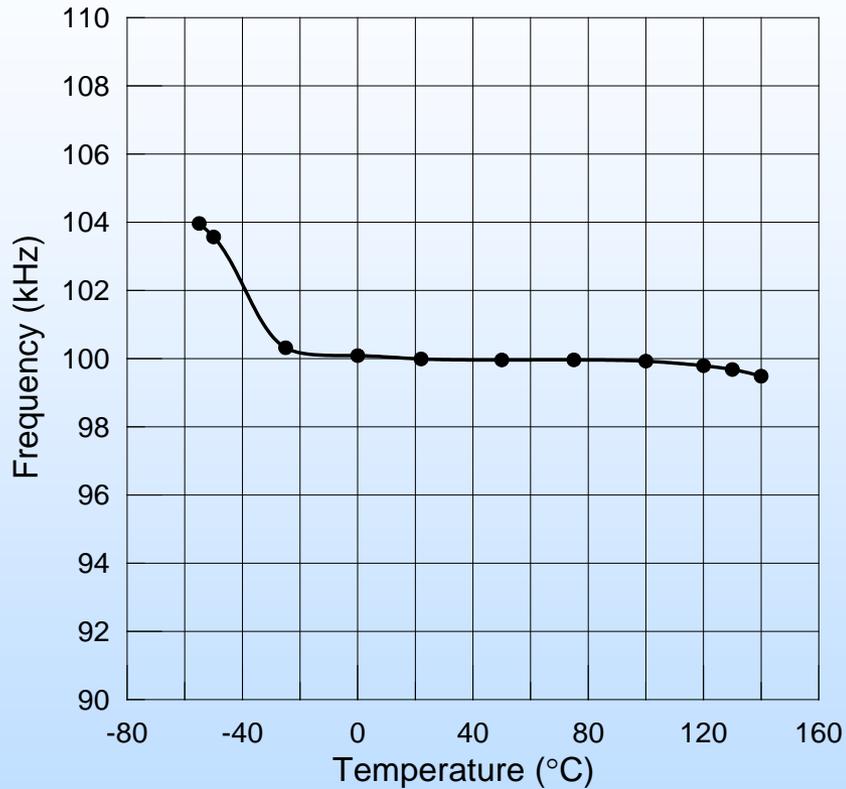
**No effect of temperature on operation of an SOI full-bridge driver.**

## Characteristics of an N-channel SOI MOSFET, type NMOS80



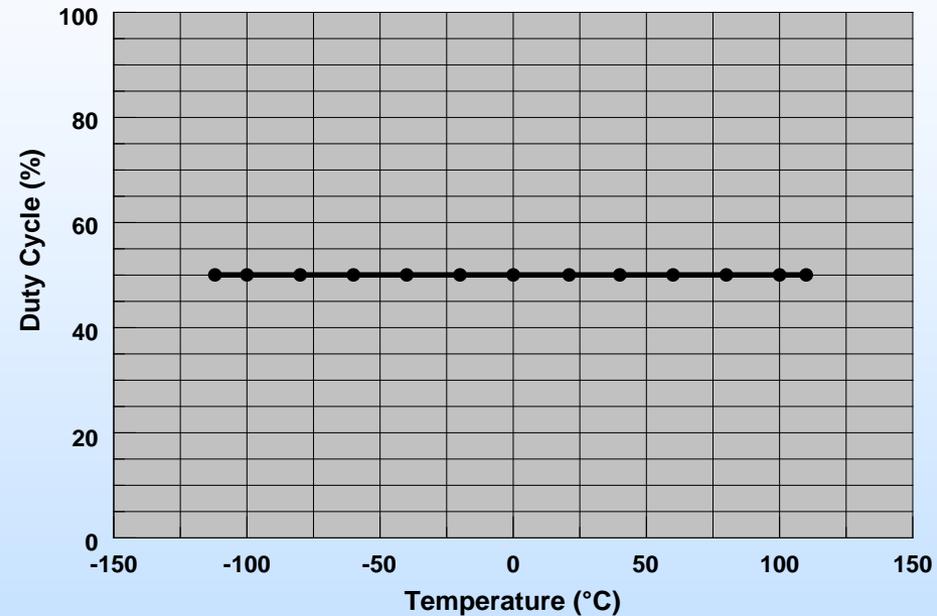
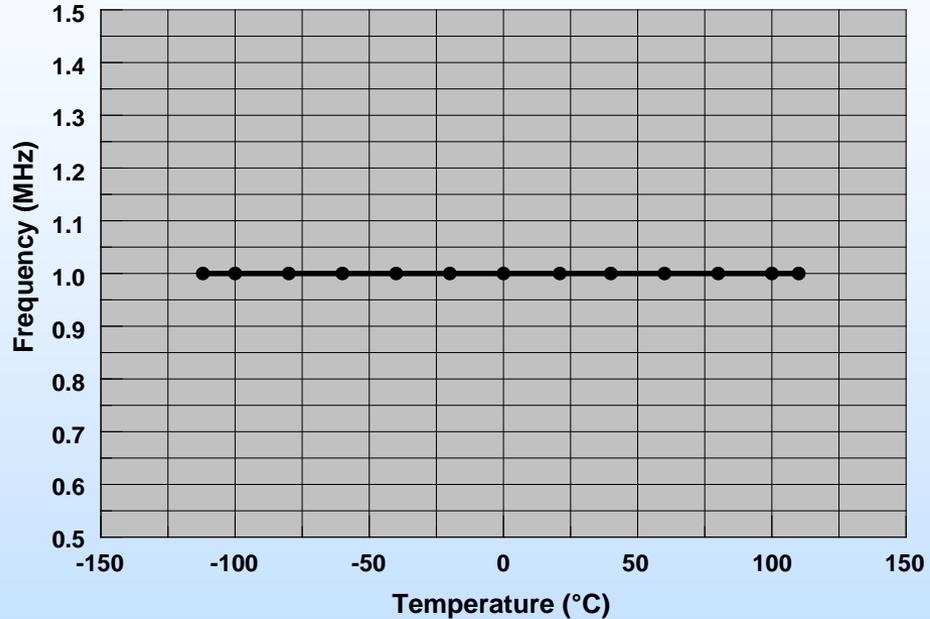
**$R_{DS}$  held steady between -195 °C and -20 °C but increased with further increase in temperature.  $V_{GTH}$  exhibited linear decrease with increase in temperature.**

## All-silicon oscillator, type ASFLM-1



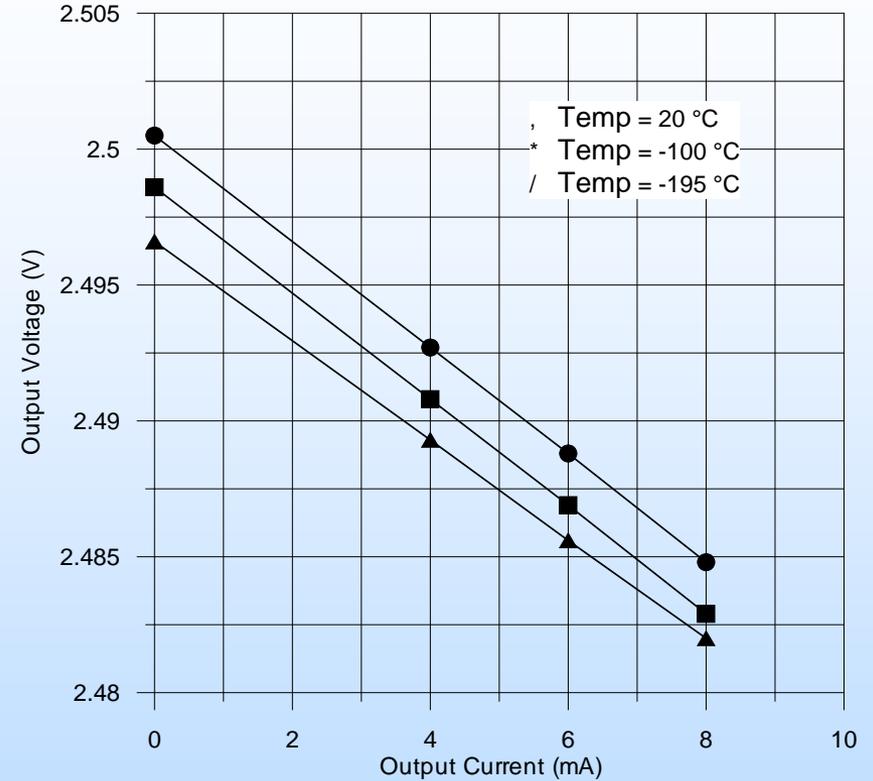
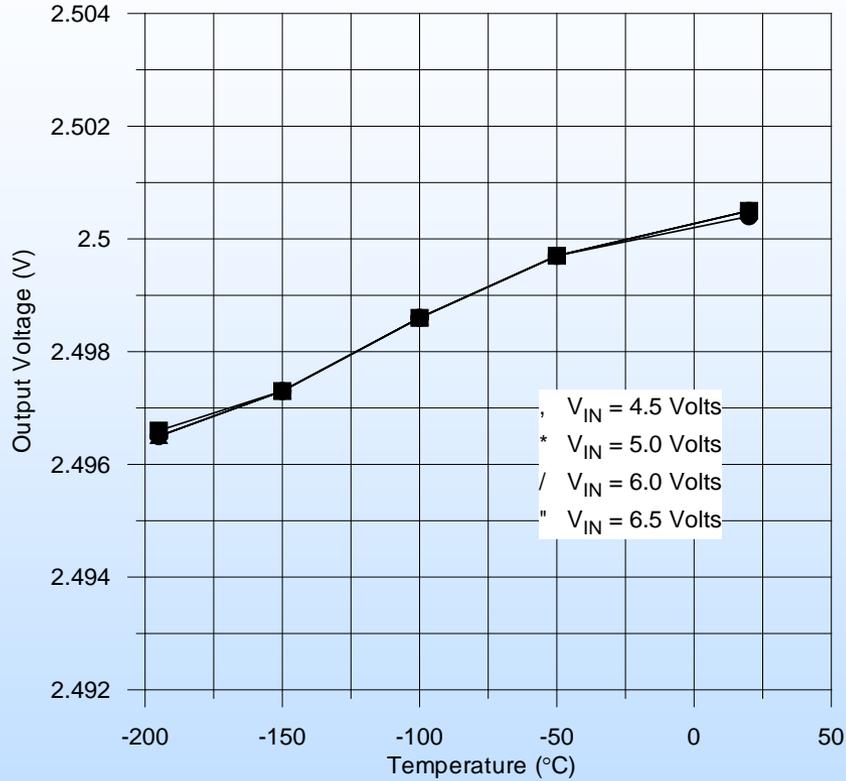
**Good frequency stability from +120 °C to -25 °C.**

## MEMS silicon oscillator, type EMK21



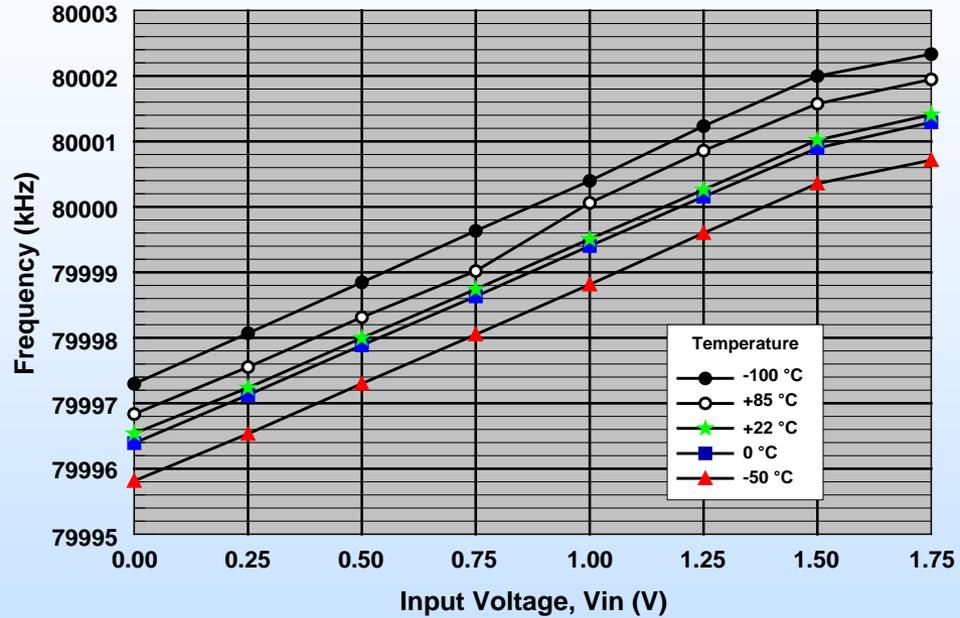
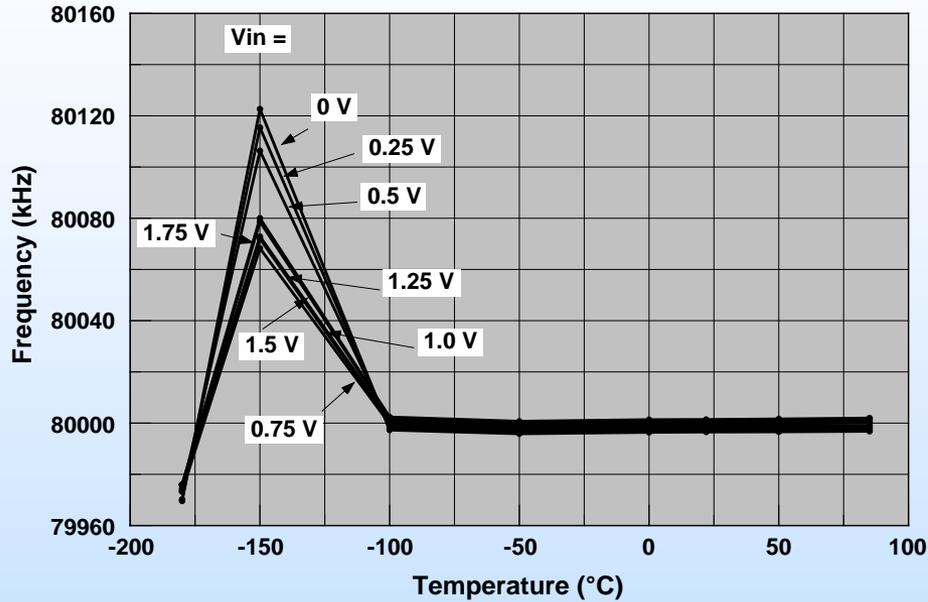
**Excellent frequency stability from +110 °C to -110 °C.**

## Floating-gate voltage reference, type X60008B



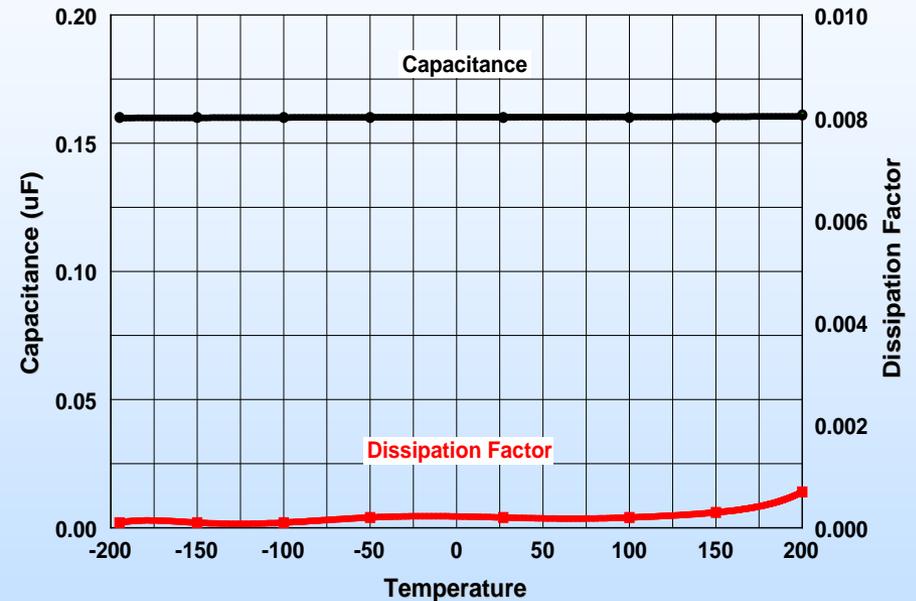
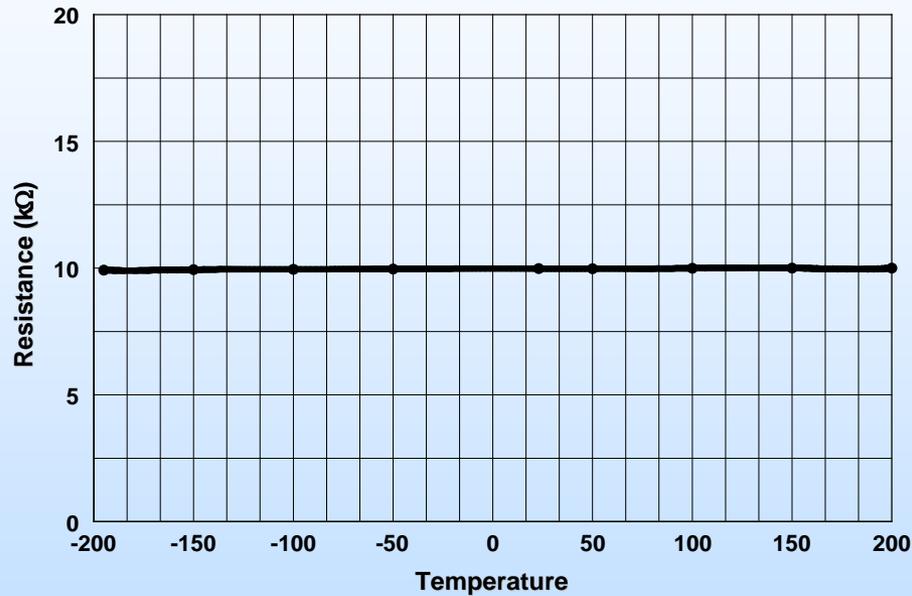
**Excellent voltage stability from +25 °C to -195 °C.**

# MEMS voltage-controlled oscillator, type SiT3701



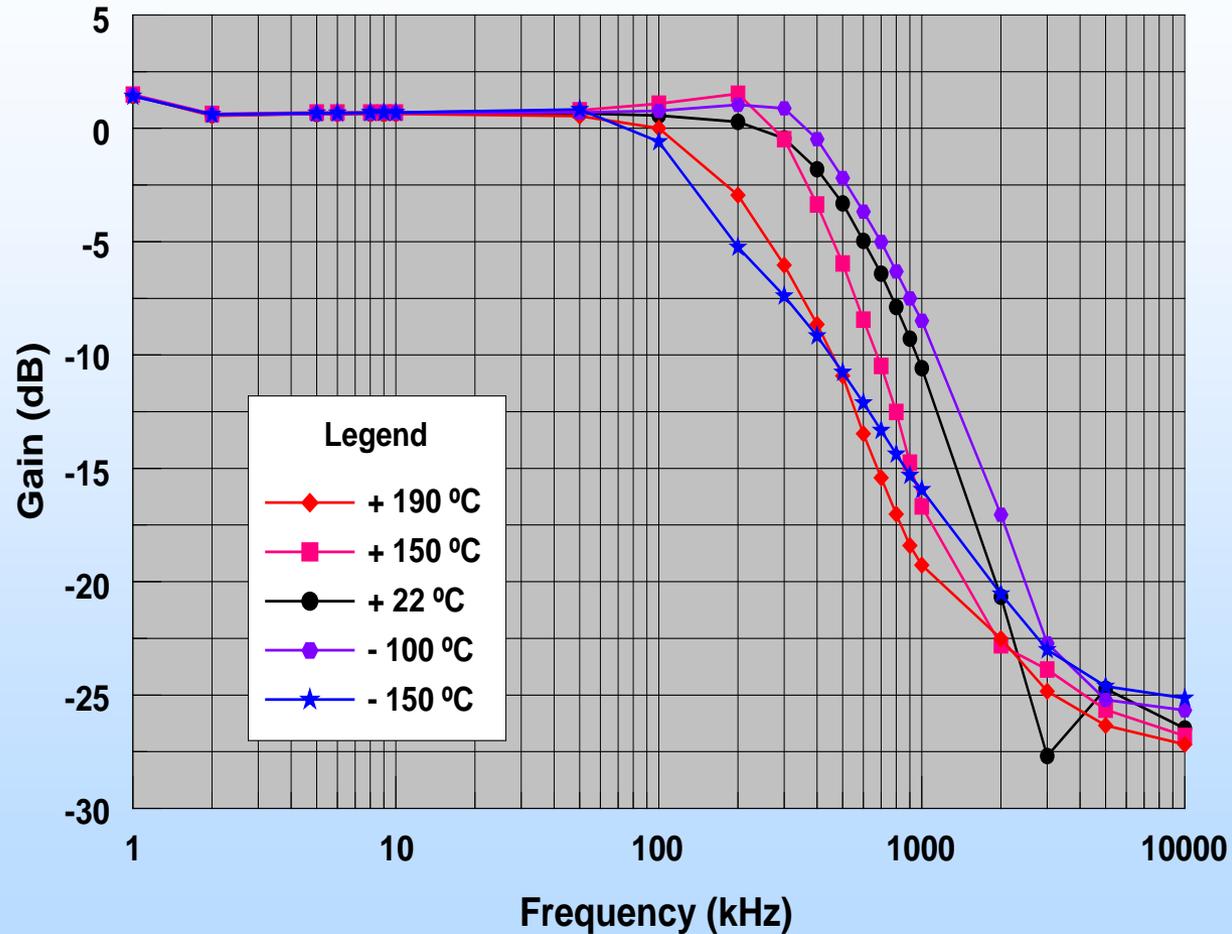
**This oscillator showed excellent frequency stability between +85 °C and -100 °C.**

# Passives: wire-wound resistor (93J10K) & NP0 capacitor (SM041A164K)



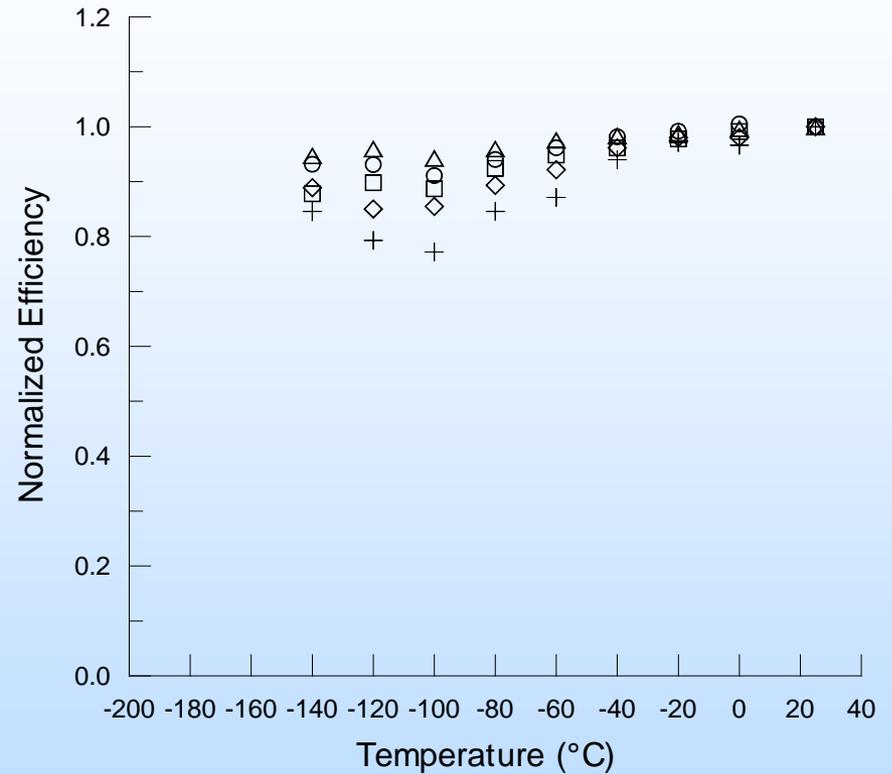
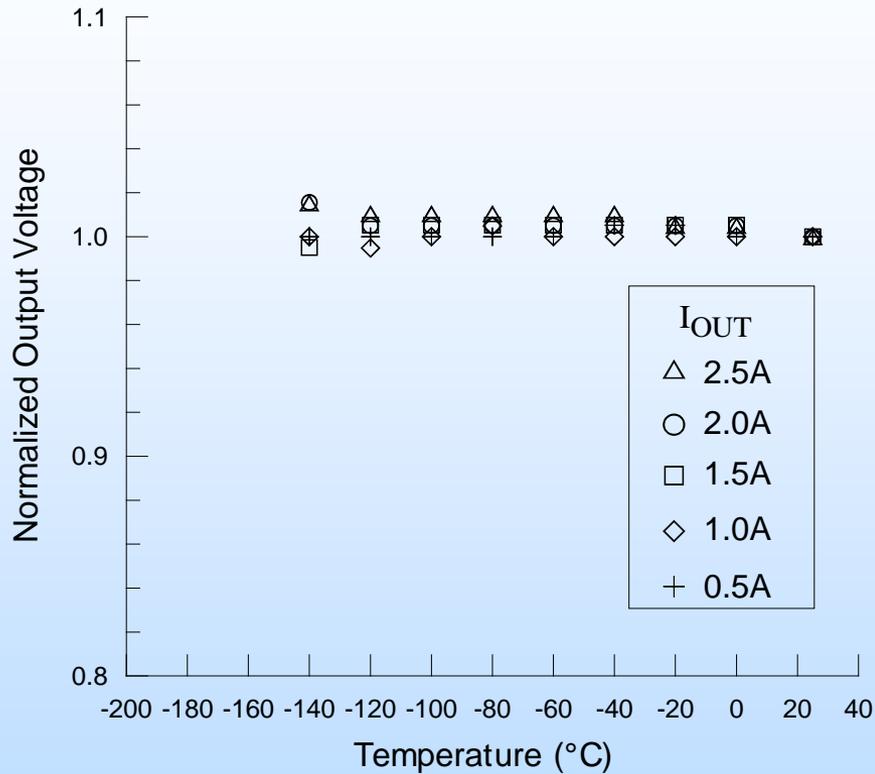
**These are special passive devices that have good stability over a wide temperature range.**

# New high temperature (150 °C) operational amplifier, type LM2904WH



**This is a new silicon operational amplifier for high temperature use.  
Rated at +150 °C, it also operated down to -150 °C.**

## 3.3V, 10W rad-hard DC/DC converter



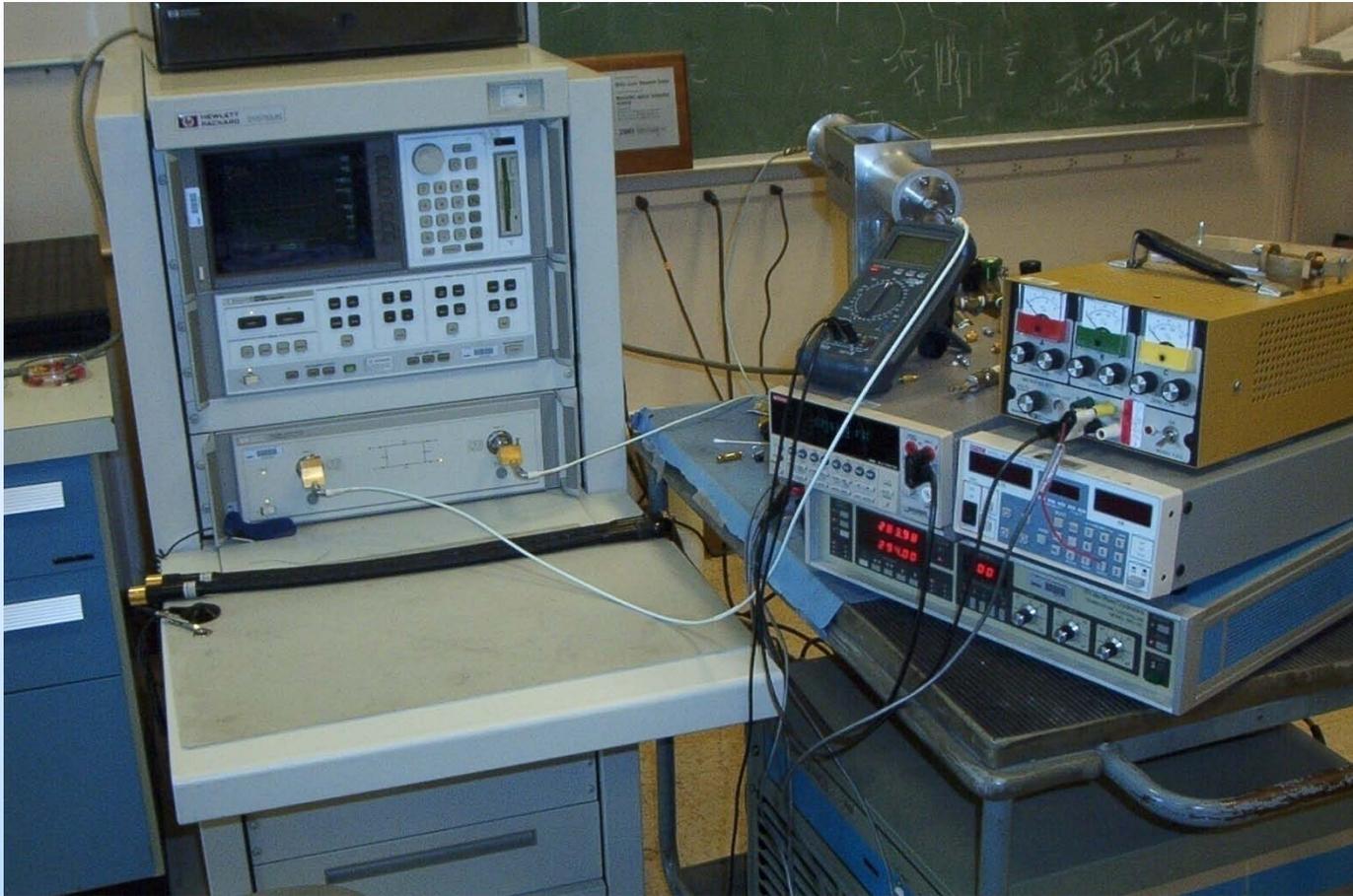
**This rad-hard DC/DC converter operated well down to -140 °C.**

## Test facilities at NASA Glenn Research Center

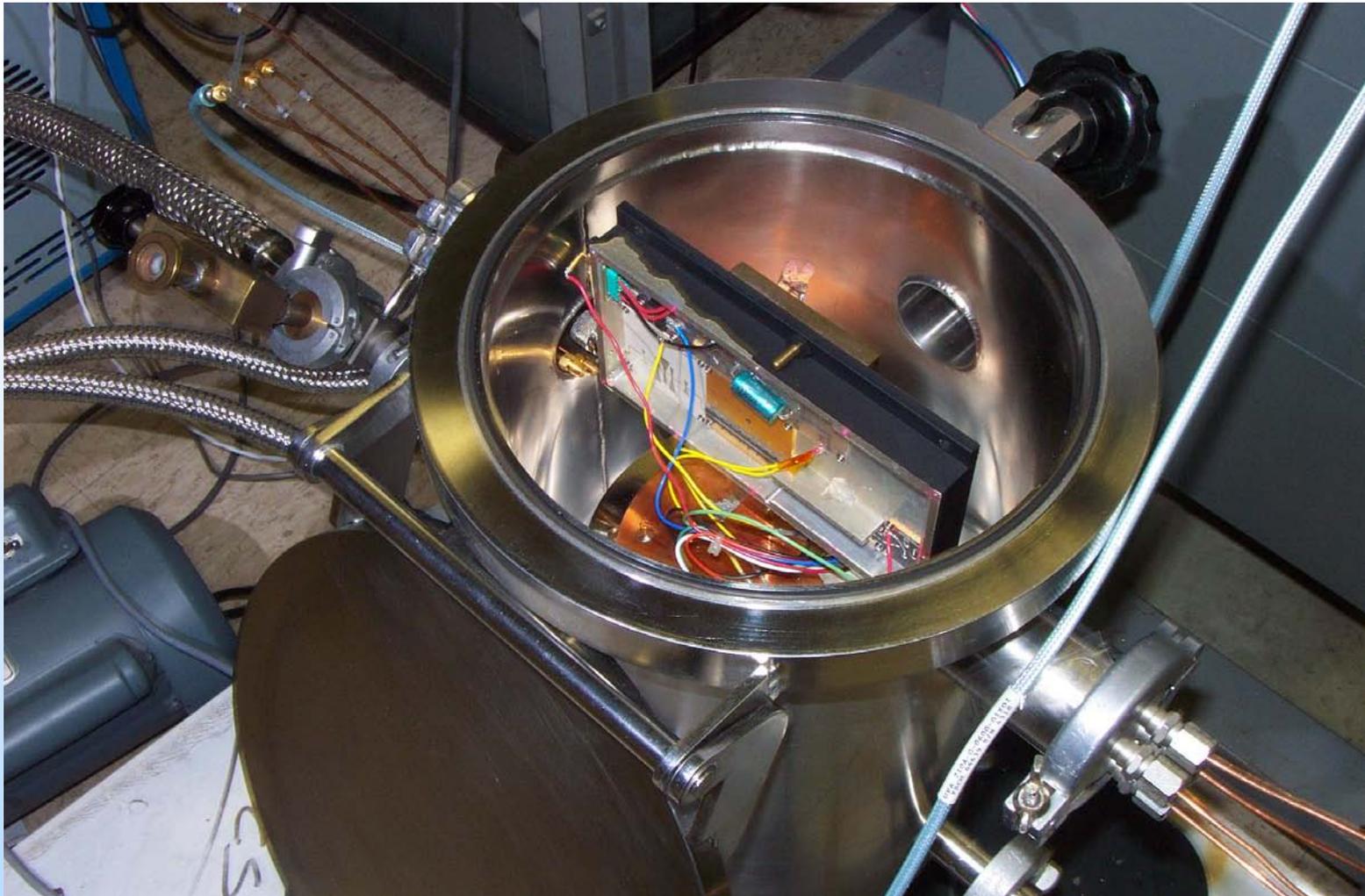


**There is a 240 liter liquid nitrogen dewar on the right, and there are two environmental chambers in the background.**

## Test facilities at NASA Glenn Research Center



**This equipment was used to evaluate semiconductor devices at extremely low temperatures and at radio frequencies.**



**This chamber was used to evaluate a radio frequency amplifier for low temperature operation in a new space shuttle landing system.**



## Plans for FY11

- **Identify and acquire SiGe, SOI, and advanced mixed signal electronic parts with potential for use in extreme temperature space missions. (Q1-Q2 FY11)**
- **Setup test facilities, determine part operational requirements, and establish test matrix. (Q1-Q2 FY11)**
- **Perform testing on acquired SiGe, SOI, advanced mixed signal parts, and flight-like hardware over an extended temperature range. (Q1-Q4 FY11)**
- **Determine performance of promising parts under wide temperature thermal cycling. (Q3-Q4 FY11)**
- **Document data and disseminate information to the NASA designers and mission planners. (Q4 FY11)**
- **Publish results on NASA NEPP Website, in technical journals, and at engineering conferences. (Q4 FY11)**