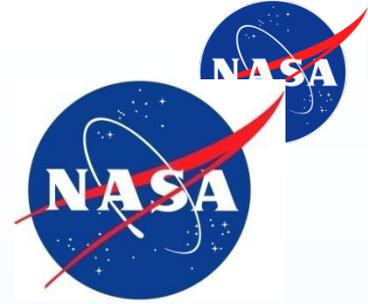


**NEPP Electronic Technology Workshop  
June 22-24, 2010**

National Aeronautics  
and Space Administration



# **On-Going Radiation Effects on FPGAs - Lessons Learned and Plans**

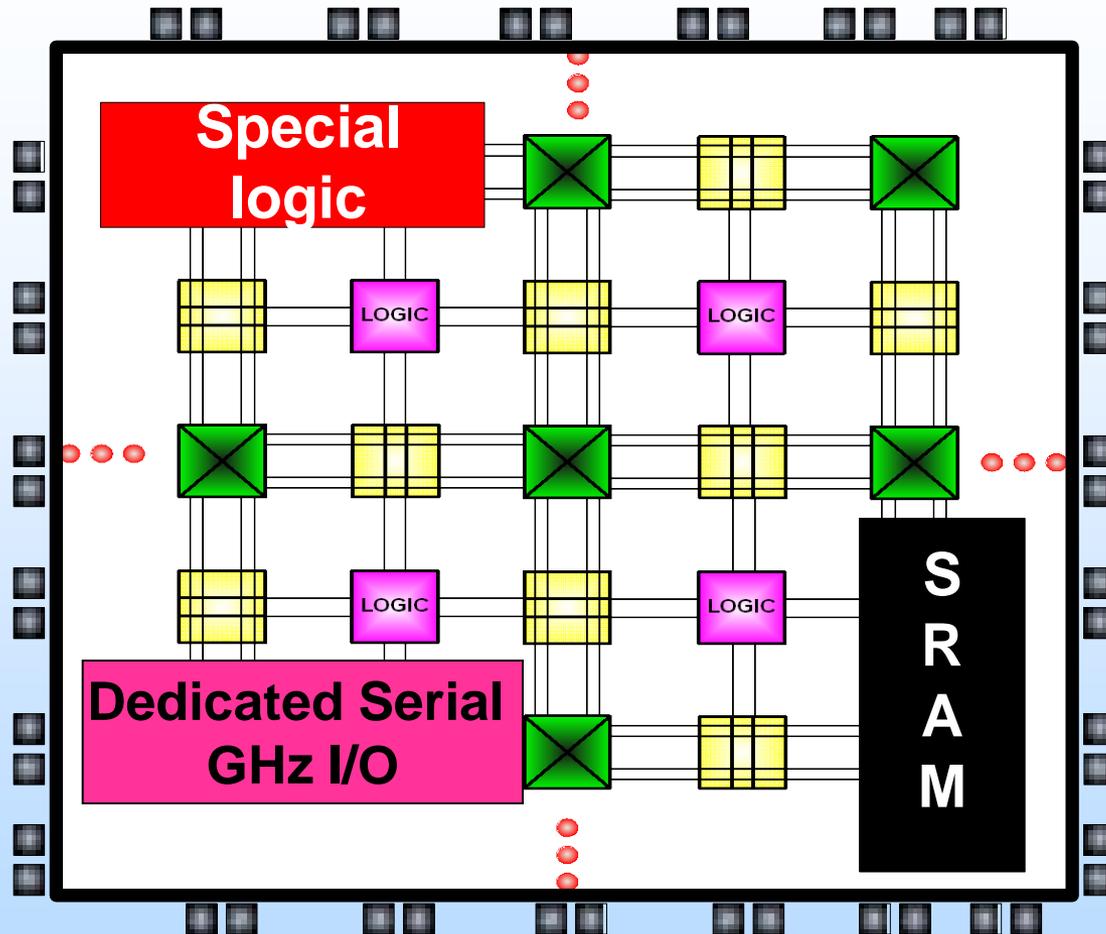
**Melanie Berg, MEI Technologies/NASA GSFC**

**M. Friendlich, C. Perez, H. Kim, C. Seidlick, A. Phan: MEI  
Technologies/NASA GSFC**

**K. LaBel: NASA GSFC**

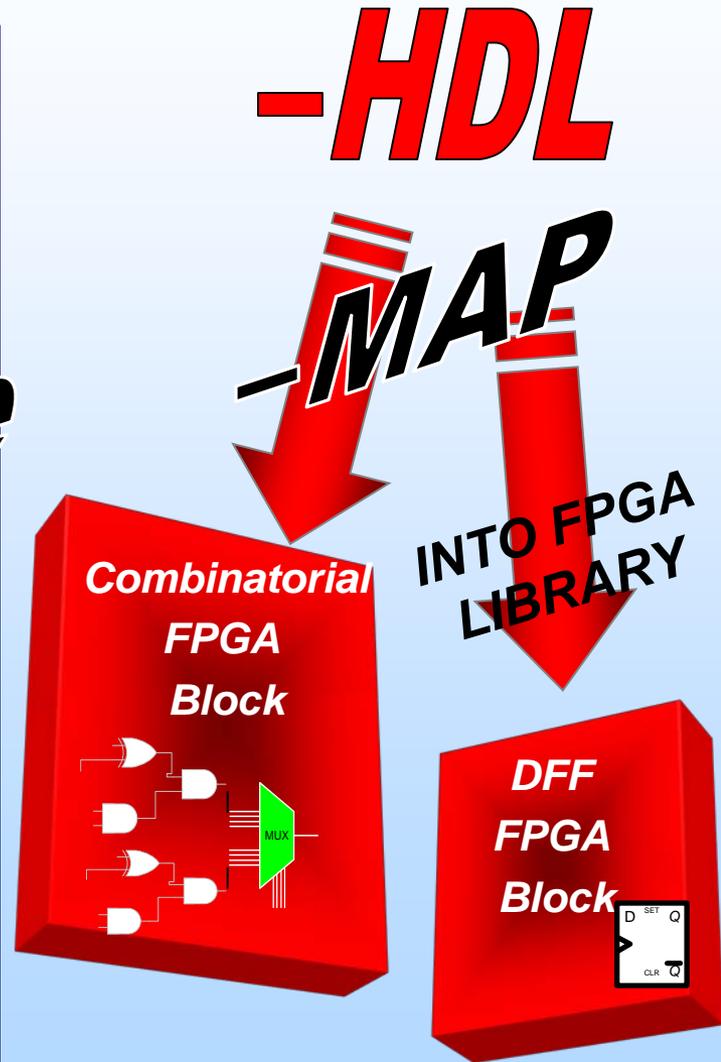
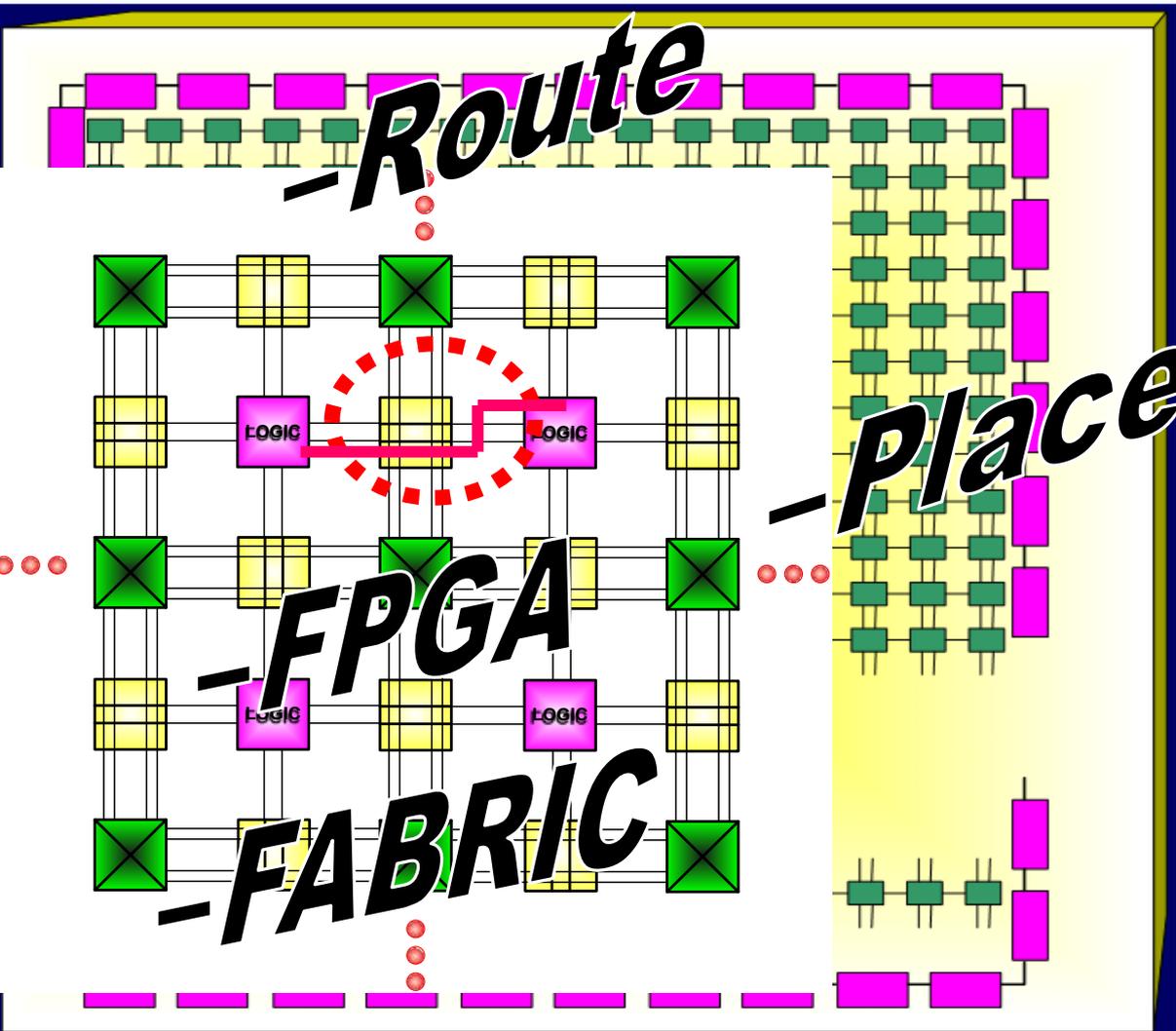
# Intro: Field Programmable Gate Array (FPGA)

## FABRIC – System On A Chip (SOC)



***User creates a design by configuring pre-existing logic blocks and routes.***

# FPGA Building Blocks: How Gates and Routes Are Utilized in FPGA Fabrics



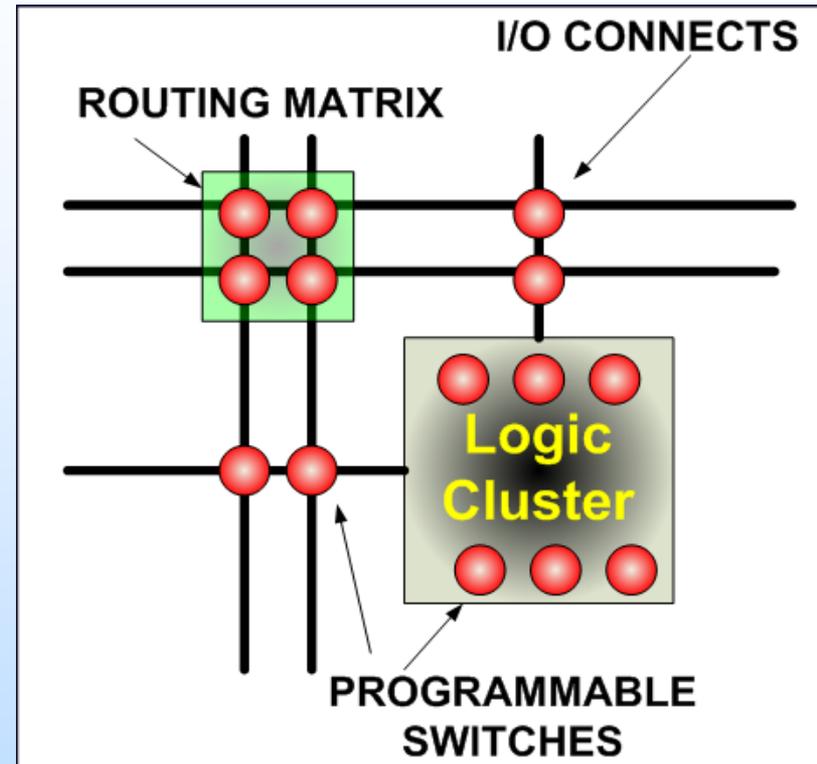
# Place, Route, and Gate Utilization are Stored in the FPGA Configuration

- **Configuration Defines:**

- **Functionality (logic cluster)**
- **Connectivity (routes)**
- **Placement**

- **Configuration Switch Types:**

- **Antifuse:** One time Programmable (OTP)
- **SRAM:** Reprogrammable (RP)
- **Flash:** Reprogrammable (RP)



# FPGAs and Single Event Effect (SEE) Susceptibility

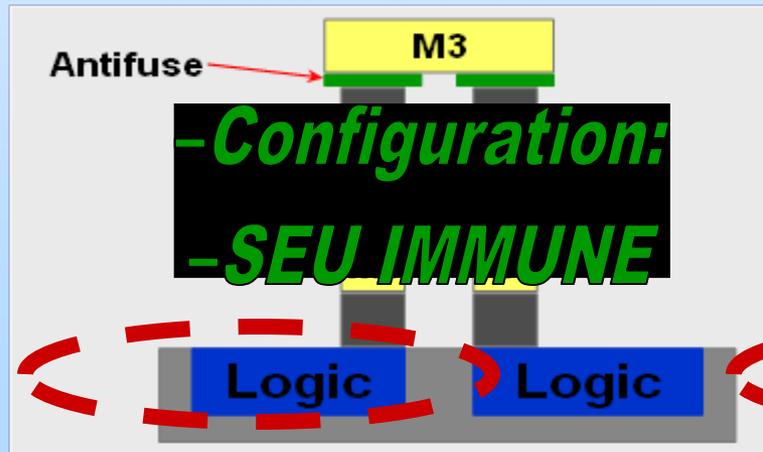
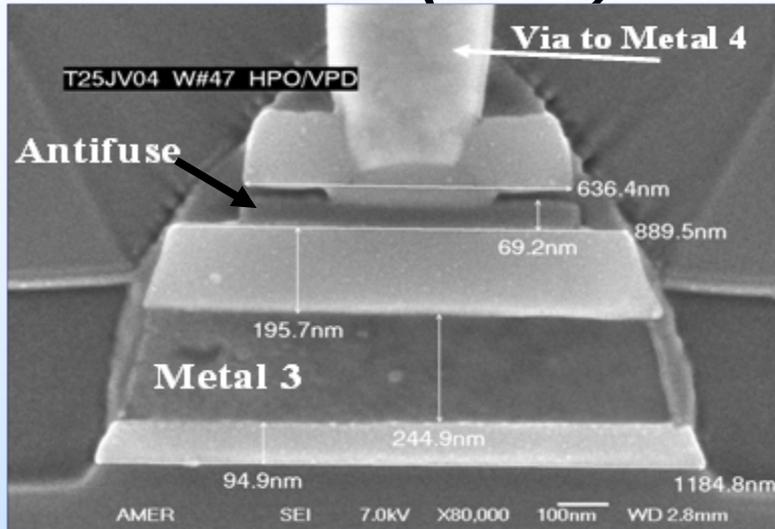


- We will only address the susceptibility of the 2 basic technology nodes of a FPGA device:
  - Configuration
  - Functional logic Blocks/routes
- Configuration and Functional logic are different technology nodes with different SEE upset rates
- Functional blocks can vary in susceptibility:
  - Fanout
  - Unused (don't care) logic
  - Highly capacitive routing matrices
  - Frequency of operation
  - Data pattern
  - Levels of functional blocks between flip flops (DFFs)

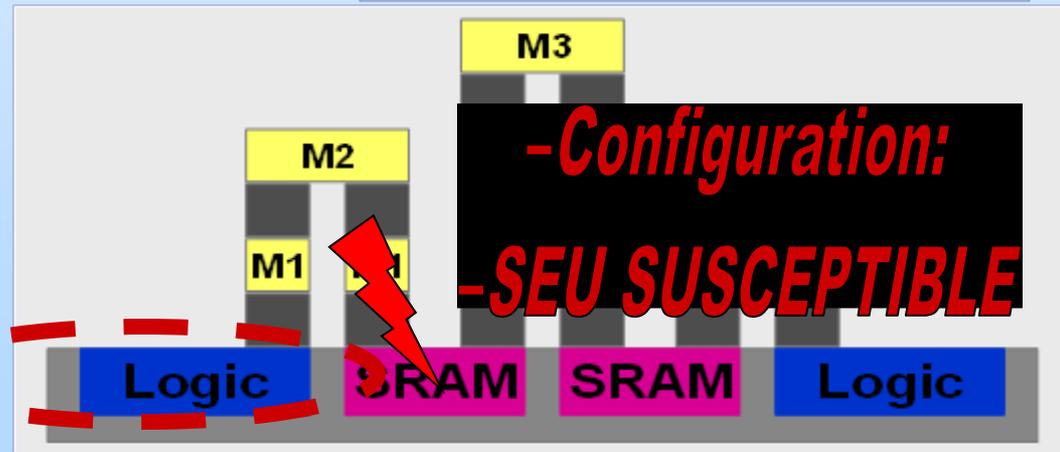
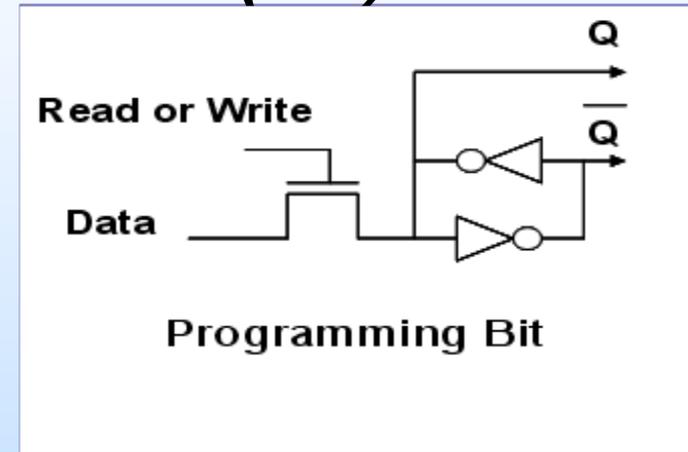
***Variation of technology, functional logic blocks, and complexity of utilization (SOC) make it no longer valid to simply count upsets during SEE testing***

# Configuration Switch Implementation and Single Event Upset (SEU) Susceptibility

## ANTIFUSE (OTP)



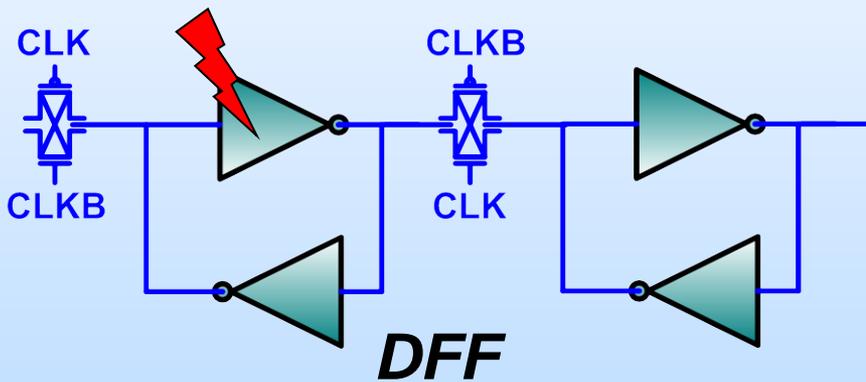
## SRAM (RP)



# Logic Building Block SEU and SET Susceptibility

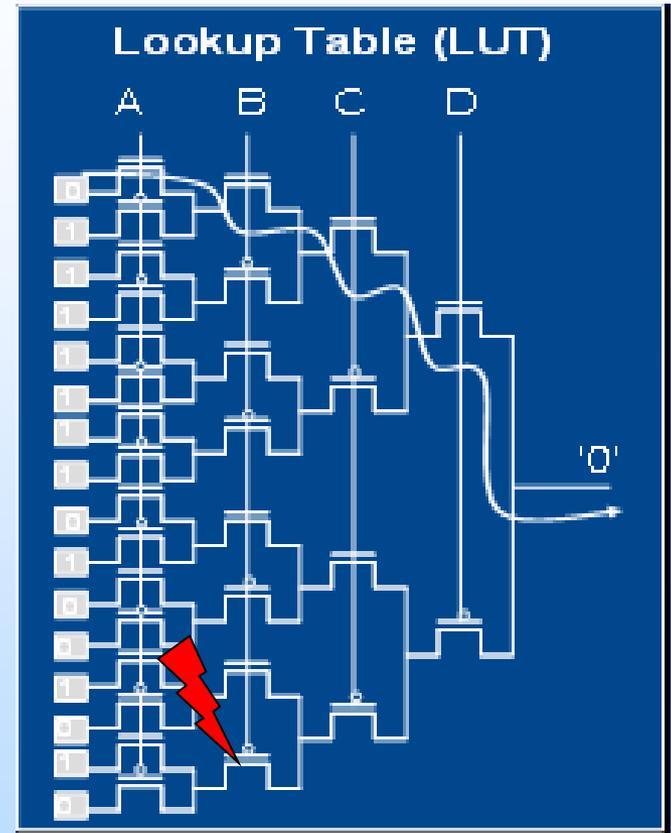


- Logic Blocks
  - Flip-Flops (DFFs)
  - Combinatorial Logic
  - Global Routes (clocks and resets)
  - Custom internal circuitry



**SEU**

**Not Frequency  
dependent**



**Xilinx combinatorial logic**

**SET**

**Frequency dependent**

# Putting It All Together...FPGAs (SEE) Susceptibility



$$P(fs)_{error} \propto P_{Configuration} + P_{functionalLogic} + P_{SEFI}$$

*Design Specific SEE upset rate*      *Configuration SEE upset rate*      *Functional logic SEE upset rate*      *Single Event functional Interrupt*

$P_{DFFSEU} + P(fs)_{SET \rightarrow SEU}$

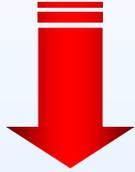
*SET must get captured and become an SEU*

**Must Clearly state which SEE type is being evaluated... Beware... sometimes difficult to differentiate**



# General SEE Testing Techniques

## SEE Test Strategy



*Different Technology*



## Configuration

- Static
- **NOT** performed for Anti-fuse FPGA
- Read Back SRAM or Flash

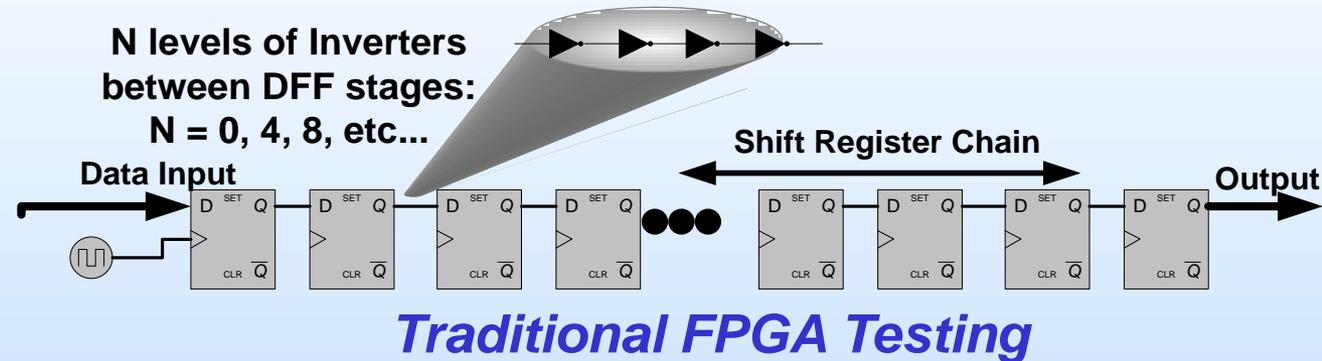
## Functional Logic

- Generally dynamic testing is required
  - DFFs and Combinatorial
  - SEFIs: Global Routes (clocks and resets)
  - SEFIs: Custom internal circuitry
- Logic blocks vary per FPGA



# FPGA Design Under Test Development

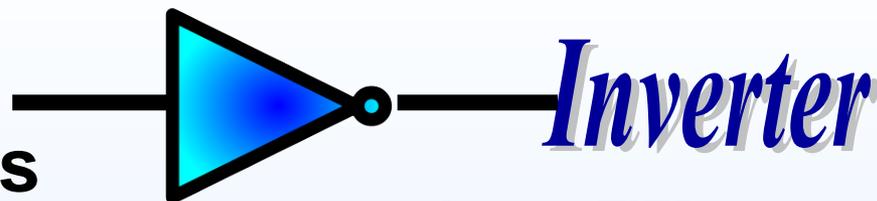
- Create FPGA designs that repeat blocks to increase statistics
- Create FPGA designs that exercise and hence expose building blocks



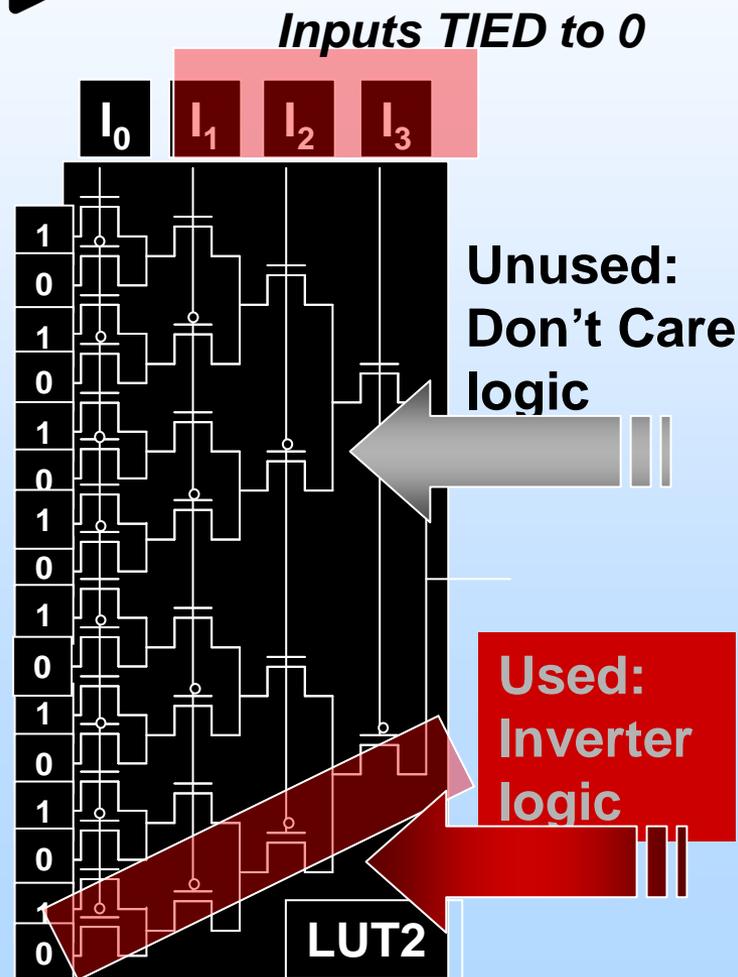
- Divide and conquer... Determine separate error cross sections that correspond to specific:
  - Frequencies
  - Designs and Building blocks (when applicable)

***No one cross section or “bit-error rate” applies to an FPGA***

# Some Questions That Have Driven REAG FPGA Test Strategy and Development



- Are shift registers designs sufficient to expose logic level susceptibility?
  - Fanout is linear
  - Can only use inverters or buffers
- How does frequency impact SEU error cross sections
- Global route SEFI considerations
- Configuration Correction Schemes (Scrubbing)





# FY10: FPGAs (Continuation)

## Description:

The main goal of this task is to investigate FPGAs from various vendors and to determine applicability for the space radiation environment. The following is a more detailed list of task goals.

- Determine inherent radiation sensitivities of advanced complex commercial CMOS (<100 nm) and hardened FPGAs
- Provide guidance on radiation test and qualification procedures
  - As a consultant
  - Test and analysis FPGA guideline development
- Determine SEU sensitivities for hardening approaches
- Comparison of fault injection versus beam SEU coverage
- Evaluate low proton energy sensitivity of commercial CMOS FPGAs (Low Energy test methodologies are discussed in detail in another task)

## FY10 Plans:

### Probable Test Vehicles:

- Achronix/BAE Hardened Asynchronous FPGA RADRunner
- Achronix Commercial Asynchronous FPGA SPD60
- Spartan 6 (45nm SRAM-Based)
- Actel RTAX2000s FPGA (150nm Anti-fuse Based)
- Actel ProASIC FPGA (130nm Flash-based)

### -Other Work:

- Support of Crypto space evaluation of Actel RTAX-S (90nm)
- Develop guideline for interpreting FPGA SEE data

## Schedule:

- Will be presented on separate slides due to number of tasks

## Deliverables:

- Test reports and quarterly reports
- Expected submissions to SEE Symposium, MAPLD, and IEEE RADECS. DTRA to review prior.

## NASA and Non-NASA Organizations/Procurements:

- Beam procurements: TAMU, IUCF, UC Davis,  
- Possible use of Berkeley Facility

## Partners:

Xilinx, BAE, Achronix, NRL, Actel

**Principle Investigator: GSFC-MEI/ Melanie Berg**

**Other participants: GSFC-MEI/Hak Kim, Mark Friendlich, Chris Perez, Anthony Phan, Tim Irwin, Christina Seidlick**



# Goals

- **Enhance current FPGA designs under test**
- **Determine Functional Operation Susceptibility:**
  - How often does the operation upset
  - Must perform dynamic tests
  - Great FPGA to FPGA comparison point
- **Determine Configuration Susceptibility for:**
  - Xilinx Virtex Family FPGAs
  - Xilinx Spartan Family FPGAs
  - ProASIC Flash FPGAs
- **Application of upset rates:**
  - Determination of dominating SEE upset rates per FPGA type
  - The role of mitigation to upset rates



# Expected Impact to Community

- **Tests are created so that SEE characterization of various FPGA devices can be compared for project device selection**
- **All test enhancements and considerations provide alternate/independent perspectives for SEE FPGA characterization**
- **Results are expected to obtain more accurate error prediction rates because device is tested and evaluated under closer to realistic circumstances**
  - **Distinction of configuration and system error rates**
  - **Frequency variation and SET evaluation**
  - **Design Complexity**
  - **Functional state space coverage distinction**



# **Highlights/Accomplishments: Lessons Learned : Actel Radiation Hardened Anti-fuse FPGA**

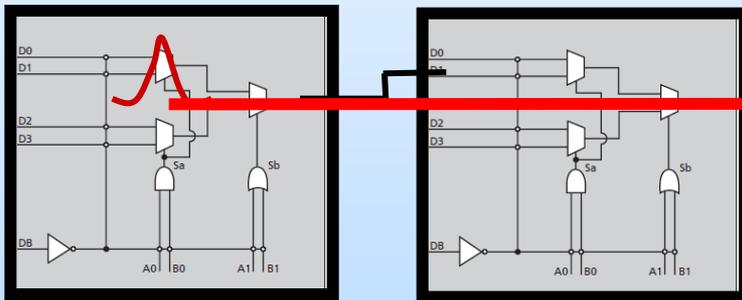


# Radiation Hardened Anti-fuse Susceptibility and Mitigation

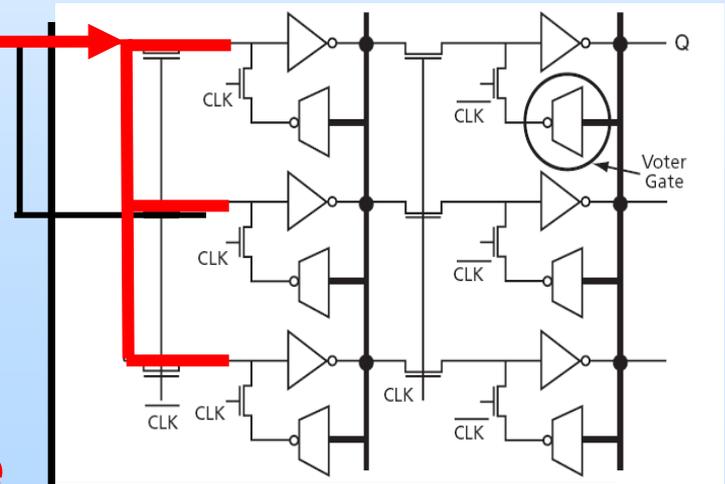
$$P(fs)_{error} \propto P_{Configuration} + P_{functionalLogic} + P_{SEFI}$$

**Design Specific SEE upset rate**     
 **Configuration SEE upset rate**     
 **Functional logic SEE upset rate**     
 **Single Event functional Interrupt**

$$P_{DFFSEU} + P(fs)_{SET \rightarrow SEU}$$



**Combinatorial logic cells**



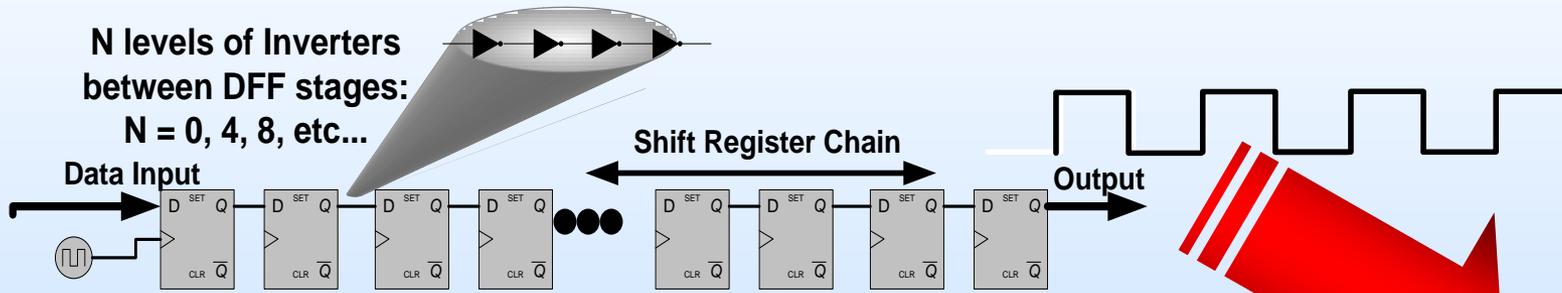
**DFF**

**Triple DFFs lower  $P_{DFFSEU}$  but can not mitigate  $P(fs)_{SET \rightarrow SEU}$  (upset rate in order of Millenniums)**

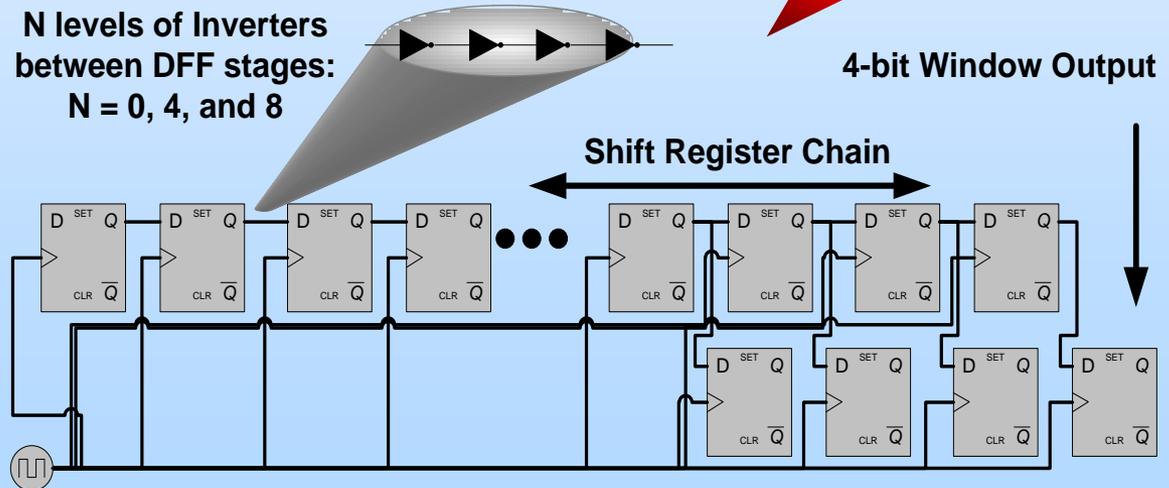
# The Predominance of $P(fs)_{SET \rightarrow SEU}$ Requires High Frequency Testing And An Architecture Enhancement



- **Shift Register Enhancement: REAG Windowed Shift Register (WSR) for High Speed Signal Integrity**



**Traditional**



**WSR**



# The WSR Advantage: Static Output

Last 4 bits of shift register. They are shifted into the window every 4 clock cycles

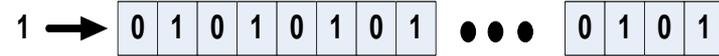
Clock Cycle

Hex A



N

Hex 5



N+1

Hex A



N+2

Hex 5



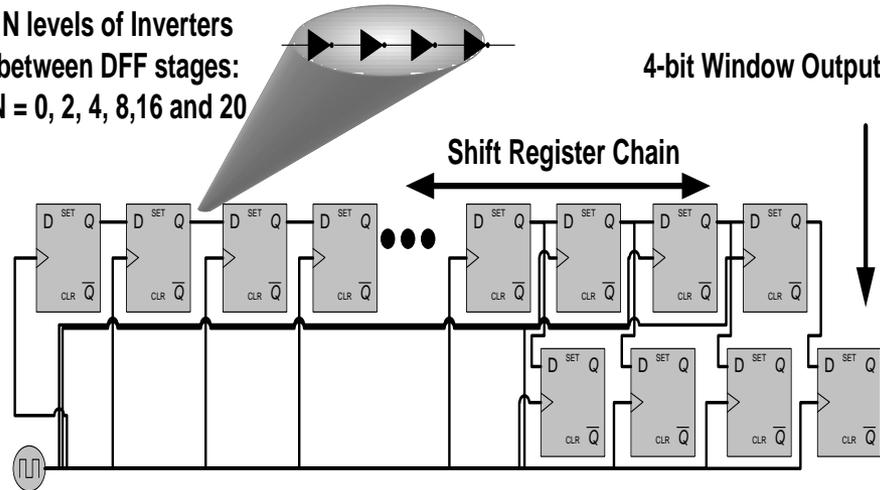
N+3

Hex A



N+4

N levels of Inverters between DFF stages:  
N = 0, 2, 4, 8, 16 and 20



Shift Register Chain

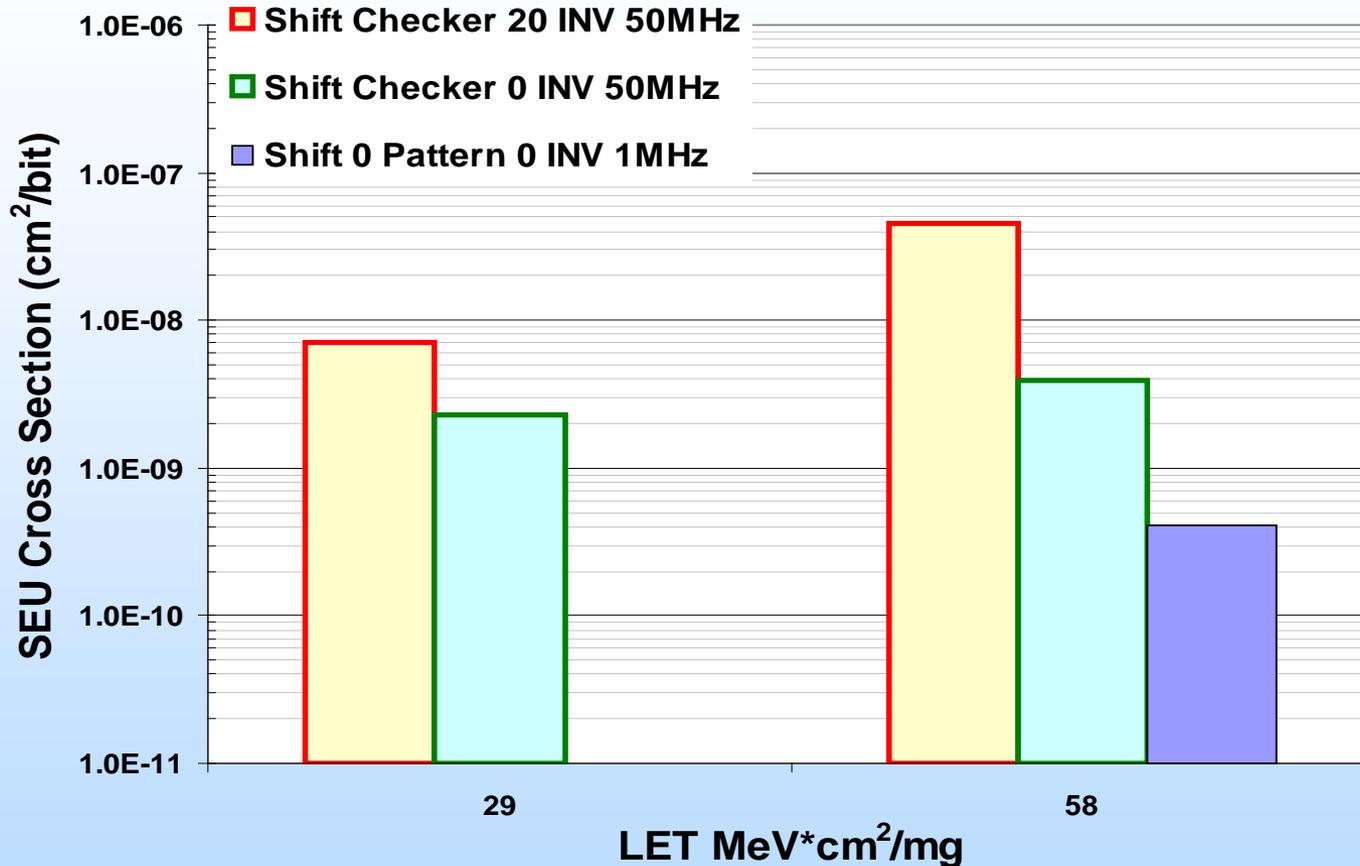
4-bit Window Output

REAG WSR

**Static output enhances signal integrity**



# Design and Frequency Impact to SEE



***Low frequency static data pattern with low frequency clock has a  $LET_{th} > 30 \text{ MeVcm}^2/\text{mg}$ ... much higher than other architectures at other frequencies***



# Highlights/Accomplishments: REAG WSR SEE Results

- Error rates are significantly dependent on Threshold  $LET_{th}$
- Choice of design impacted  $LET_{th}$
- Choice of data pattern and frequency of operation impacted  $LET_{th}$  (>2 orders of magnitude)

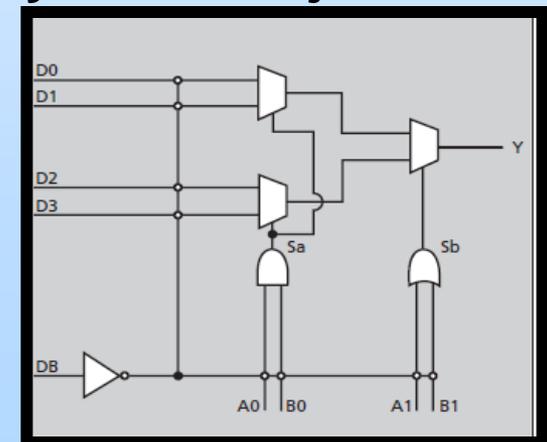
	Low Frequency	Increased Frequency
$LET_{th}$ MeV*cm <sup>2</sup> /mg	$LET_{th} >37$	$8 < LET_{th} < 30$
Bit Error Rate (errors/bit-day)	$dE_{bit}/dt \approx 1 \times 10^{-10}$	$1 \times 10^{-10} < dE_{bit}/dt < 5 \times 10^{-8}$

**If Frequency or data pattern were not varied during testing, then an incorrect  $LET_{th}$  and  $dE_{bit}/dt$  would have been calculated**

# Considerations when Developing a Complex Design under Test Architecture



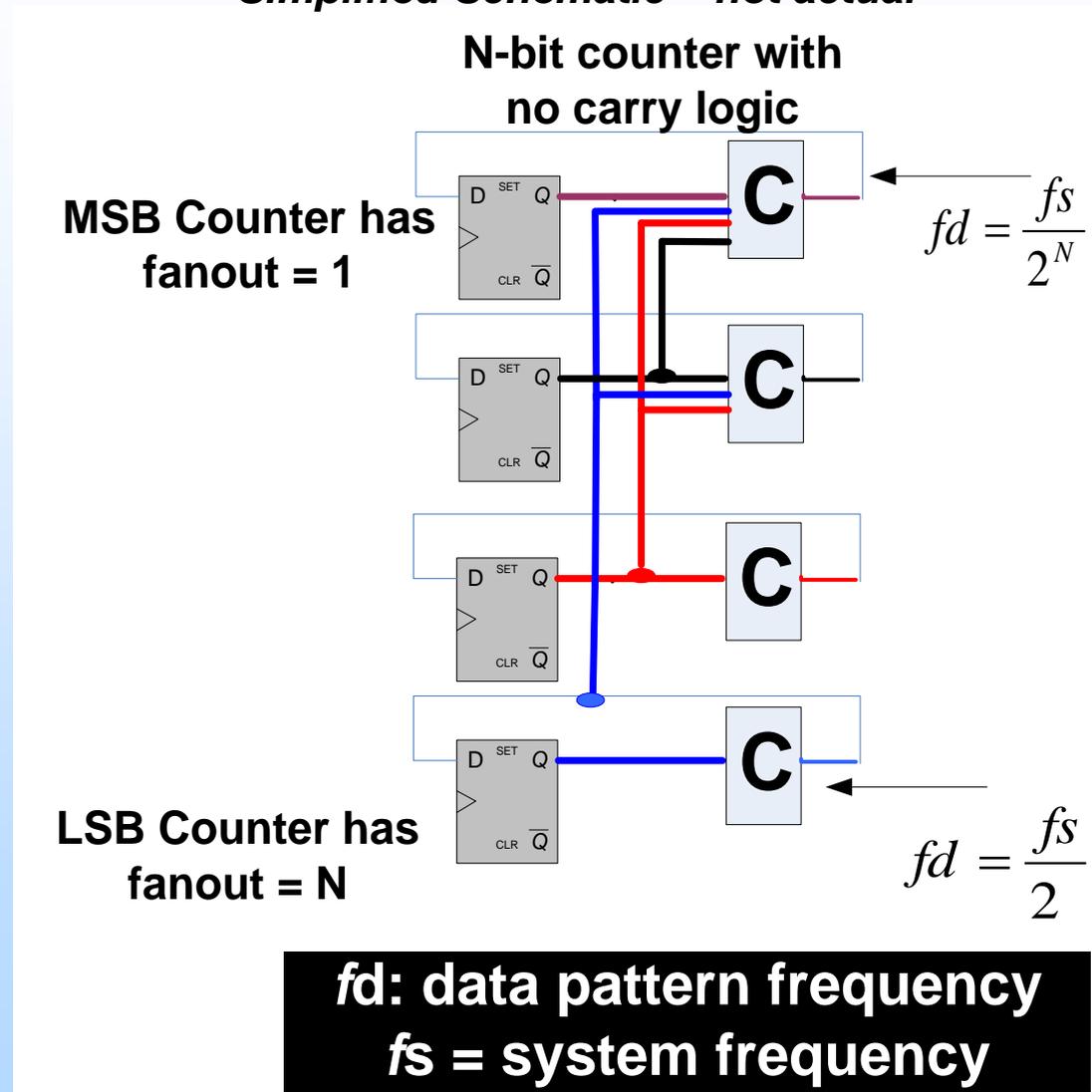
- **Are inverters efficient test structures?**
- **Want to investigate something more realistic than a shift register**
  - **It should have the characteristics of a complex design with:**
    - fan-out and fan-in > 1
    - contains a mixture of sequential and combinatorial logic.
  - **The circuit should be replicated to increase statistics.**
  - **Its state space can be traversed within relatively short time periods such that all states are equally likely to be subject to particle strikes during radiation testing.**



# Counters Meet Requirements

*Simplified Schematic – not actual*

- Has characteristics of a complex design with:
  - fan-out and fan-in > 1
  - contains a mixture of sequential and combinatorial logic.
- Variety of data pattern frequencies ( $f_d$ )
- State space Traversal =  $2^N/f_s$





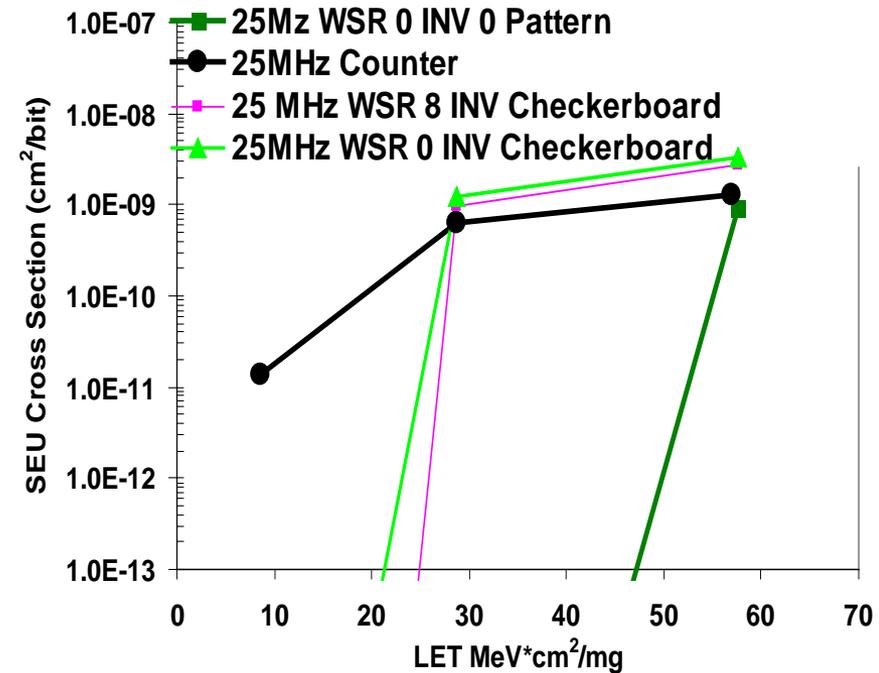
# Highlights/Accomplishments: Texas A&M Heavy Ion Results Counters versus WSRs

- Checkerboard (CB) 8 inverter (INV) chains  $\approx$  0 INV chains at 25 MHz.
- However, as demonstrated in 2004 data, there is a significant difference in cross sections at higher frequencies.
- 24 bit counter cross section is similar to CB WSR:

–  $1 \leq \#CCells \text{ Levels} < 8$

– Data pattern of counter varies per bit

$$\frac{f_s}{2^N} \leq f_d \leq \frac{f_s}{2}$$



**25MHz Counter LETth is lower than 25MHz WSR but similar to 100MHz CB WSRs**

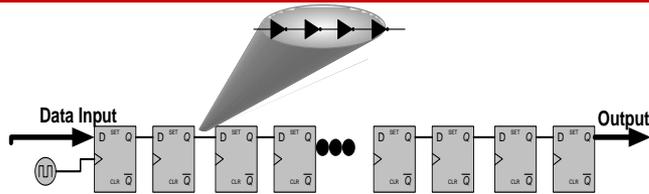
# REAG Evolution of FPGA Designs Under



## Test

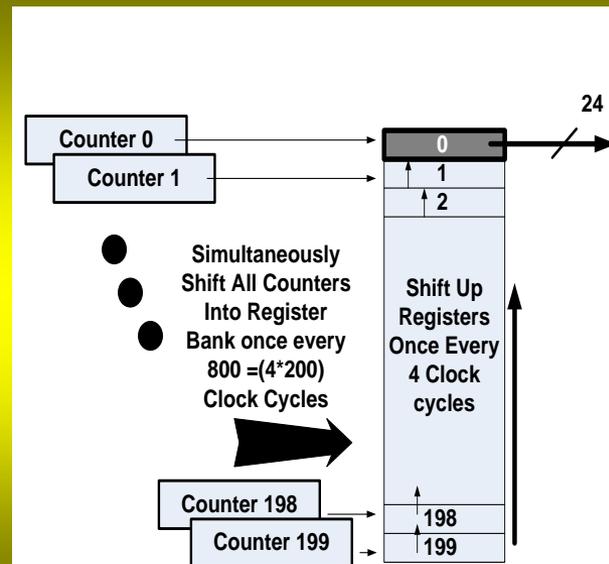
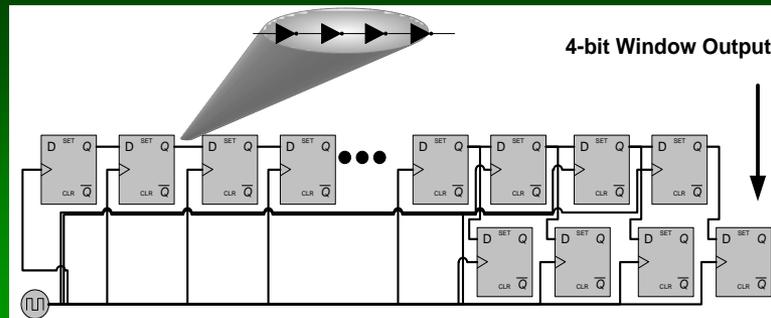
*Traditional Shift Register Testing with addition of Combinatorial logic*

*All Designs are used for all FPGA dynamic tests*



*WSRs: High Speed Signal Integrity*

*Counter Arrays: More Realistic testing... not meant to replace WSRs – just an enhancement*





# **Highlights/Accomplishments: Lessons Learned: SRAM Based FPGAs... Xilinx Virtex Series**



# SRAM Configuration Susceptibility vs. Functional logic Susceptibility:

- For non-mitigated designs, Consortium data shows that configuration upsets are most significant

$$P_{system} \propto P_{Configuratoin}$$

	Probability	Error Rate	LEO	GEO
<i>Xilinx Consortium: VIRTEX-4VQ STATIC SEU CHARACTERIZATION SUMMARY: April/2008</i>			<i>Upsets</i>	<i>Upsets</i>
			<i>device – day</i>	<i>device – day</i>
<b>Configuration Memory: XQR4VSX55</b>	$P_{configuration}$	$\frac{dE_{configuratoin}}{dt}$	7.43	4.2
<b>Combined SEFIs per device</b>	$P_{SEFI}$	$\frac{dE_{SEFI}}{dt}$	$7.5 \times 10^{-5}$	$2.7 \times 10^{-5}$

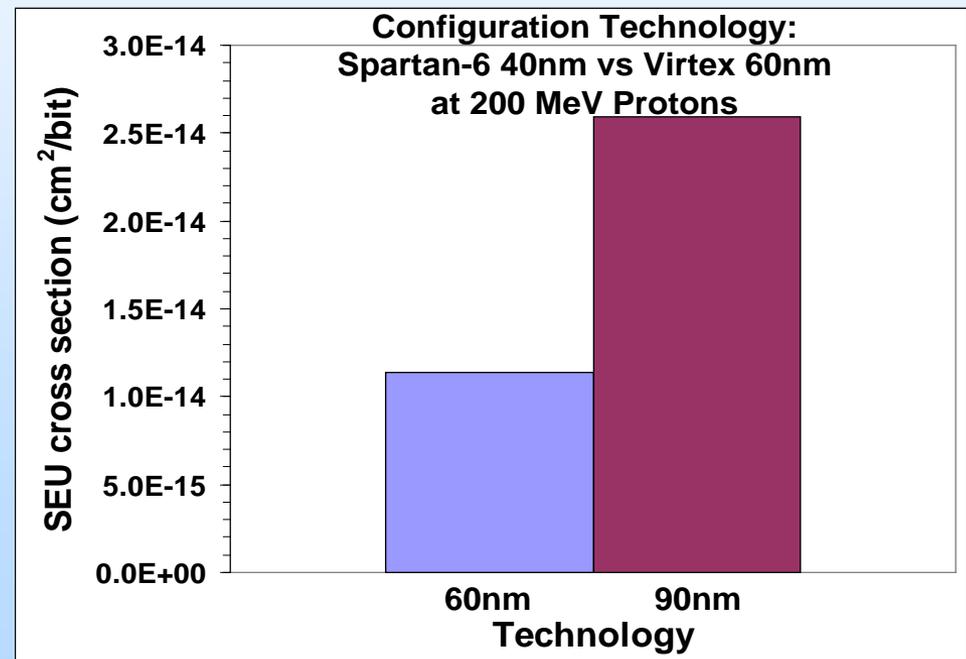
**REAG Investigation: How does Configuration upsets scale with technology and how does mitigation (redundancy + scrubbing) impact configuration upset rates**



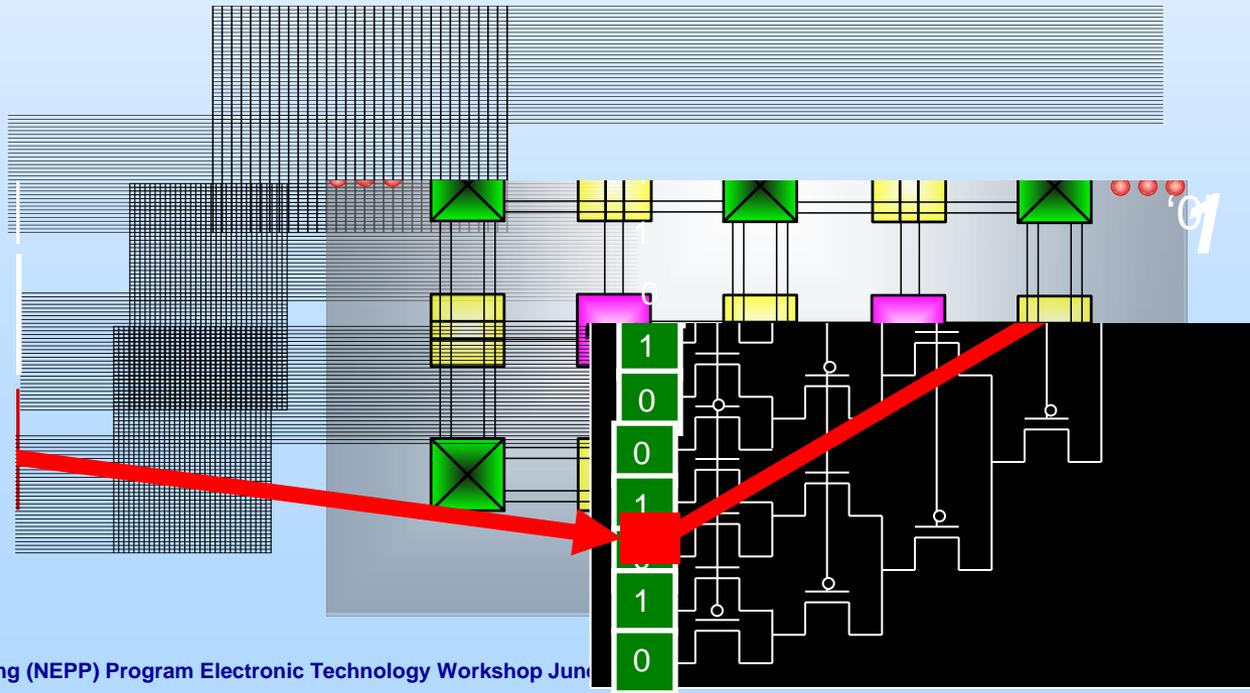
# What have we learned: SRAM Configuration Testing

- Configuration was tested by reading back memory after irradiation (static testing):
  - Fluence had to be significant to generate enough errors for proper statistics
  - No Scrubbing

- On our way to UC Davis for Spartan-6 low energy proton testing... Direct ionization investigation



**Technology Scaling: Spartan-6 has a reduced cross section at 200MeV Protons than the Virtex-5**



# Scrubbing and Accelerated SEE Dynamic Testing

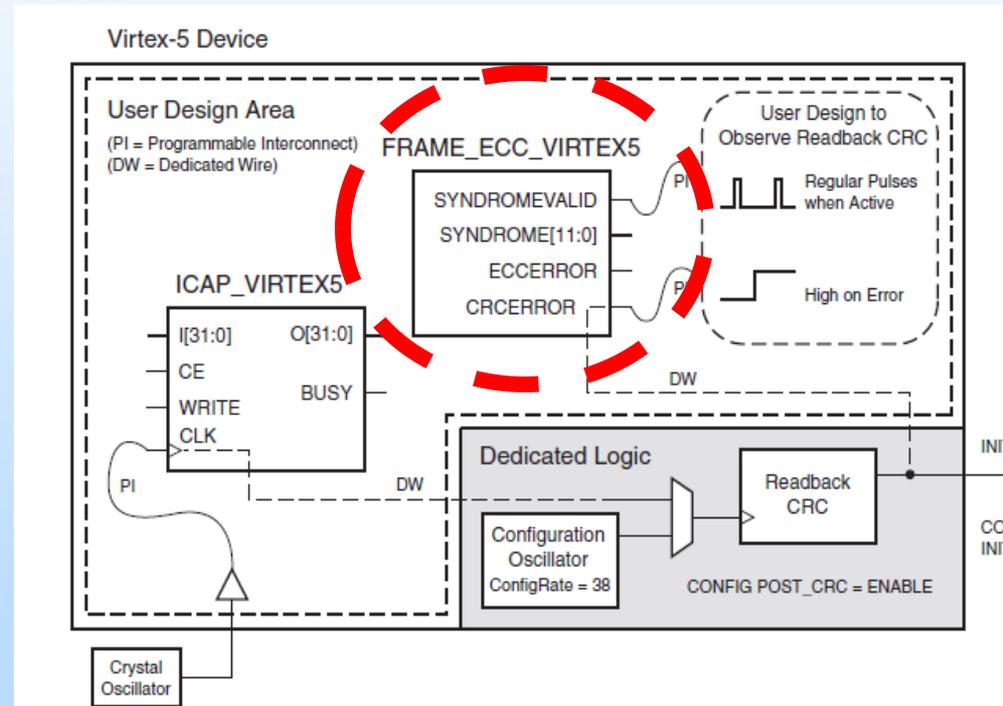


- **First...Find bit upset rate of configuration memory (static)**
- **Dynamic tests:**
  - **Scrubbing doesn't help non-mitigated functionality**
  - **Scrubbing + mitigation tests very well**
- **Scrub Configuration faster than configuration bit upset rates**
- **Various methods of scrubbing:**
  - **Blind full scrub**
  - **Readback+internal Xilinx circuitry (Frame ECC+ SCTLR)**
  - **Readback invoked full scrub**
  - **With accelerated testing – blind scrubbing is the fastest is the most efficient - can test with higher flux**

# Caution: Utilization of Xilinx Internal Circuitry for Scrubbing



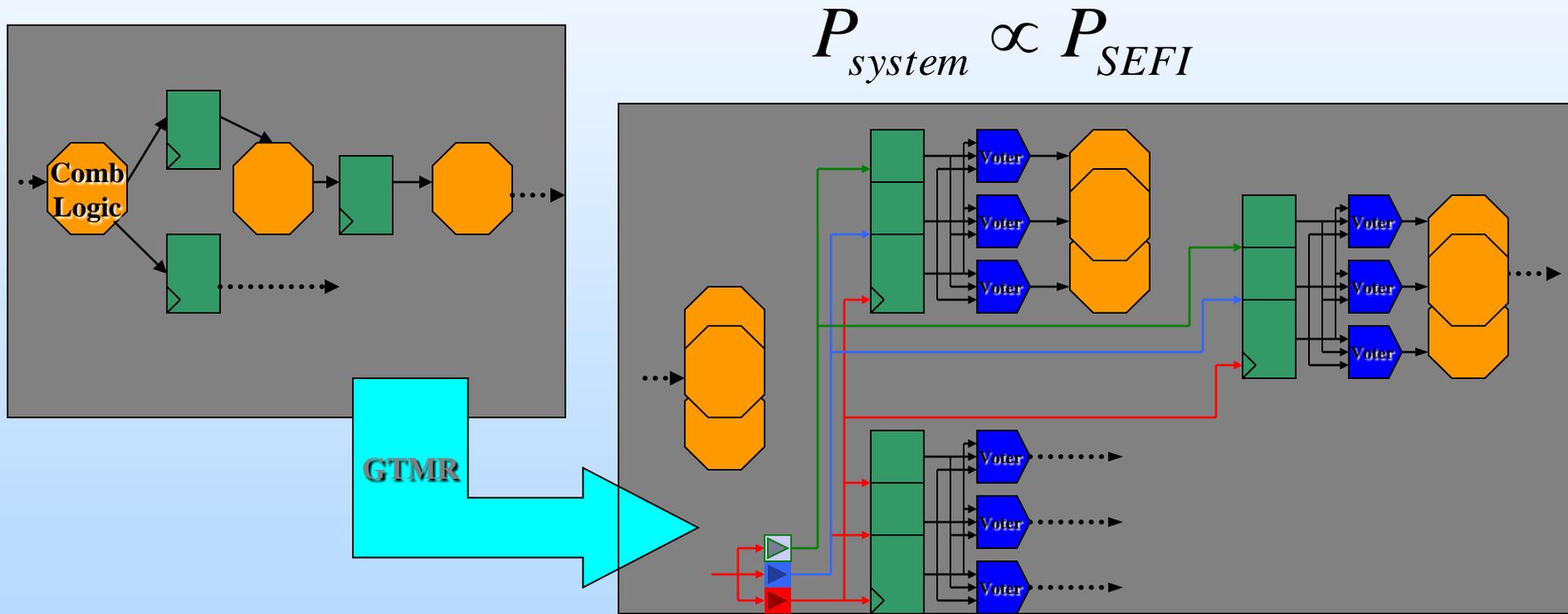
- Special embedded logic used to correct configuration
- Logic is unprotected (non-mitigated)
- When embedded logic is upset:
  - Can write bad frames
  - Can stop working
- Custom internal mitigated scrubbers (or external scrubbers) work best.



***Best to bypass Xilinx embedded non-mitigated Scrubbing Logic***

# Xilinx SRAM Error Prediction with Proper Scrubbing + Mitigation

- When using Scrubbing + Global Triple Modular Redundancy (GTMR or XTMR), the most significant upset rate Reduces to  $P_{SEFI}$ .
- SEFI rate is in the order of a Millennium



**Proper implementation of Mitigation can reduce the upset rate from days to Millenniums .**

# PLANS FOR FY10/11



- **Actel RTAX-s**
  - **Technical plans**
    - May or June 2010 Heavy Ion Testing
    - Hone in on LET<sub>th</sub> of the WSRs, counters, and memory modules
  - **Deliverable plans**
    - Update and release current Test Report (July 2010)
    - RADECs paper submission (04/01/2010)
    - SEE presentation (04/2010)
- **Actel RT ProASIC (Flash Based FPGA configuration)**
  - **Technical plans**
    - Heavy Ion and Proton Testing end of FY10
    - WSRs, counters, and memory modules (similar to RTAX-s)
  - **Deliverable plans**
    - Currently in discussion

# PLANS FOR FY10/11

## Continued



- **Xilinx Spartan 6**
  - **Technical plans**
    - Heavy Ion and low energy Proton Testing end of FY10
    - WSRs and counters with and without mitigation
  - **Deliverable plans**
    - Indiana University -Proton Test Report 04/2010
- **Achronix RadRunner**
  - **Technical plans**
    - Laser Testing 5/2010
    - WSRs, counters, and embedded memory
  - **Deliverable plans**
    - Depends on test completion

# SCHEDULE



	Microelectronics	2009			2010								
	T&E	O	N	D	J	F	M	A	M	J	J	A	S
Actel RTAX-s	On-going discussions for test samples												
	Radiation Test Development and Testing												
	Data Evaluation and Test reports												
	Paper Submission												

TBD waiting for Vendor DUT design

# Schedule



		2009			2010								
		O	N	D	J	F	M	A	M	J	J	A	S
BAE/ Achronix FPGA	On-going discussions for test samples												
	Radiation Test Development												
	Test Devices and reports												
	Paper Submission												



# Schedule

		2009			2010								
		O	N	D	J	F	M	A	M	J	J	A	S
Achronix FPGA	On-going discussions for test samples												
	Radiation Test Development												
	Test Devices and reports												
	Paper Submission												



# Schedule

		2009			2010								
		O	N	D	J	F	M	A	M	J	J	A	S
	<b>Microelectronics</b>												
	<b>T&amp;E</b>												
Spartan6	On-going discussions for test samples												
	Radiation Test Development												
	Test Devices and reports												
	Paper Submission												

# Schedule



		2009			2010								
		O	N	D	J	F	M	A	M	J	J	A	S
Actel ProASIC	On-going discussions for test samples												
	Radiation Test Development												
	Test Devices and reports												
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