



Challenges of Developing Qualification Methods for DDR Class Devices – Part 2

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Outline

- Reliability Concerns...
- Qualification Approach
- Test/Operational Concerns
- Hardware Development
- Test Efforts & Plans
- Conclusion



From TID to General Reliability

- TID is interested in mechanisms that are impacted by charge generation
- General reliability is interested in the failure modes that will manifest as a result of any environment, age, or usage parameters
- But manufacturers devote significant resources to testing these devices – why do we need to test, and how are we different?
 - Certain parameters of NASA use may be outside of standard usage – long life, extreme environments, off-spec sheet use...
 - We need to be knowledgeable about running these devices to support program questions

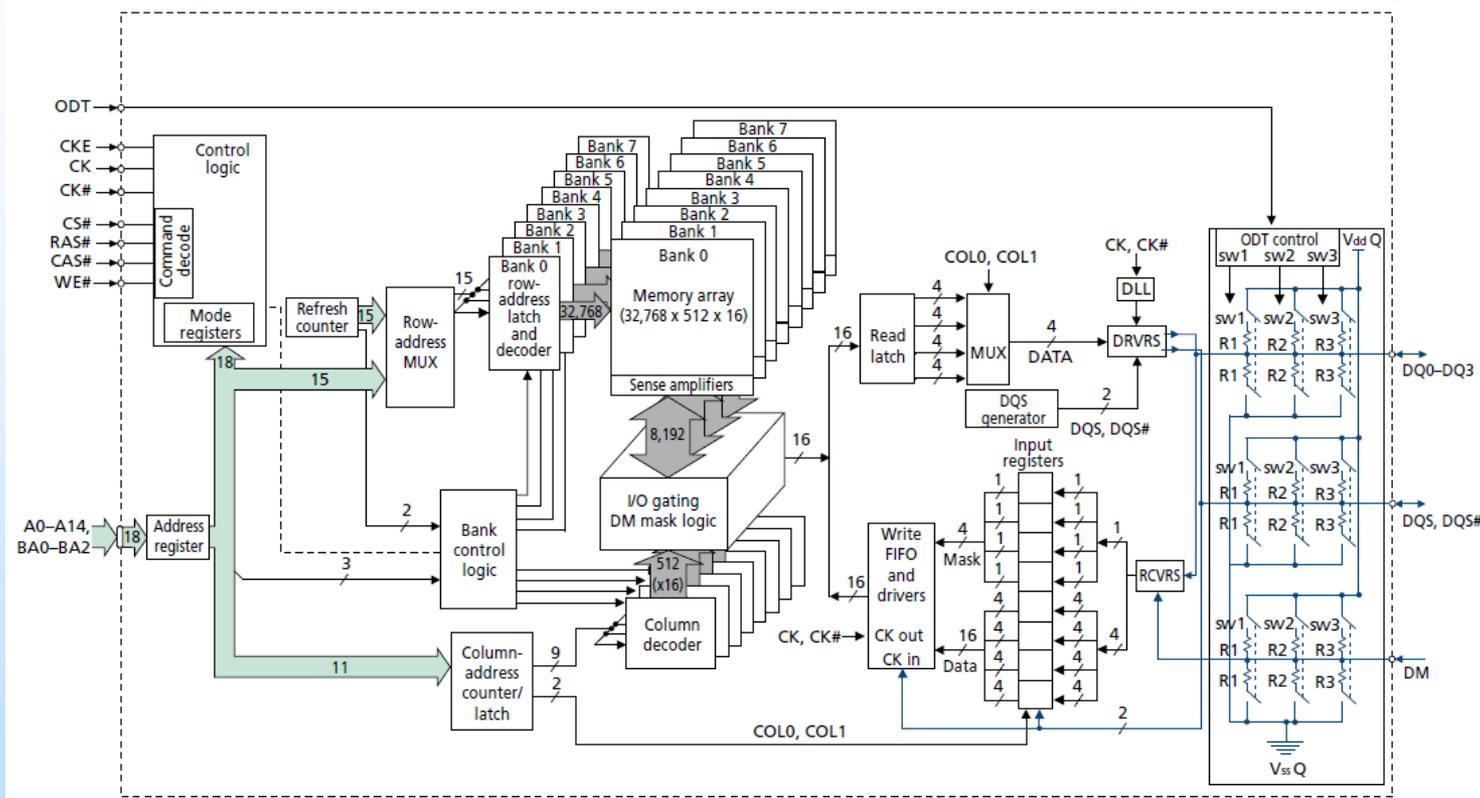


Reliability concerns

- TDDDB - time dependent dielectric breakdown
 - parameters: T, E field
- HCI – hot carrier injection
 - parameters: Current, # of bias switches
- Electromigration –
 - parameters: Current, Temperature, Activation Energy
- NBTI – negative bias temperature instability
 - parameters: E field, # of switches
- Test key is to try to hit as many reliability concerns with a minimal test matrix



Impact of Device Complexity



- Many different types of structures:
 - DRAM Cells, Registers, Buffers, Drivers, Voltage Regulators, Charge Pumps, Functional blocks: CRC, Pipelines, State Machines
 - Each has its own failure risk and parameter dependencies



Test Matrix

$$X(p, M, F(t), Pat(t), V, T, f, D, S(t)) = \begin{cases} Pass / Fail \\ Range \\ Limit \\ \# Counts \end{cases}$$

- General reliability testing covers a vast set of target parametrics and operating parameters
 - p – parameter (e.g. data access time)
 - M – device mode
 - F(t) – device function during test
 - Pat(t) – data pattern during test
 - V – operating bias
 - T – environment temperature
 - f – clock rate
 - D – duty cycle
 - S(t) – stress history of device
- In addition:
 - # of test devices in sample
 - # of desired manufacturers
 - # of test lots

General reliability test matrix is intractable - it requires targeted selection of tested elements.



Qualification Challenges

- Establishing application usage requirements in concert with known device-type risks
- Using devices outside of the datasheet
 - Need to develop recommendations for both standard testing and derating needs
 - Failure mechanisms can be observed before they make a device fail a datasheet parameter
- Complex devices have many failure sources and modes - large test matrixes
- DDR devices are constantly changing



Qualification Approach I of II

- Device Selection
 - Generally plan on packaged devices unless a program is looking for a specific die/device
 - Target devices should include those of program interest as well as new RHBD/space grade devices such as Aeroflex, Boeing, SpaceMicro or others
 - Form factor may support loose devices and/or DIMMs



Qualification Approach II of II

- Establish test plan and take data
 - Depending on application and engineering goals, may need to develop parametric test capabilities specific for device
 - Set of environmental, bias conditions, and target test duration shall be set.
 - Utilize test setup to identify
 - First failures, leading parameter degradation, operational issues
- Reporting/Recommendations
 - Issue derating and usage guidelines
 - Prepare information for support of future program need and potential failure analysis



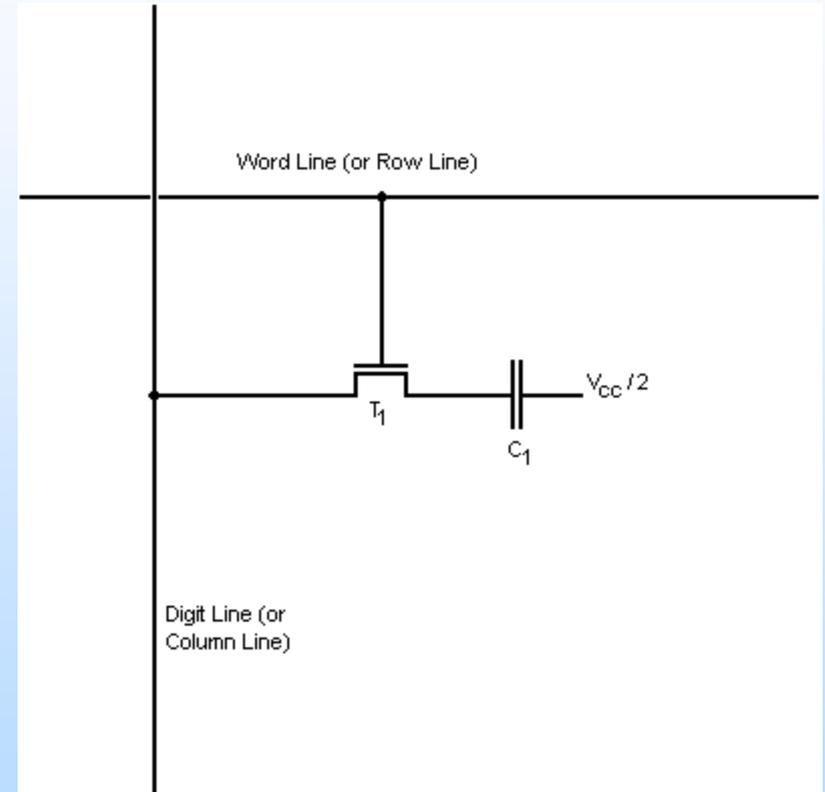
Testing Approach

- Testing many devices
 - Even after paring down, test matrix will be large
 - Will want 3 to 5 devices under each operating condition
- Testing different types of parameters
 - Data sheet timing parameters, bias levels, current draw under key operations
 - Non-data sheet parameters such as potential derating frequencies and refresh rates
- Life testing devices vs. Characterizing parameterics
 - Need constant functional operation during life testing
 - Will likely need to support 10+ simultaneous life test setups
 - Characterization will require more detailed operation than required during life-testing.



Example: DRAM Cell Biasing

- The worst case bias across the gate to storage cell requires frequent refresh and/or inverting data
- Once charged to V_{CC} or 0, C_1 begins to discharge through T_1
- Refresh restores(inverts) the bias on C_1
- Frequent refreshing provides the worst case for high-bias failure mechanisms
- Some mechanisms (like HCI) will be worse if the bias switches.





Leading Failures

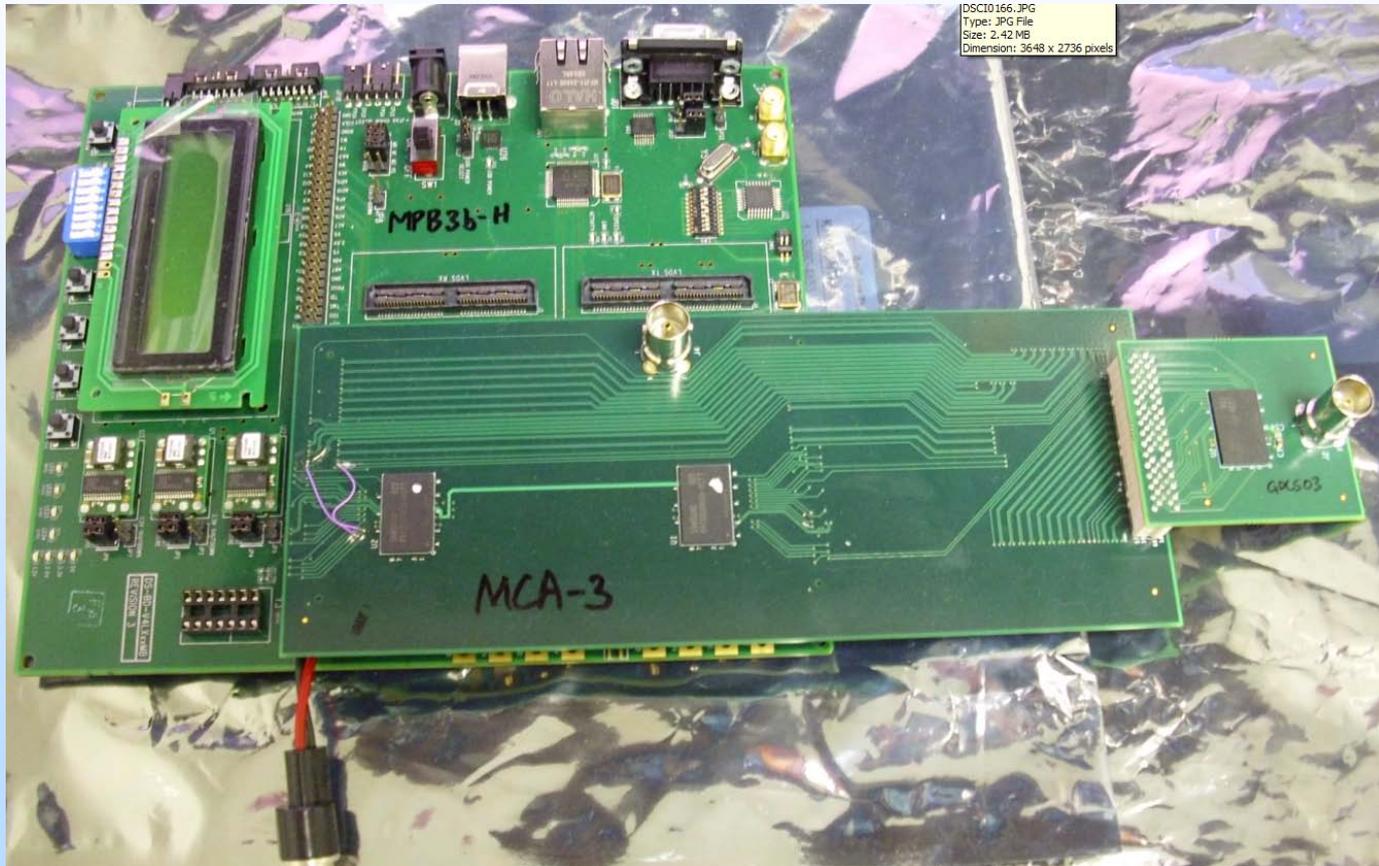
- Due to primarily targeting packaged devices, failure modes will be limited
 - Data errors
 - Decay in data storage capability (retention time or lost bits)
 - Modified operating bias
 - Changes in parameter ranges for operation
- Degraded performance may be difficult to link to a device structure
- Random Errors (degradation leading to reduced margin)
- Degraded Nodes (degradation leading to function loss)
- Reduced parameter-area of reliable operation
- Increased/altered device current draw



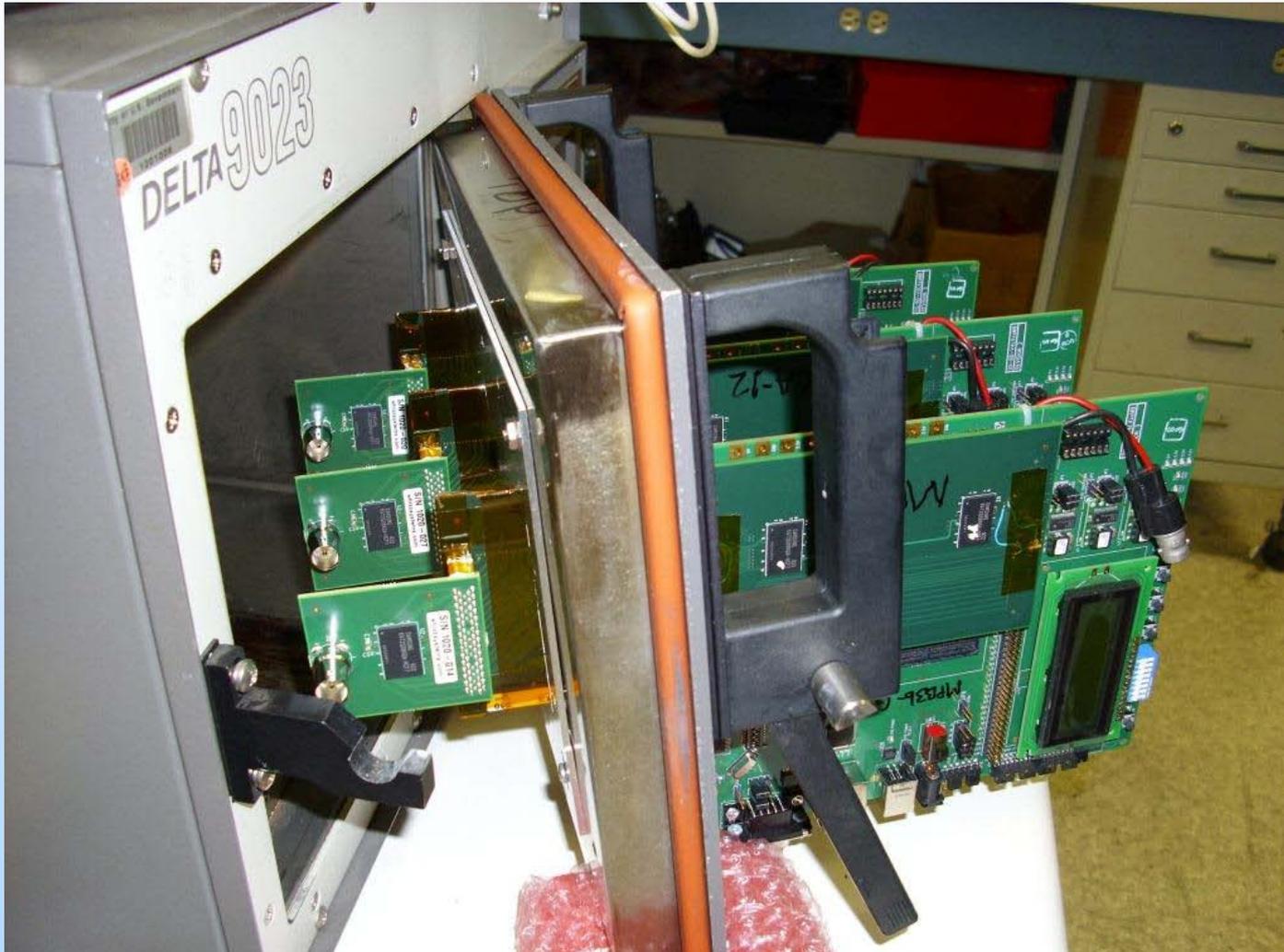
Test Hardware

- Supporting the following goals
 - General reliability testing
 - General project support
 - Flexible test capability to support off-spec-sheet testing
 - Interoperability to support NEPP-wide compatibility (including DIMM testing)
- Testing needs:
 - Individual part testing in small quantities
 - Targeting many data-sheet parameteric values
 - Test capabilities for many parts under life stress
 - Provide adequate operating conditions to achieve worst-case stress levels
 - Requires a couple complementary test setups
- Hardware directions:
 - Inexpensive expandable system for long life tests
 - Flexible and fast systems for full testing of key parameterics
 - Expanded compatibility of test hardware

Test Resources @ JPL



Test Resources @ JPL



Test Resources @ JPL



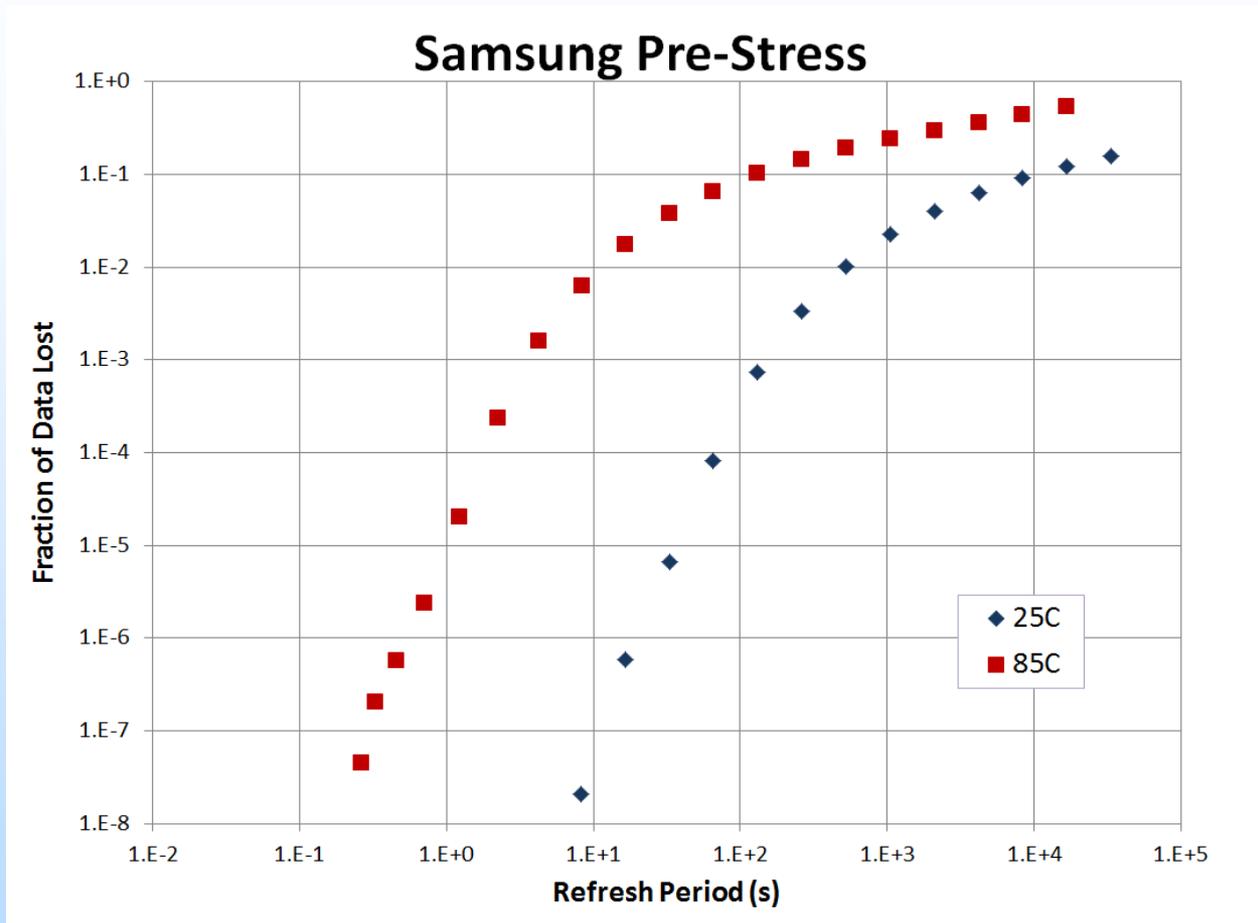
Test Resources @ JPL

- Credence D10 is a high-capability tester (up to 400MHz, adequate signal pins for DDR2)
- Part of a development plan to enable full parametric testing of individual devices
- Virtually no multi-part test capability (especially in key test environments)
- Life testing of devices will still require resources for operating many devices





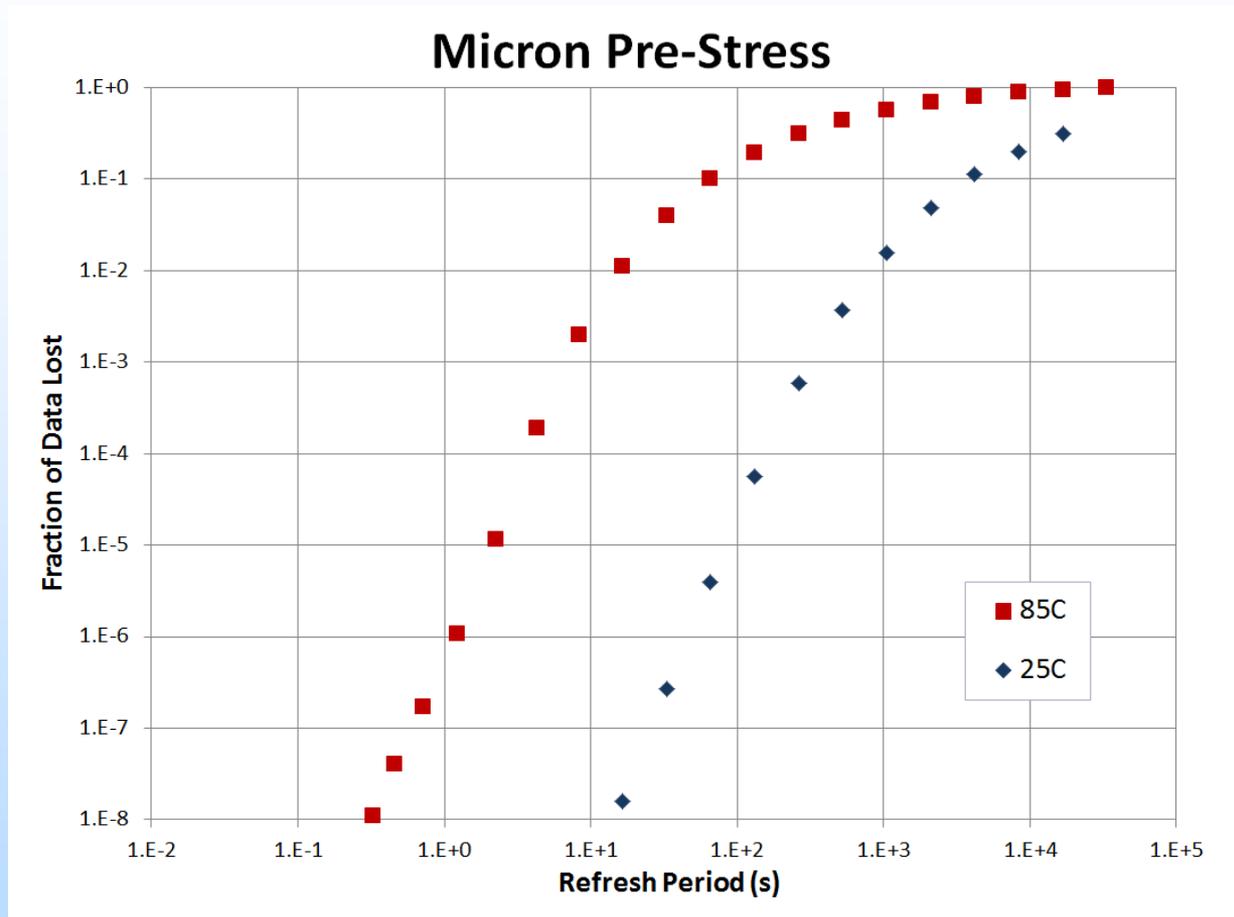
Test Efforts



- Pre-stress data on Samsung shows normal operation
- At 85C most bits hold for more than 1000s.



Test Efforts

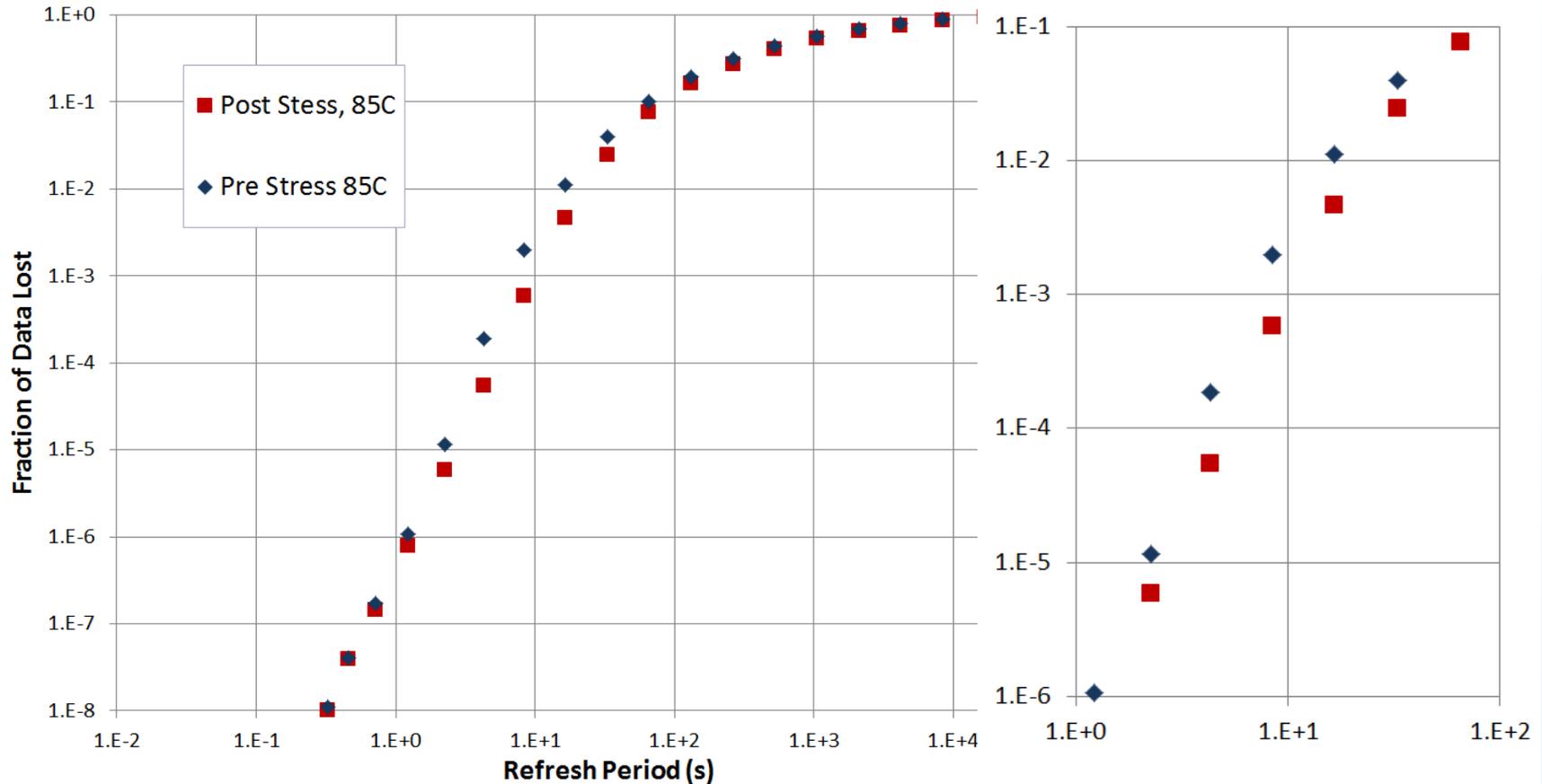


- At 85C most bits are lost by 100s, but the worst bits are better than we saw with Samsung

Example Results



Micron Pre-Stress



- For stored data, only change is to mid-range bit distributions



Future Directions

- Widen scope of target devices
 - Continue testing of DDR2, pushing down to 40nm
 - Look into options for DDR3, if there is program interest
 - Increased manufacturer sample over what has been done so far
- Increase parametric test capabilities
 - Key parametrics will require specialized tester capable of testing key timing and frequency-related items.
 - Improving high volume test system to enable other parametrics (such as additional test functions and some key parameter altering)
 - Enables wider sampling of potential device degradation modes
 - the value of which is indicated by the data presented.
- Increase cross-NEPP support
 - Working to ensure JPL and GSFC test equipment and target devices are relatively interchangeable

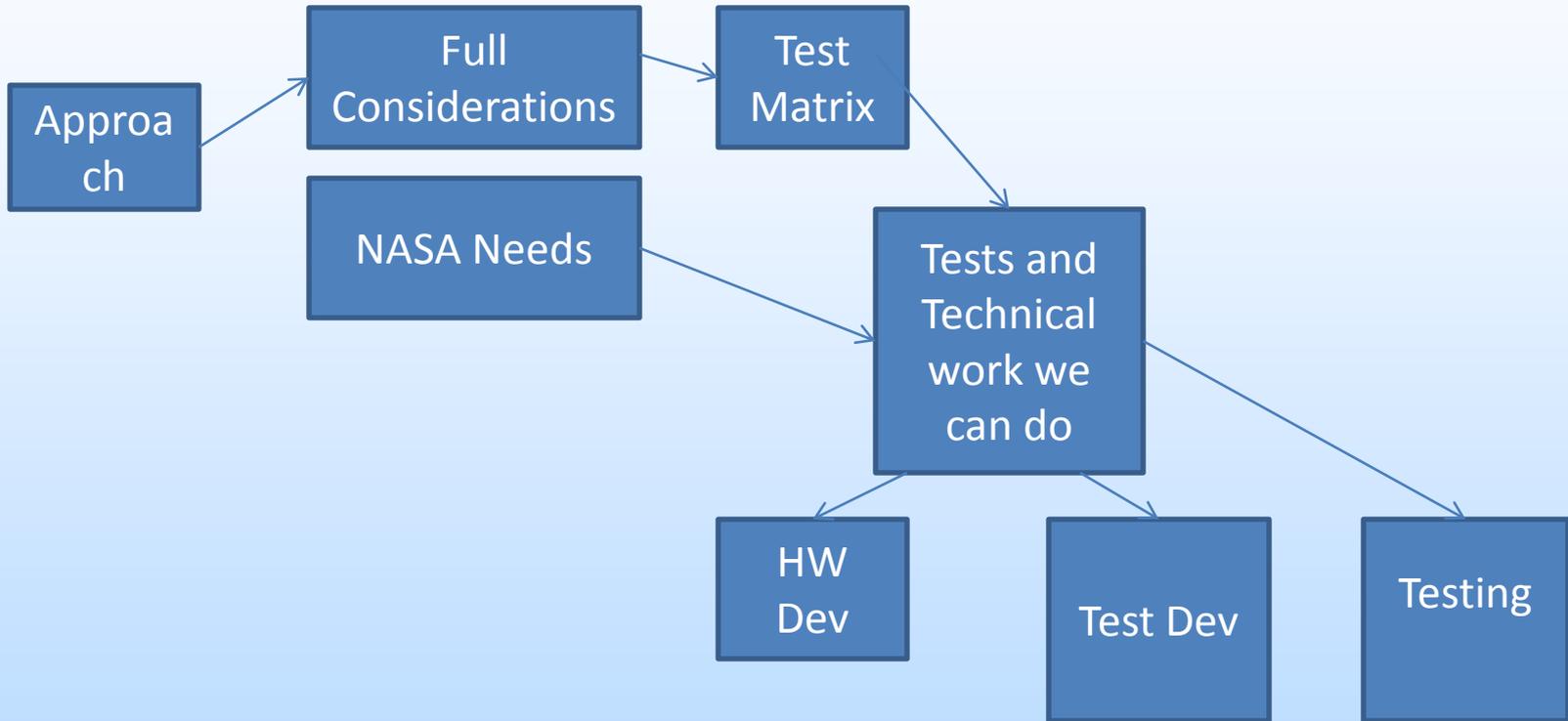


Conclusion

- Qualification approach seeks to provide useful data for NASA programs
 - Specifically understanding non-standard use and testing for NASA-specific environments
 - Develop knowledge to support analysis of spacecraft issues
- Reliability test matrix is too big
 - DDR devices are essentially complex ICs with many subcomponents
 - Failure mechanisms depend on different operating conditions
 - Must employ methods to select most relevant measurements
- Test hardware to support target measurements
 - Developing multiple hardware solutions targeting complimentary roles
 - Will be able to support 18-36 simultaneous DUTs
 - Working to ensure interchangeable hardware across NEPP
- Test efforts
 - Data reported on 78nm DDR2 – indicated potential benefit from additional parametrics
 - Results applicable to storage array and operating currents
 - Testing targeted static pattern at 125C/2.7V
- Future efforts will continue to improve testing capability
 - Working to increase test matrix/methods, in concert with further understanding of mechanisms and parameters of interest to flight projects.
 - Increase targeted test devices sampling including sub 65nm devices
 - Provide test capabilities to identify additional parameteric shifts



END





References

- Micron 2Gb DDR2 data sheet
- Mosis tech_cmos_rel FAQ “Reliability in CMOS IC Design: Physical Failure Mechanisms and their Modeling”
- Wikipedia DDR4 entry
- Jin Et. Al. “Prediction of Data Retention Time Distribution of DRAM by Physics-Based Statistical Simulation” – shows potential mechanism for our response is traps under the gate.



Additional Resources

- <http://www.sciencedirect.com/science/article/pii/S0026271402000306>
- <http://trs-new.jpl.nasa.gov/dspace/handle/2014/20169>
- <http://ieeexplore.ieee.org/Xplore/login.jsp?url=http%3A%2F%2Fieeexplore.ieee.org%2Fiel5%2F8520%2F26927%2F01197774.pdf%3Farnumber%3D1197774&authDecision=-203>
- <http://www.quickstartmicro.com/Sample%20Slides%20Quick%20Start%20IC%20Reliability.pdf>

Device Operation during Life Testing



- Key parameters for a given circuit element:
 - Temperature, Voltage(Electric Field), Activation Energy, Current Density, Times Switched,
 - At any given node, $V=V(t)$
- Desired operations
 - Switching of all transistors
 - Switching/operating a key subset of transistors
 - Operating at degraded frequency (for derating)
 - Operating worst case voltage and temperature, possibly off the datasheet.
 - Keep all “static” items biased the same as in operation
 - For DRAM data, this is achieved by simply refreshing, but can also be achieved by writing and reading the array repeatedly
 - Similar to industry standard Dynamic Operation Stress (DOS)



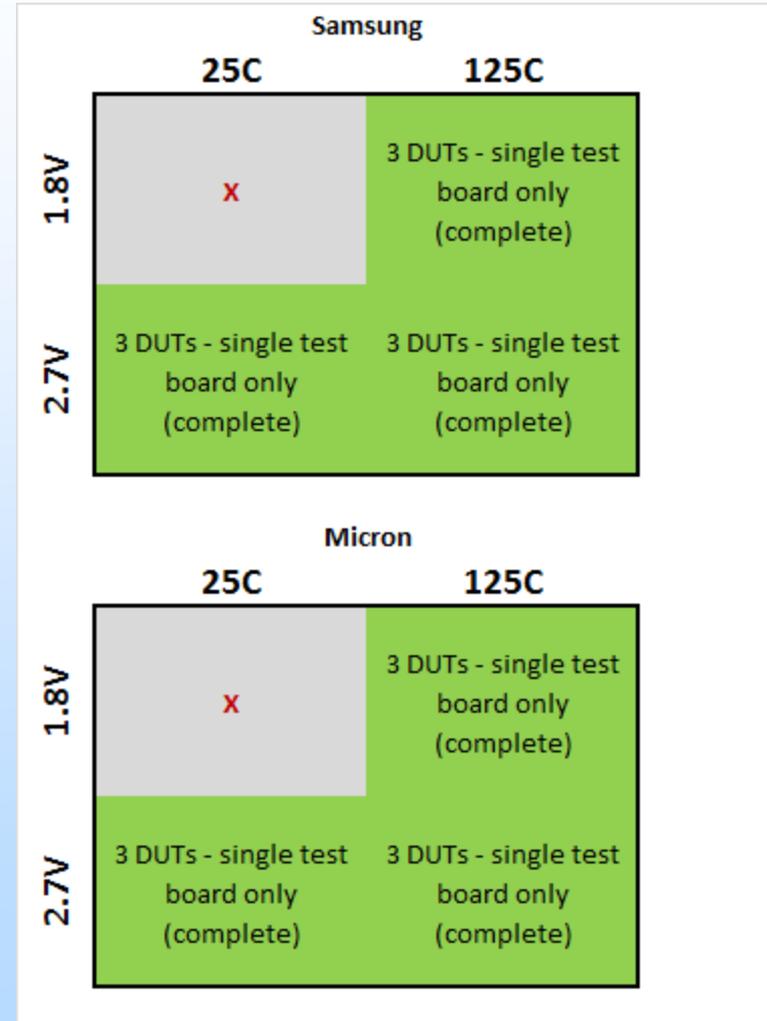
A Parametric Approach

- Reliability testing generally targets key datasheet parameters
- Bias – Supply and I/O bias
 - E.g. V_{IL} – The maximum input voltage that will be sampled as a '0'
 - Tested by shmooing V_{IL} from low till errors seen
- Currents – I_{DD} during various operations
 - E.g. I_{DD3N} – Active standby current; I_{DD7} – Operating bank interleave read current
 - Tested by observing I_{DD} while operating device under specific function
 - Dependent on operating frequency (400+MHz for DDR2)
- Timing
 - E.g. #####
 - Key timing values defined during a specific functional state – I.e. for Micron 2Gb, the state is I_{DD7} (above)
 - When looking for degradation, shmoo is required
- Data Retention
 - Walmart Task Force!!!



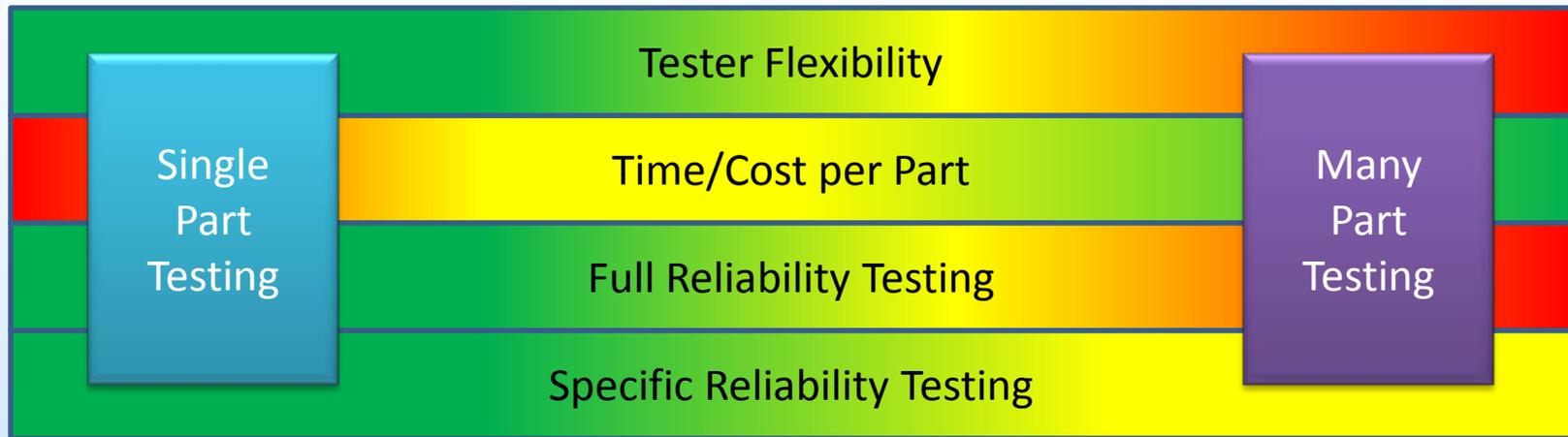
Test Efforts

- Perform Stress testing of Micron and Samsung 78nm 2Gb DDR2
 - Efforts focused on single-DUT test system
 - 9 under test at a time
- Characterization
 - Pre/post and periodic characterization
 - Measure a few basic data sheet parameters as well as cell data retention
- Device Stress
 - Stress devices with 2.7V and/or 125C
 - Perform stress for 1000 hrs





Single vs. Multi-Part Testing



- Qualitative relative capability suggest that many-part testing is desired when cost/part is key.
- For DDR, industrial testers provide some ability to move the costs around, but generally limit testing to standard parameters
- For testing of lots of parts, we prefer something in the middle, or a dual-approach...