



Evaluation of Microchip Tantalum Capacitors

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Scope of NEPP Tasks

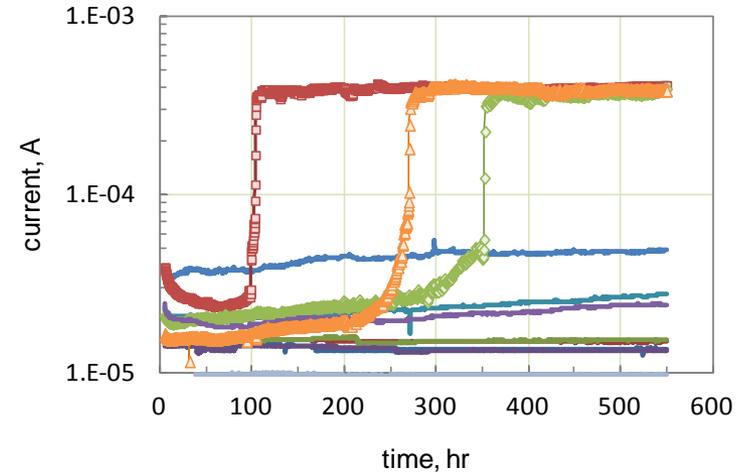
● Screening Techniques for Ceramic Capacitors with Cracks

- Breakdown voltages (DWV).
- Acoustic microscopy.
- Impedance spectroscopy.
- Absorption currents and voltages.
- Humidity Steady-State Low Voltage Testing.
- Degradation of leakage currents at different T and RH conditions.

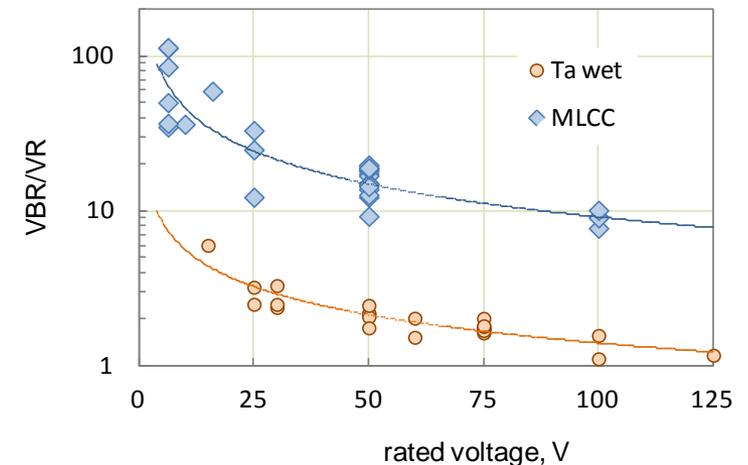
● Reliability of Advanced Wet and Solid Tantalum Capacitors

- Wet tantalum capacitors.
- HV polymer capacitors.
- Microchip capacitors.

Mfr.M 1210 10uF 25V 125C at 50V



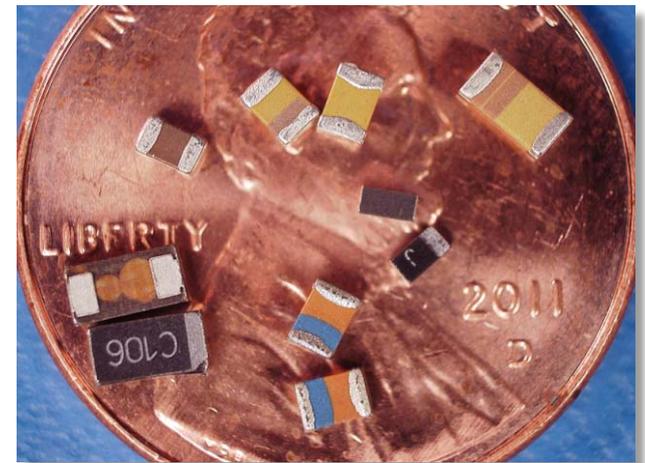
Ceramic and Tantalum Capacitors



Purpose and Outline

Purpose: Evaluate performance, potential reliability risks, and suggest adequate S&Q tests.

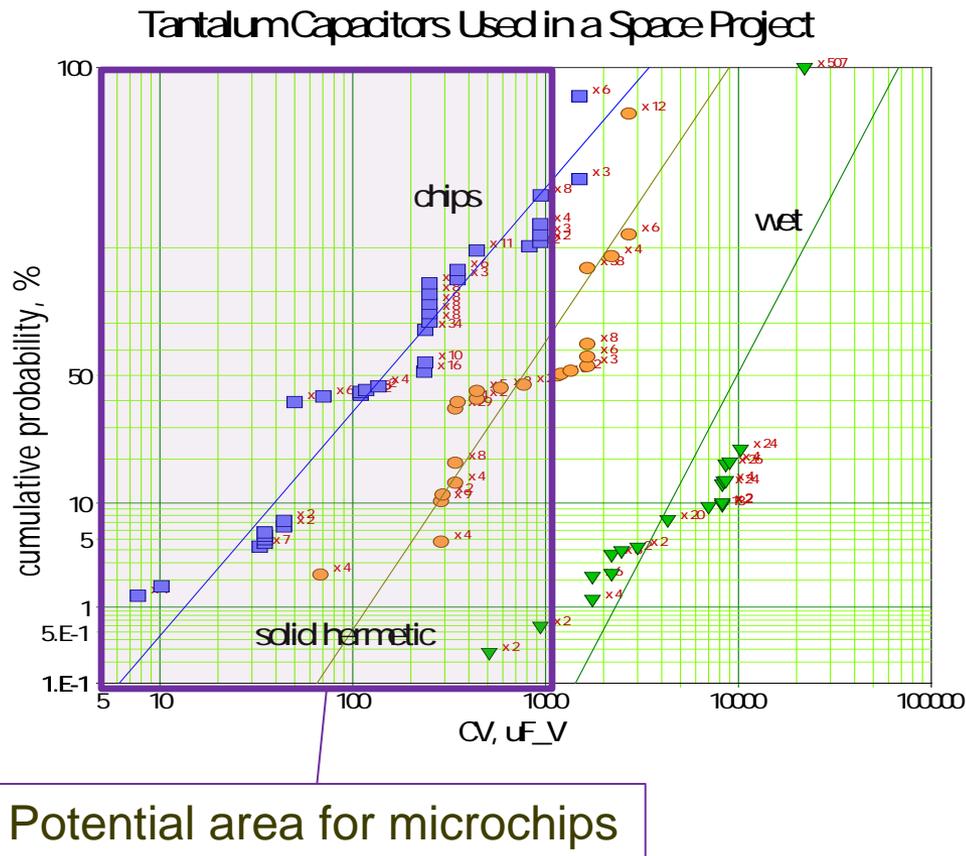
- ❑ Introduction
- ❑ Design
- ❑ Electrical characteristics
- ❑ Effect of soldering-induces thermal shock
- ❑ Thermo-mechanical characteristics
- ❑ Effect of mechanical stresses
- ❑ Step stress life testing
- ❑ Conclusions



EIA size 1206,
0805, 0603

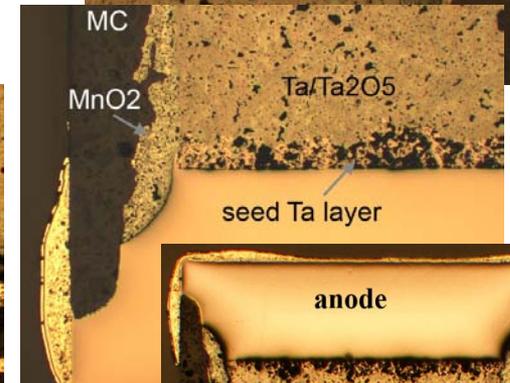
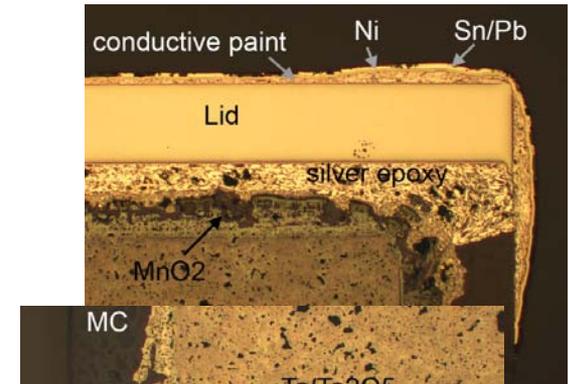
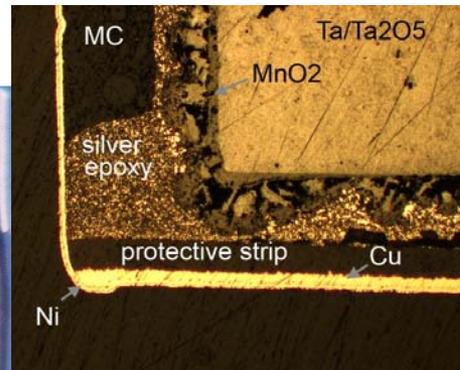
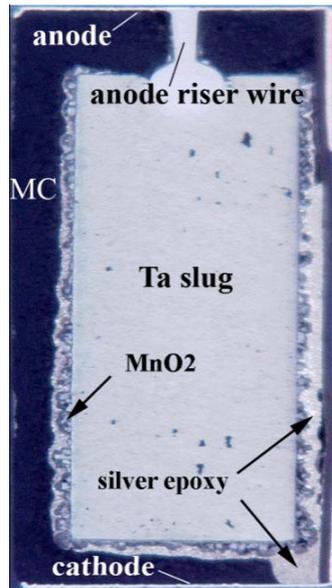
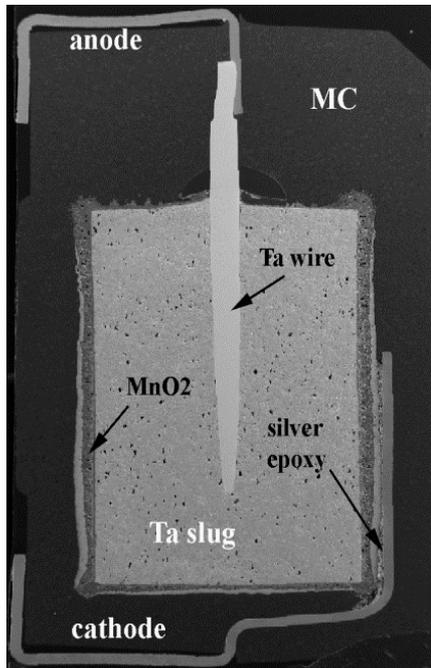
Use of Tantalum Capacitors in a Space Project

- ❑ Conservative approach for space designs – low CV.
- ❑ Small size reduces the probability of ignition.
- ❑ Microchips compete with MLCCs?
- ❑ Decreasing the weight and size has obvious benefits for space applications.
- ❑ Concerns:
 - Performance.
 - Effect of soldering.
 - Reliability.



Design of Microchip Capacitors

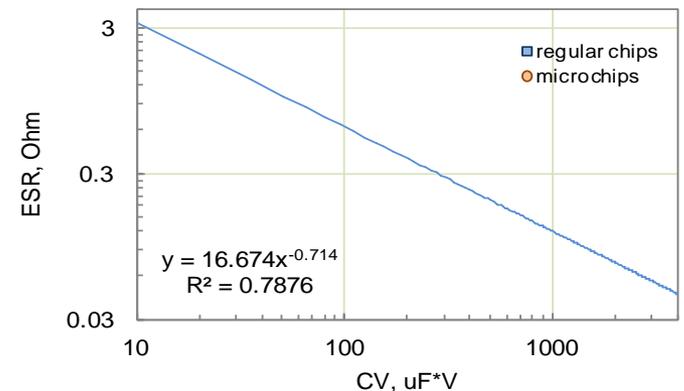
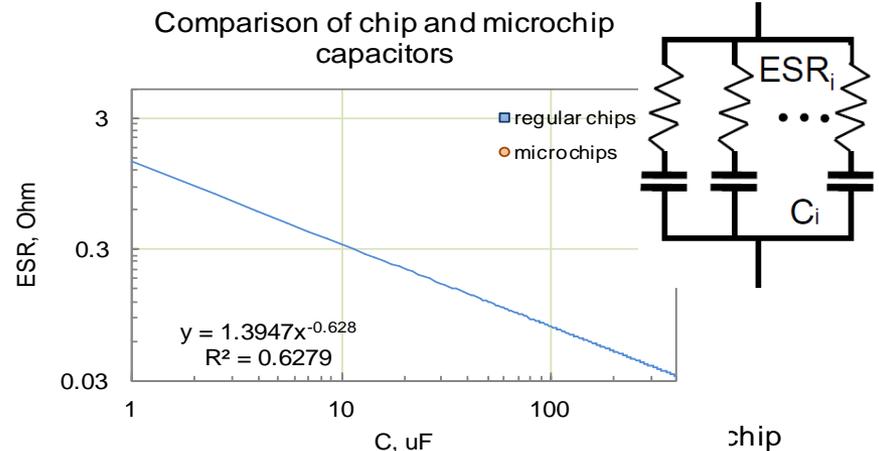
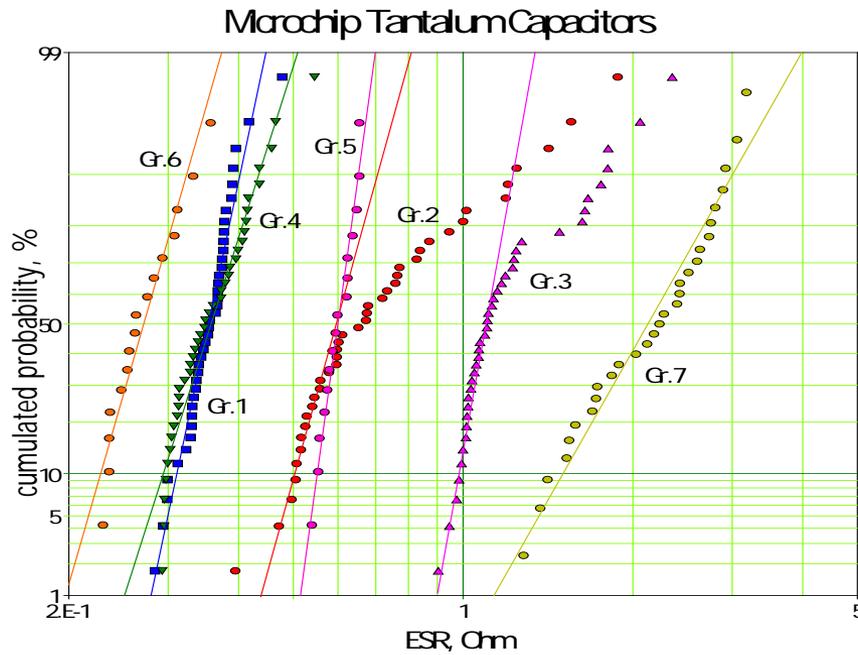
- ❑ No welding interconnections. Increase in efficiency from ~30% to more than 50%.
- ❑ Protective strip and wafer-base designs.
- ❑ Drawback: no stress relief during soldering.



Microchips Used in this Study

Gr.	C, μF	ΔC %	VR, V	DCL, mA	DF, %	ESR, Ohm	EIA case	L, mm	W, mm	H, mm
1	33	20%	10	3.3	12	1	1206	3.2	1.6	1.6
2	33	20%	10	3.3	20	5	0805	2.1	1.4	1.4
3	1	20%	35	0.5	8	5	0805	2.1	1.4	1.4
4	10	10%	10	1	8	6	0805	2.1	1.4	1.4
5	10	10%	16	0.8	8	6	1206	3.2	1.6	1.7
6	47	10%	10	2.35	8	1		3.5	2.8	1.5
7	4.7	20%	6.3	0.16	8	5	0603	1.6	0.85	0.85

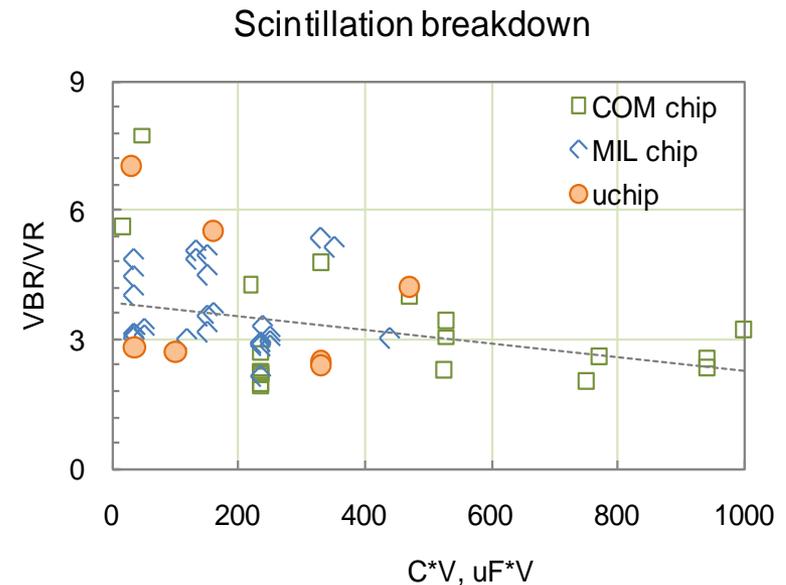
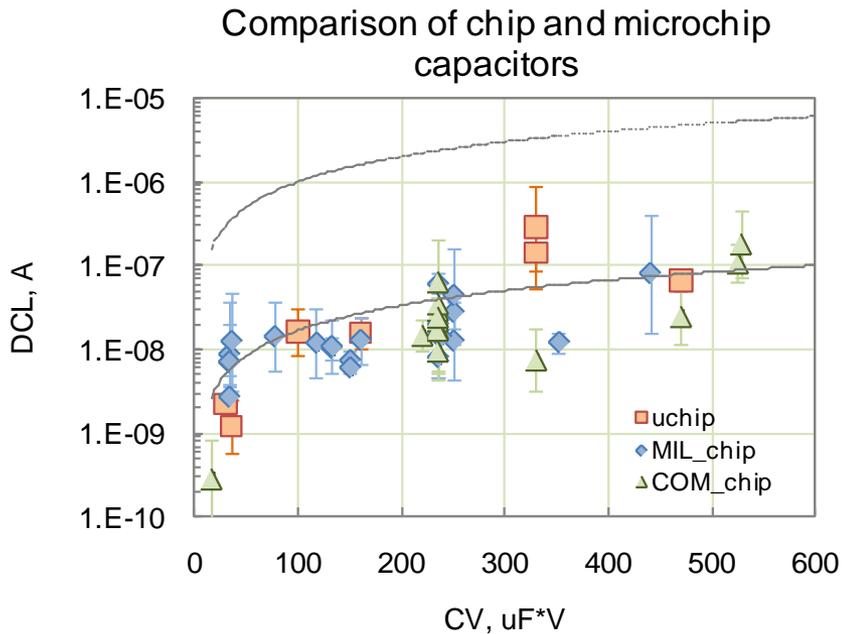
Performance: ESR



- ❑ Some lots have outliers.
- ❑ Microchips have ESR close regular chips.
- ❑ Larger ESR – better resistance to surge currents.
- ❑ ESR decreases with capacitance.
- ❑ A better fit: $ESR = f(CV)$.

$$ESR = \frac{16.64}{(C \times V_R)^{0.71}}$$

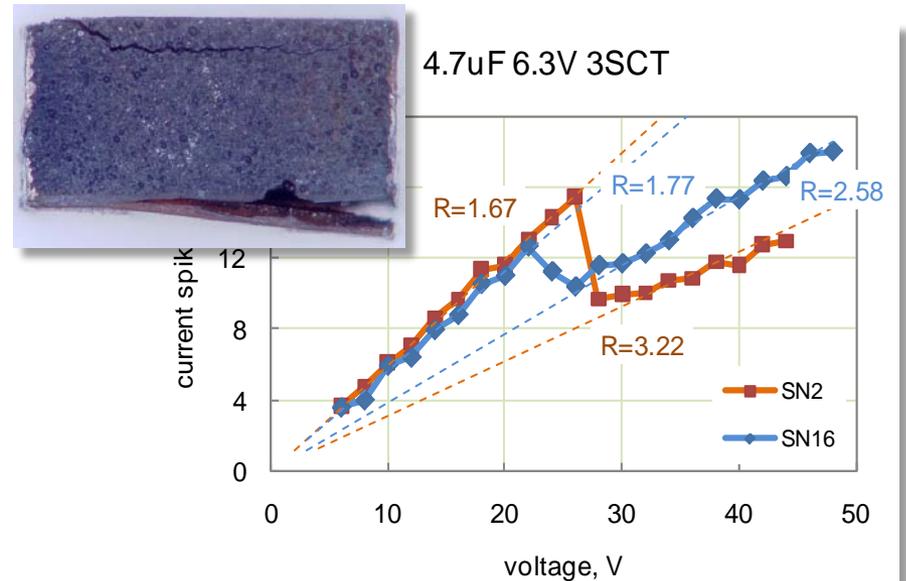
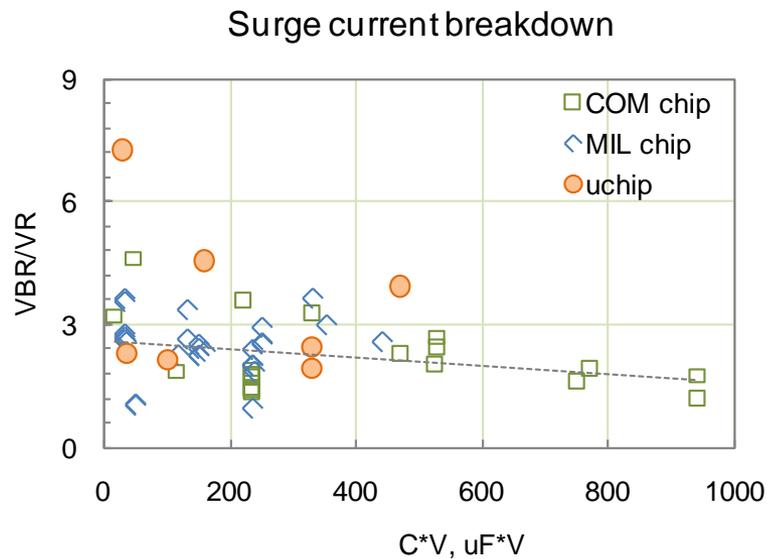
Performance: DCL and VBR_scint



- ❑ All microchips, except for two lots, had DCL within the range that is typical for regular chips.
- ❑ Margins of VBR_scint for all microchips exceeded 50% that is typical for high quality regular chip capacitors.

Performance: Surge Current Breakdown

- ❑ Some lots had VBR_SCT margins in the range from 170% to 330% that exceeds performance of military-grade capacitors.
- ❑ Fracturing resulted in ESR increase and open circuit failures.
- ❑ Increase in ESR and fracturing are prevailing in small-size parts because thin packages do not create compressive stresses large enough to suppress tensile stresses caused by SCT.



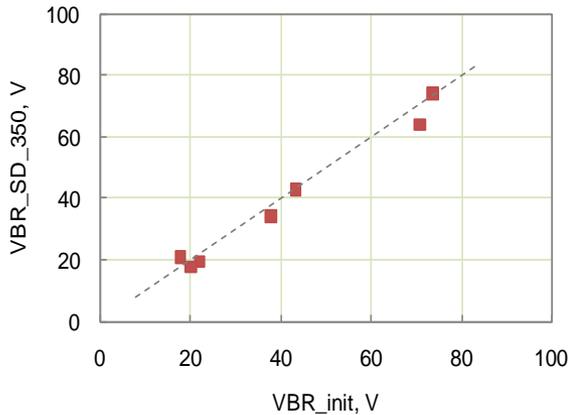
Terminal Solder Dip Test

Lot	C, μF	VR , V	Size, LxWxH, mm ³	Test cond.	AC	DCL	VBR	Results/Comment
Lot 1	33	10	3.2x1.6x1.6	TSD_300	0/10	0/10	0/10	Degradation of C, ESR, DF and DCL
				TSD_325	1/10	0/10	0/10	
				TSD_350	2/10	0/10	0/10	
Lot 2	33	10	2.1x1.4x1.4	TSD_300	1/10	1/10	0/10	Degradation of C, ESR, DF and DCL
				TSD_325	1/10	0/10	0/10	
				TSD_350	1/10	2/10	0/10	
Lot 3	1	35	2.1x1.4x1.4	TSD_300	1/10	0/10	0/10	Degradation of ESR
				TSD_325	3/10	1/10	0/10	
				TSD_350	5/10	2/10	0/10	
Lot 4	10	10	2.1x1.4x1.4	TSD_300	0/10	0/10	0/10	Degradation of DF and ESR at TSD_350
				TSD_325	0/10	0/10	0/10	
				TSD_350	0/10	1/10	0/10	
Lot 5	10	16	3.2x1.6x1.7	TSD_350	0/20	0/20	0/10	No degradation
Lot 6	47	10	3.5x2.8x1.5	TSD_350	0/20	0/20	0/10	No degradation
Lot 7	4.7	6.3	1.6x0.85x0.85	TSD_350	0/20	1/20	0/10	Degradation of DCL

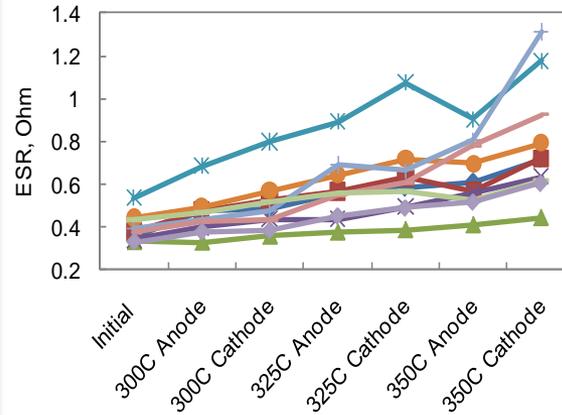
Some lots can sustain manual soldering

Terminal Solder Dip Test, Cont.

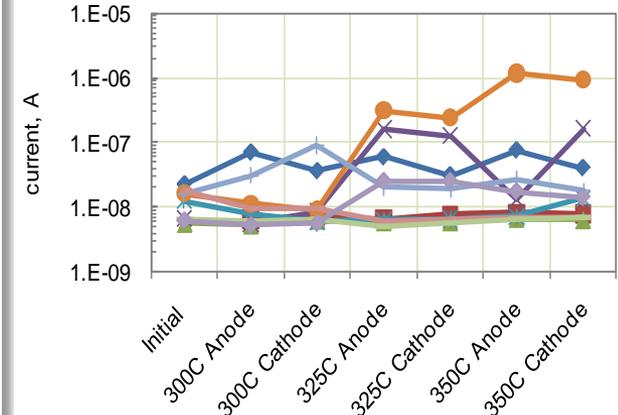
Effect of SD_350 on 3SCT



Gr.1 33uF 10V

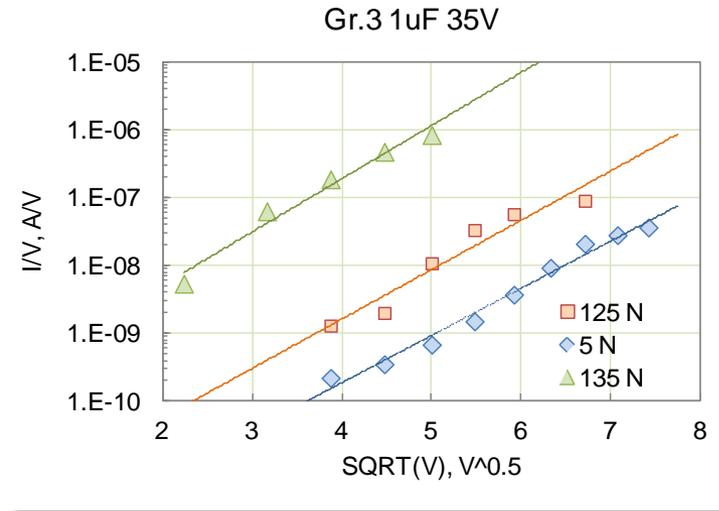
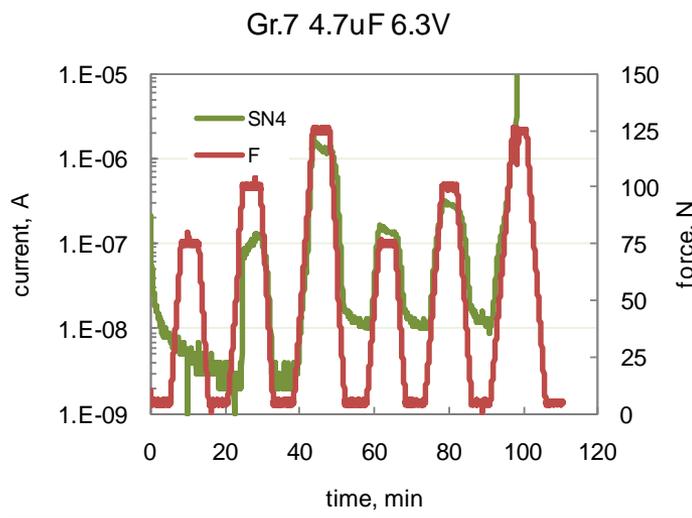


Gr.4 10uF 10V

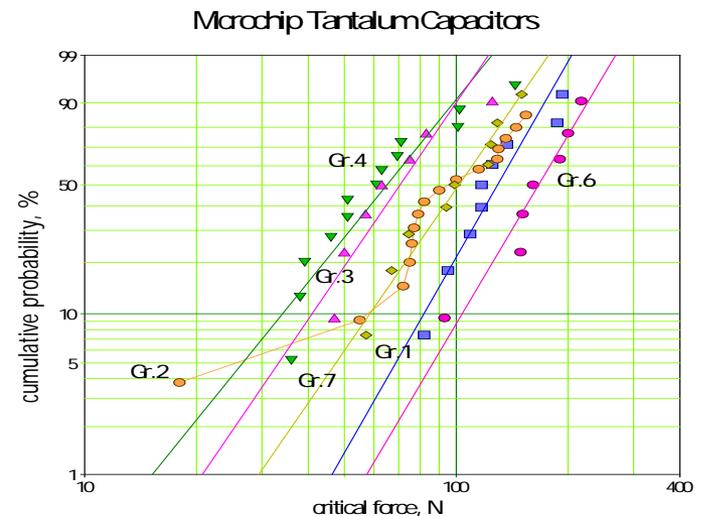


- ❑ All lots passed SCT at rated voltages and no substantial variations in distributions of VBR was noted.
- ❑ Degradation of ESR was greater during cathode side solder dipping compared to the anode side.
- ❑ Degradation of leakage currents occurred mostly after anode side solder dip testing.

Effect of Mechanical Stresses



- ❑ Compressive stresses might cause degradation in the parts.
- ❑ Stress-induced traps generation increases Poole-Frenkel conductivity.
- ❑ Stress-induced degradation is reversible.
- ❑ Some parts might be “out of family” degrading at relatively low stresses.



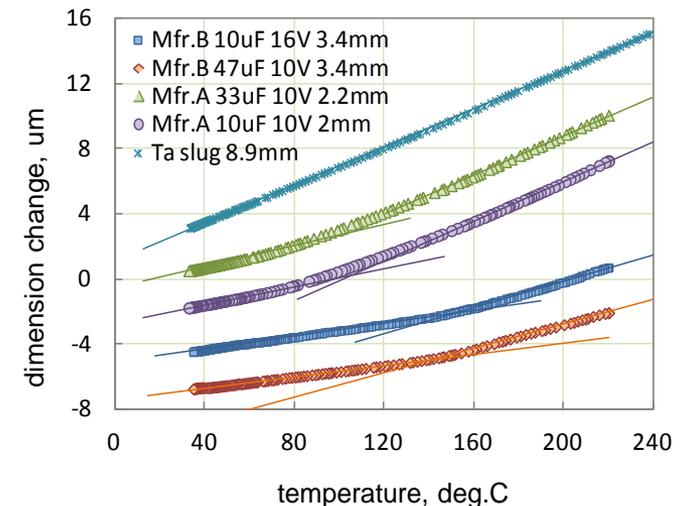
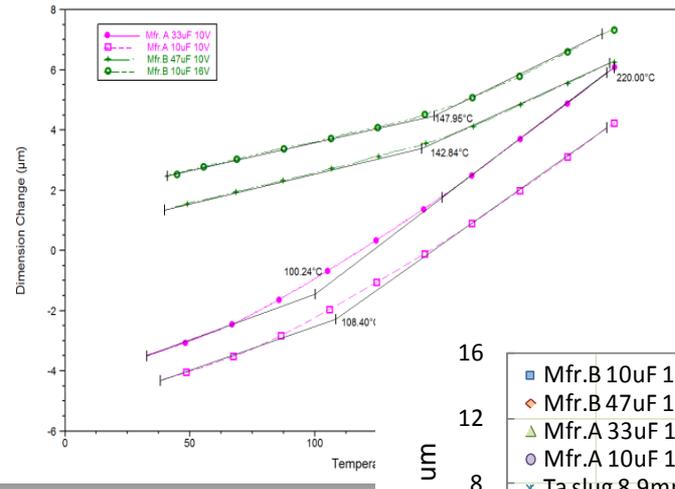
Thermo-Mechanical Characteristics

❑ Tantalum slug:
CTE ~ 6.2 ppm/ $^{\circ}\text{C}$.

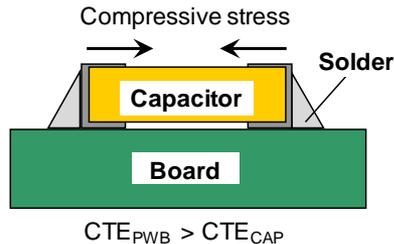
❑ Mfr. A:
 $T_g \sim 100$ $^{\circ}\text{C}$
CTE1 ~ 12 ppm/ $^{\circ}\text{C}$ at $T < T_g$.
CTE2 ~ 34 ppm/ $^{\circ}\text{C}$ at $T > T_g$.

❑ Mfr. B:
 $T_g \sim 150$ $^{\circ}\text{C}$
CTE1 ~ 6.5 ppm/ $^{\circ}\text{C}$ at $T < T_g$.
CTE2 ~ 12 ppm/ $^{\circ}\text{C}$ at $T > T_g$.

❑ Substantial CTE mismatch between
MC and tantalum slug might cause failures during TC.



Effect of Mechanical Stresses, Cont.



$$\sigma = \frac{(\alpha_{PWB} - \alpha_{cap}) \times (T_g - T_r)}{(E_{cap})^{-1} + \left(E_{PWB} \times \frac{A_{PWB}}{A_{cap}} \right)^{-1}}$$

Characteristic	FR4	PI	μ chips
T _g , °C	145	230	
CTE, ppm/°C	15	12.4	5.6 to 14
E, GPa	17.5	23.5	10

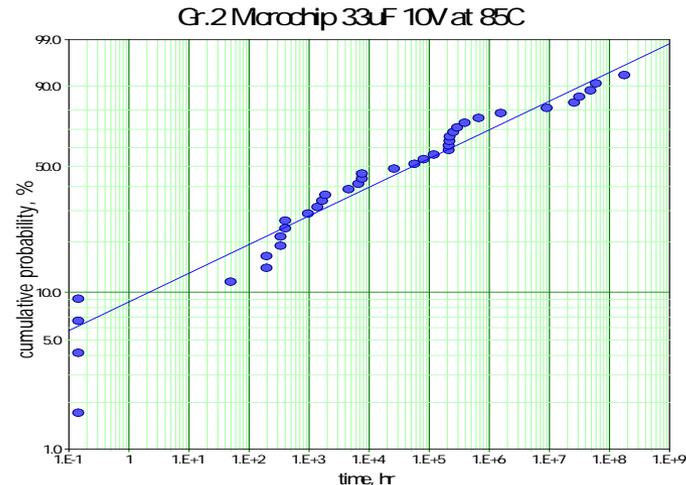
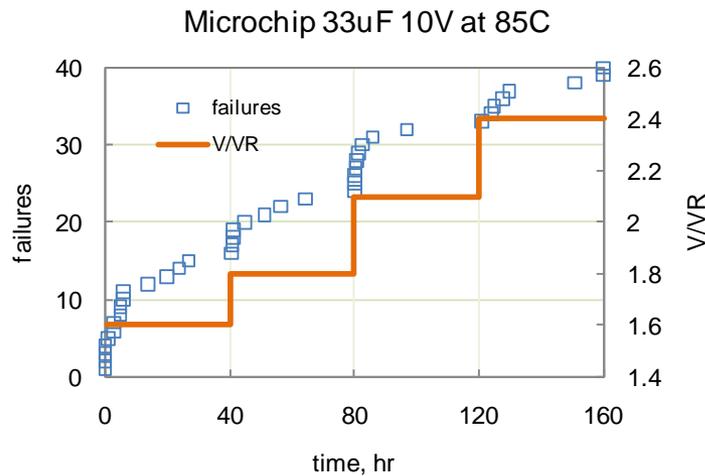
- ❑ For both, PI and FR4 boards, the level of stresses is relatively low, and there is no risk of degradation for normal quality parts.
- ❑ Some microchips might degrade at relatively low stresses.
- ❑ To assure that soldering will not cause damage and failures of the parts a qualification testing at a stress of 10 MPa is recommended for high-reliability applications.

Life Step Stress Testing

- Weibull-exponential cumulative damage model.
- Step duration 20 to 40 hrs.
- Testing at 22 °C, 85 °C, and 125 °C allows for estimation of the voltage acceleration constant (B) and effective activation energy (Ea).

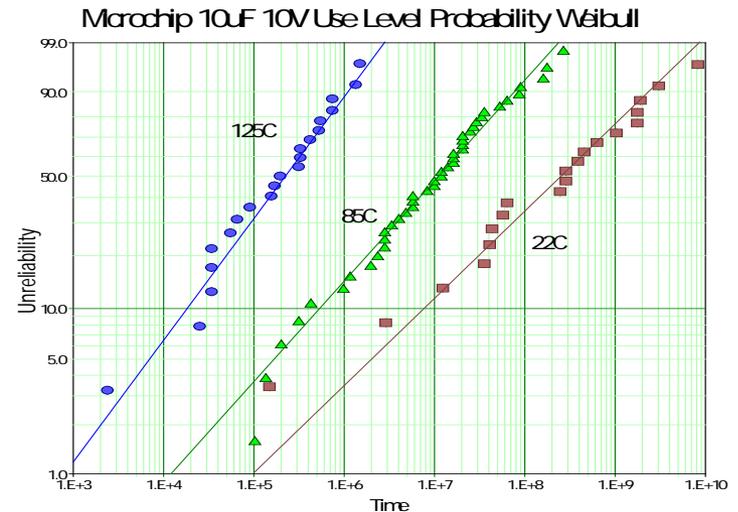
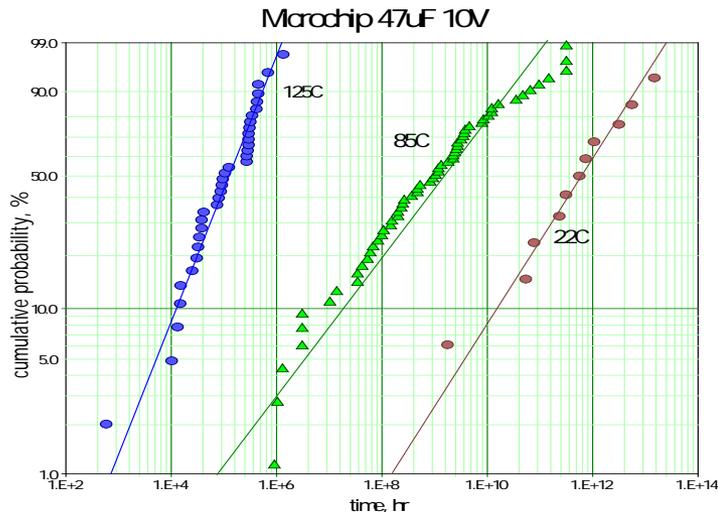
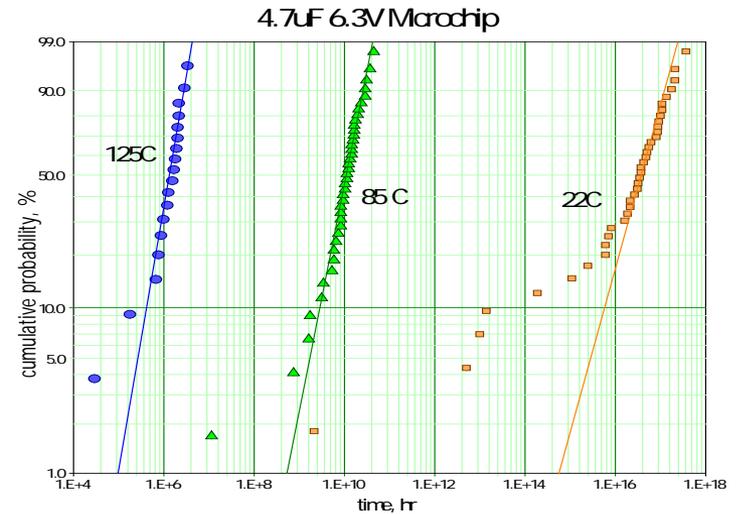
$$\eta = \exp\left(\alpha_0 + \alpha_1 \times \frac{V}{V_R}\right)$$

$$AF_V = \frac{\eta(V)}{\eta(V_R)} = \exp\left[\alpha_1 \times \left(\frac{V}{V_R} - 1\right)\right] = \exp(B \times u)$$



Life Step Stress Testing, Cont.

- ❑ In one group had $\beta > 1$, \Rightarrow wear-out.
- ❑ Inception time ~ 100 years at $125\text{ }^\circ\text{C}$ and $>10^{10}$ years at RT.
- ❑ This group had high VBR \Rightarrow high quality dielectric.
- ❑ Early failures were likely due to defects in the oxide.



Life Step Stress Testing, Cont.

- At 85 °C $6 < B < 18$. Some lots deviate substantially from the accepted standard constant ($B_s = 18.77$).
- FR calculated at conditions simulating Weibull grading test per MIL-PRF-55365 showed that microchip capacitors can be screened to a high FR levels up T-level (0.001%/1000hr).

Lot	T, °C	QTY	β	α_0	α_1	$\eta(VR)$	WGT FR, %/1000hr	Ea, eV
Gr.2	85	40	0.19	26.98	-14.12	3.85E+05	1.6E-02	
GR.4	22	20	0.51	33.53	-13.43	5.39E+08		0.66
	85	43	0.62	35.05	-18.23	2.01E+07	6E-03	
	125	21	0.81	36.39	-23.70	3.25E+05		
Gr.6	22	11	0.51	38.42	-10.56	1.25E+12		1.37
	85	60	0.34	31.87	-9.92	3.39E+09	4.7E-04	
	125	34	0.82	18.44	-6.26	1.95E+05		
Gr.7	22	38	1.05	46.16	-7.89	4.17E+16		2.15
	85	40	1.4	29.40	-6.02	1.43E+10	1.2E-11	
	125	18	1.62	18.48	-4.16	1.66E+06		

Selection, DPA, S&Q

DPA:

- Verify the shape and size of silver epoxy.
- Radiography to assure adequate thickness of the plastic package, manganese layer, and the size of the contact area between silver-epoxy and terminations.

Screening:

- Two-side radiography.
- SCT for all types, measurements of ESR, and delta analysis.
- WGT using a verified AF_V . Optional BI: 40 hrs at 85 °C and 1.5VR. Maximum PDA. Verification of contacts.

Qualification testing:

- SCT and VBR_scint to obtain baseline distributions.
- 100 TC: -65 °C to +150 °C. Post-TC measurements of VBR.
- Life testing at 105 °C and 1.1VR for 2000 hours.
- RSH should include post-test VBR.
- TSD_325 if parts are to be soldered manually.
- Flex-stress testing (TBD).
- Effect of stress: DCL at 10 MPa.



Conclusion

1. All AC and DC characteristics of microchips were within the specified limits and 5 out of 7 lots had VBR and DCL margins that are typical for high quality chip tantalum capacitors.
2. Values of ESR for microchips are close to the equivalent molded chip capacitors. An increase of ESR and fractures were observed during surge current testing in some lots.
3. Microchips can be robust enough to sustain manual soldering TS. However, different lots have different susceptibility to degradation.
4. Microchips are sensitive to compressive stresses. Lots with excessive sensitivity might cause failures after soldering.
5. Different types of microchips have different CTE and T_g. Large CTE might cause damage to the dielectric and fractures in the attachment.
6. Failure rate for microchips can be as low as for T-level (0.001%/1000hr) MIL-PRF-55365 parts.
7. At 85 °C the acceleration constant varies from 6 to 18. The value of AF_V should be determined for each part type for accurate FR grading.