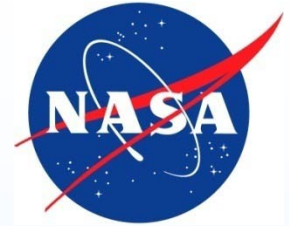


**NEPP Electronic Technology Workshop**  
**June 11-13, 2012**

National Aeronautics  
and Space Administration



# **MRAM Technology and Status**

**Jason Heidecker**

**Jet Propulsion Laboratory, California Institute of Technology**

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# What is an MRAM?

*MRAM = Magnetoresistive RAM*

- WRITE using magnetic hysteresis.
- READ using magnetoresistance.
- Built on CMOS. TSOP packages (or ceramic flat-pack for space)
- Architecture similar to SRAM.
- First memory to use magnetic structures exploiting electron SPIN as well as CHARGE.
- Future technologies have potential for very HIGH DENSITIES.
- MEMORY CELLS are nonvolatile (unlimited retention) and immune to radiation-induced upset. Also unlimited endurance.





# MRAM: The Ideal Memory?

- DRAM Density
- SRAM Speed
- NAND Nonvolatility
- Rad-Hard Memory Cells

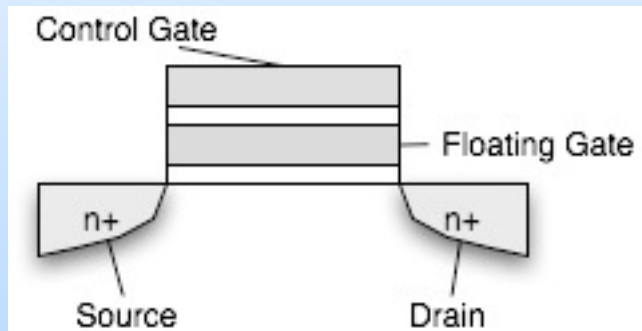
***Potential to be first nonvolatile Gb memory with unlimited endurance and 20+ year retention (and SEU immunity bonus)***

# Spintronics

## *MRAM, The Spintronic Memory*

### Traditional Memory

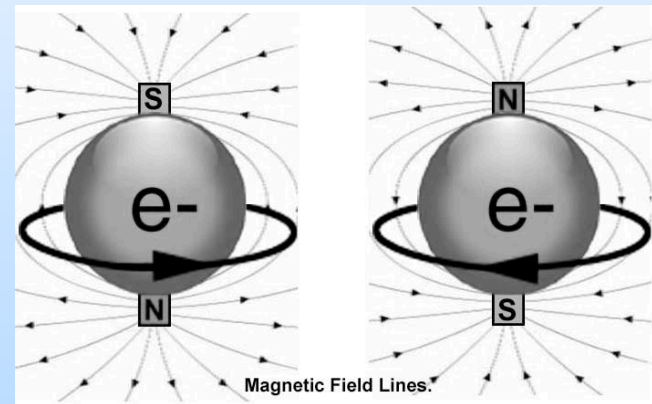
- Bulk Movement/Storage of Electrons



Ref [1]

### Spintronics

- Exploitation of Electron *Spin* and Resulting Magnetic Moment



Ref [1]

***Information is carried by electron spin in addition to, or in place of its charge.***

# Read: Magnetoresistance (MR)

## *Types of magnetoresistance (MR):*

Name	Increase in Resistance
Ordinary (OMR)	2%
Giant (GMR)	50%
Colossal (CMR)	99.9%
Tunnel (TMR)	200%



***Modern “MTJ” MRAMs***

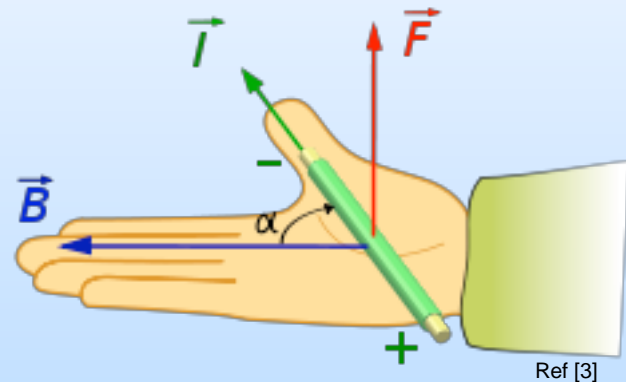
# “Ordinary” Magnetoresistance Effect

*Resistance of material changes with applied magnetic field.*

Effect discovered by Lord Kelvin in 1856.

Increased resistance is due to Lorentz Force:

$$\vec{F} = q(\vec{E} + \vec{v} \times \vec{B})$$



Ref [3]

Also known as “anisotropic magnetoresistance” (AMR) because effect is 0 when current and B are parallel and maximum when perpendicular.

## Corbino Disc

*Magnetic field adds circular current component  $I_\theta$  and creates resistance to radial component  $I_\rho$ .*

Ref [2]

Change in resistance is proportional to  $B^2$  (Kohler’s Rule):

$$\frac{\partial \rho}{\rho} \propto a \left[ \frac{H}{\rho} \right]^2$$

# “Giant” Magnetoresistance

## Birth of “spintronics

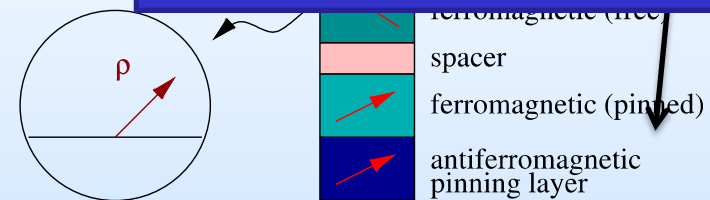
Using pinning layer also known as “spin valve” structure

- A much larger magnetoresistance effect (up to 50%) observed in thin-film structures composed of alternating ferromagnetic and non-magnetic layers (e.g. Fe/Cr/Fe). Thicknesses in nm.
- Current passes parallel to layers: current in plane (CIP).
- Resistance of material is affected by alignment of magnetic moments of magnetic materials which creates changes in scattering of spin up or spin down electrons.
- *In practical application as memory cell, change in resistance is too small (4-8%). Not good enough for high density memory.*

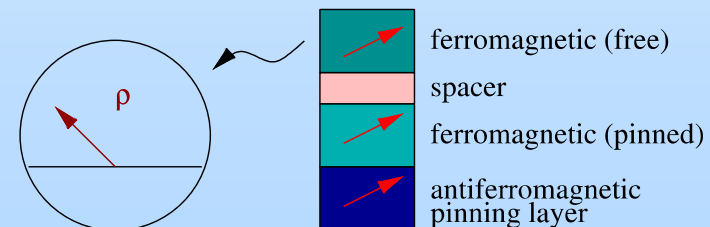
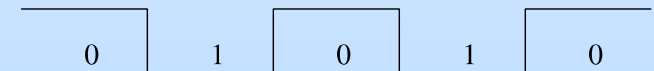
*The 2007 Nobel Prize in physics was awarded to Albert Fert and Peter Grünberg for the discovery of GMR, which they did (independently) in the 1980s.*

## Disc Head Readers

*Discovered by IBM and published in 1991. Modern MRAM is derivative of this structure.*



unmagnetized magnetized



Ref [4]

# “Colossal” Magnetoresistance

- Very large change in resistance under magnetic field observed mostly in certain manganese oxide compounds
- First seen in 1950s by Jonker and Stanten (Philips)

- Effect not well understood
- Materials not to be seen in MRAM (or any other electronics) any time soon

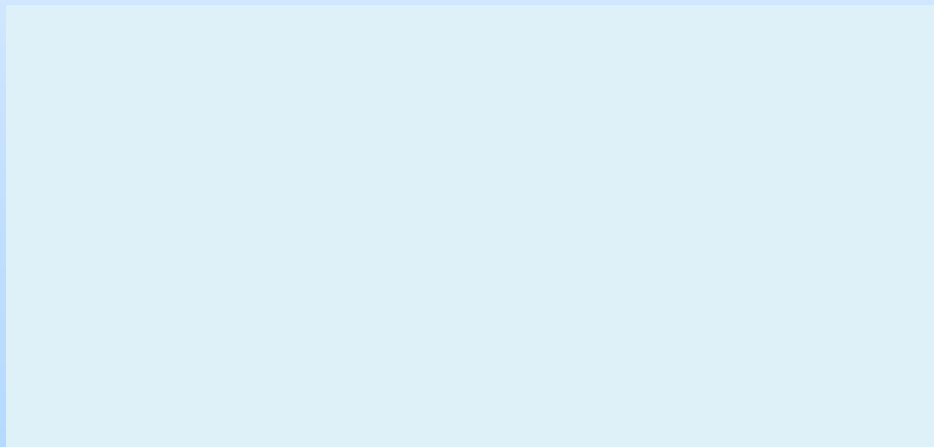
istance has recently been discovered in  $\text{La}_{1-x}\text{Ca}_x\text{MnO}_3$ . The largest effects have been observed for  $x=0.07$ . The effects observed, on the order of  $\Delta R/R(H) = 125$ , the resistance changes by 99.9%. Figure 14 shows the resistivity of the material undergoes a low temperature behavior. The colossal magnetoresistance effect research has shown that the insulating to metal transition temperature. HP has produced high quality CMR films of about 95%. This resistance reduction is relative to the low temperatures (Figure 16). These results were reported at the National Laboratory in February, 1995 [Ref. 8]. The main problem with these materials is the field dependence of the resistance. To obtain the large effect. These issues will be the focus of future research.

Ref [5]

# “Tunnel” Magnetoresistance and the MTJ

## *Magnetic Tunnel Junction (MTJ) Cell Structures*

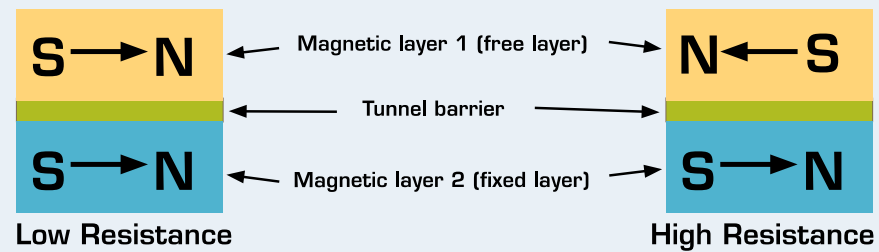
- Two layers of magnetic metal (such as cobalt-iron) separated by a layer of insulator (typically aluminum oxide, ~1 nm)
- Tunneling Magnetoresistance
  - Consequence of spin-dependent tunneling



Ref [6]

# MTJ Operation

## MTJ STORAGE ELEMENT



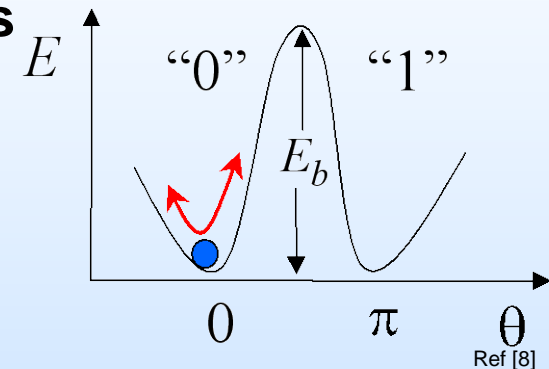
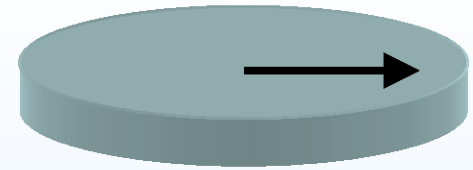
Ref [6]

Ref [7]

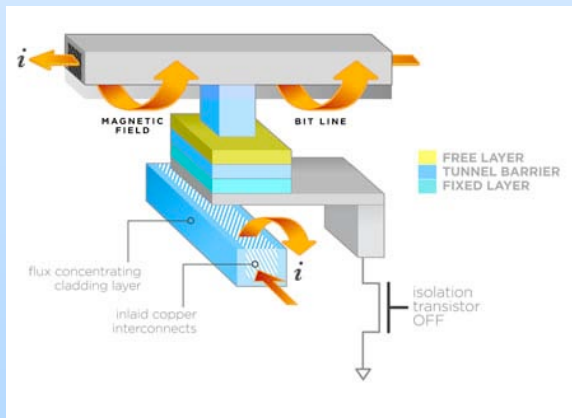
# MTJ Drawbacks

## Scaling Issues

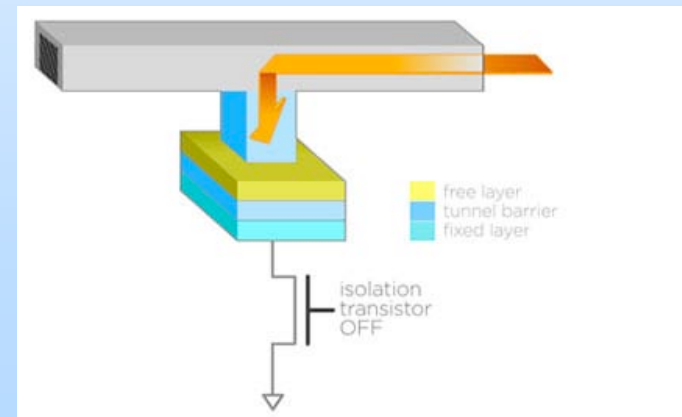
- Smaller bits are more susceptible to thermal fluctuations



## Complicated Lithography



1<sup>st</sup> Gen: MTJ Cell



2<sup>nd</sup> Gen: STT Cell

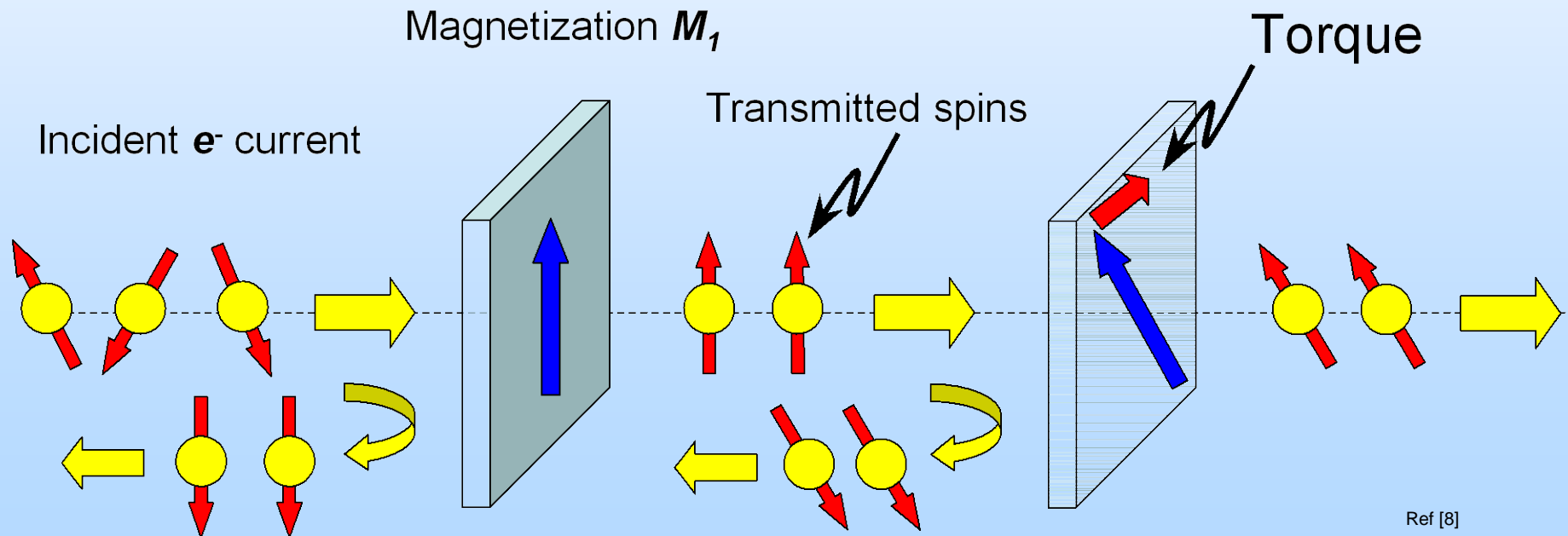
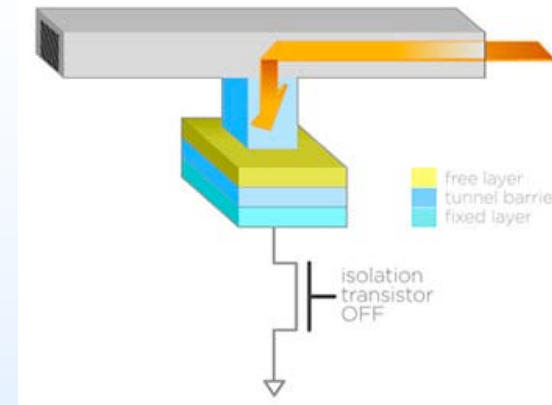


# MRAM Future: Thermally Assisted Switching (TAS)

- **Idea is to heat the cell, which lowers the strength of the required magnetic fields for switching**
- **Advantages:**
  - **Eliminates write selectivity problems: write select is temperature driven**
  - **Lower power: only one magnetic field required for write**
  - **It is thermally stable due to the exchange bias of the storage layer.**
- **Main Advocate: Crocus (Spintec spin-off): Just received \$300M to build factory in Russia.**

# MRAM Future: Spin Torque Transfer (STT)

- **Advantages:**
  - **Lower Power Consumption**
  - **Better Scalability**
  - **Simpler Cells**

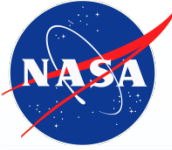


The timing diagram illustrates the relationship between the address (A), chip enable (E), write enable (W), data input (D), and data output (Q) signals. Key timing parameters are defined as follows:

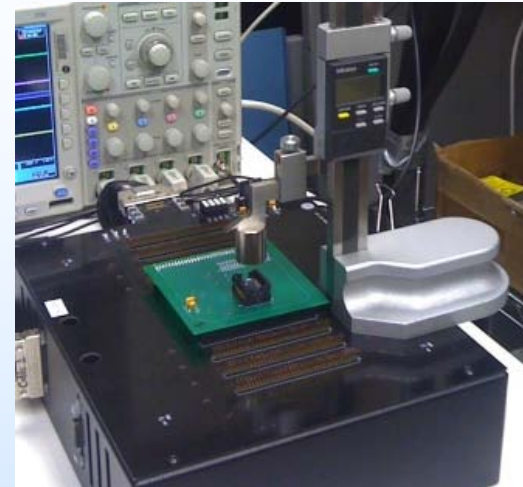
- $t_{AVAV}$ : Address Valid to Address Valid (Setup and Hold)
- $t_{AVWH}$ : Address Valid to Write Enable (Setup)
- $t_{WHAX}$ : Write Enable High to Address Valid (Setup)
- $t_{WLEH}$ : Write Enable Low to Address Valid (Setup)
- $t_{WLWH}$ : Write Enable Low to Write Enable High (Pulse Width)
- $t_{AVWL}$ : Address Valid to Write Enable Low (Setup)
- $t_{DVWH}$ : Data Valid to Write Enable High (Setup)
- $t_{WHDx}$ : Write Enable High to Data Valid (Setup)
- $t_{WLOZ}$ : Write Enable Low to Output Low-Z (Setup)
- $t_{WHQX}$ : Write Enable High to Output High-Z (Setup)

The diagram shows the timing of the AD9080 during a read operation. The signals involved are Address, CS (Chip Select), OE (Output Enable), Data out, and Vcc Current. The Address signal is shown as a bus with a read operation indicated by a double-headed arrow. The CS signal is active-low, and the OE signal is active-low. The Data out signal shows the data being read, with a period labeled 'Valid Data'. The Vcc Current signal shows the power supply current, which transitions from  $I_{CC}$  to  $I_{CB}$  at 50% duty cycle. Various timing parameters are labeled:  $t_{RC}$  (Address setup/hold),  $t_{AA}$  (CS setup),  $t_{CO}$  (CS hold),  $t_{HZ(3,4,5)}$  (CS hold after high-Z),  $t_{OE}$  (OE setup),  $t_{OLZ}$  (OE hold),  $t_{LZ(4,5)}$  (OE hold after low-Z),  $t_{PU}$  (Data out setup),  $t_{PD}$  (Data out hold), and  $t_{OH}$  (Data out hold after high-Z).

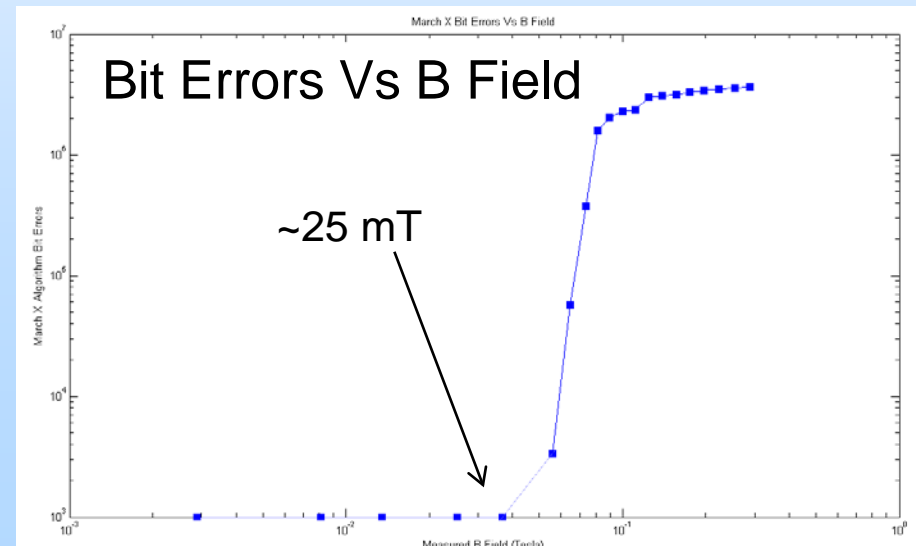
# Device Reliability: 1 Mb Everspin (JPL)



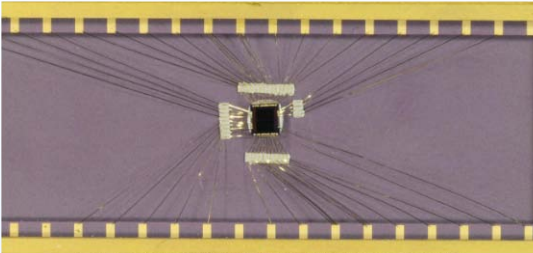
- Unlimited Endurance
- 20+ year Retention
- Low susceptibility to external magnetic fields
- -55 to 125 C operation (E2V upscreen)
  - Sold by Everspin as -45 to 130C



B field measurements at JPL



# Radiation Effects - JPL



***A 1 Mbit MRAM die packaged in a 40-pin dual-in-package (DIP) for SEL testing (top) and thin-small-outline-package (TSOP) for TID testing (bottom).***

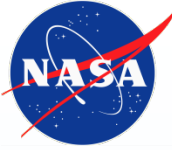
Run #	Device	Energy (MeV/AMU)	Energy (MeV)	Ion	Eff. LET	Run Time (s)	Fluence
1	1	25	1766	Kr	21.2	177	2.0E+05
2	1	25	1766	Kr	21.2	242	3.0E+06
3	1	25	1766	Kr	21.2	45	5.0E+06
4	1	25	313	Kr	39	54	5.0E+06
5	1	25	1077	Xe	56	51	5.0E+06
6	2	25	1077	Xe	56	61	5.0E+06
7	2	25	1077	Xe	56	62	5.0E+06
8	2	15	2429	Au	84.1	89	1.0E+07
9	3	15	2429	Au	84.1	79	1.0E+07
10	4	15	2429	Au	84.1	54	1.0E+07

Ref [10]

***Ion beams used for SEL testing.  
No latchup observed during any testing.***

# Memory Comparison

	SRAM	DRAM	NOR Flash	NAND Flash	FRAM	PRAM	MTJ MRAM	STT MRAM
Density	144 Mb	8 Gb	1 Gb	64 Gb	4 Mb	512 Mb	16 Mb	Gb?
Access Time	<1 ns	260 ps	25 ns	20 ns	55 ns	16 ns	35 ns	<10?
Standby I (mA)	2	150	<1	<1	<1	<1	<1	<1
Read I (mA)	100	1000	20	25	<10	16	30	15?
Write I (mA)	100	1000	50	25	<10	20	30	15?
Endurance	Infinite	Infinite	100k	0.5-100k	10 <sup>14</sup>	10 <sup>6</sup>	Infinite	Infinite
Retention	~0	~0	>10 yrs	>10 yrs	>10 yrs	>10 yrs	>20 yrs	>20 yrs
Cell Size (F <sup>2</sup> )	100	8	6	5	10	6	10	<4?
Rad-Hard Cell	✗	✗	✗	✗	✓	✗	✓	✓
Cost/Mb (\$)	2	.0004	.01	.0002	10	.05	1.5	?

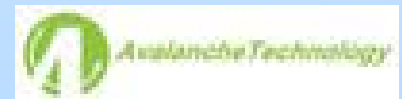
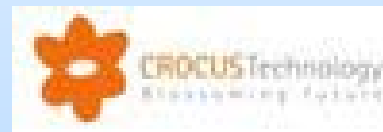


# Applications

*Wherever nonvolatility, quick booting, high endurance, and/or radiation-hardness are important.*

- **Home Computing**
  - Quick boot discs, similar to Flash
- **Mobile Computing**
  - Nonvolatility
- **Military/Space**
  - Nonvolatile, Rad-Hard
- **RFID**
  - Embedded MRAM

# MRAM Players (Past and Present)





# MRAM Areas of Focus

## Commercial MTJ Vendors

- Everspin
- E2V (Everspin Upscreen)

## MTJ IP

- NVE
- Spintec

## Inactive

- Motorola (2005, spun off Freescale)
- Freescale (2008, spun off Everspin)
- Infineon (~2006)
- Cypress (2005)
- Micron (MTJ) (2003)

## Commercial Rad-Hard MTJ

- Honeywell
- Aeroflex

## Thermally Assisted Technology (TAS) R&D

- Crocus, IBM
- Spintec

## Spin Transfer Torque (STT) R&D

- IBM
- Samsung
- Hynix-Grandis
- Everspin
- Avalanche Technology (CA start-up)
- Spin Transfer Technologies (NYU start-up)
- Intel
- NEC
- Renesas
- Fujitsu
- Toshiba
- Micron, A\*Star (Singapore)



# MRAM Product Roadmap

Year	Device	Manufacturer
2004	4 Mb MTJ	Freescale
2005	1 Mb MTJ Rad-hard	Honeywell
2005	STT MRAM Prototype	Sony
2009	32 Mb STT MRAM Prototype	Hitachi
2010	4/16 Mb MTJ Rad-hard	Aeroflex
2012?	16/64 Mb Rad-hard QML Class V	Aeroflex/Honeywell
2015?	Gb STT	Toshiba

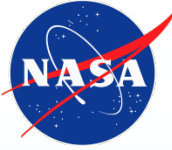


# Flight Heritage - SpriteSat

- SpriteSat – Tohoku University, Japan
- Various Payloads/Launches Since 2008
- 4 Mb Freescale devices
- Replacing Flash and SRAM with MRAM

## Flight Heritage – CubeSat - COVE (JPL)

- Launch October 2011 (Ref: 11)
- CubeSat On-board Processing Validation Experiment, “COVE”
- Secondary Payload on University of Michigan M-Cubed CubeSat
- Included:
  - Xilinx Virtex-5QV FPGA
  - Everspin MR4A16B MRAM (4 Mb)
  - Numonyx P5QPCM PRAM (128 Mb)
- First attempt: NPOESS Preparatory Project (NPP)
- M-Cubed did not separate from another CubeSat, Explorer 1-Prime
  - *Although beacons have been heard, University of Michigan team has been unable to send commands to satellite.*



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