

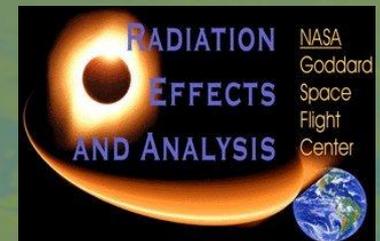


HiREV NEPP Technical Interchange: "CMOS Physics of Failure Lifetime Modeling"

Jon Osborn, Chris Paul, Jim Dixon, John Scarpulla,
Ron Laco, Dave Eccles
The Aerospace Corporation

June 13, 2012

Presented to NASA NEPP
Meeting at NASA GSFC



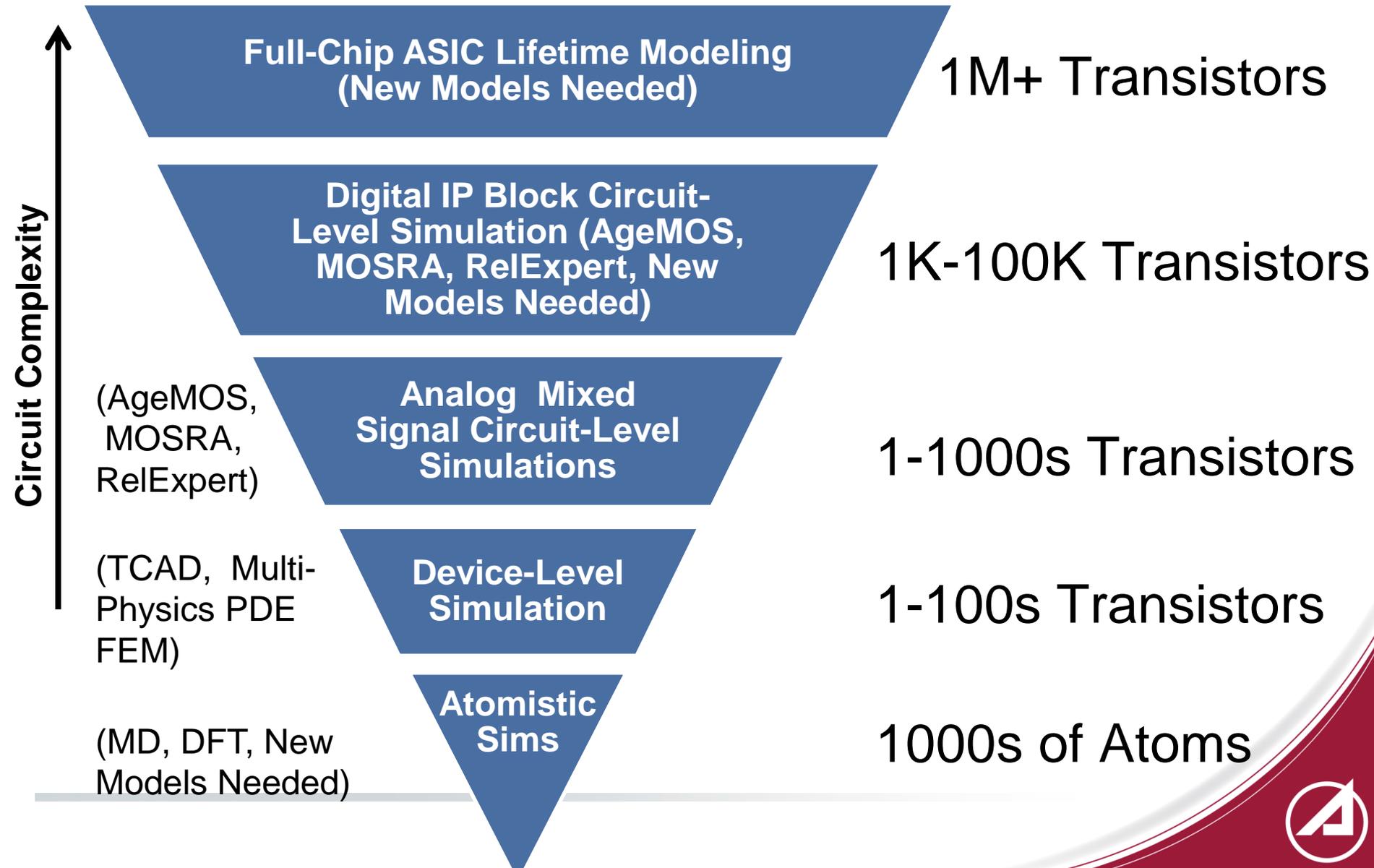
Topics of Discussion

- Multi-Level PoF Modeling & Simulation
- HiREV nano-CMOS Road-Map
- FY12 Lifetime Focus Areas
- CMOS Failure Modes Under Investigation
- Analog Mixed Signal Lifetime Simulation
- 90nm CMOS ASIC Full-Chip Lifetime Model
- Looking Forward

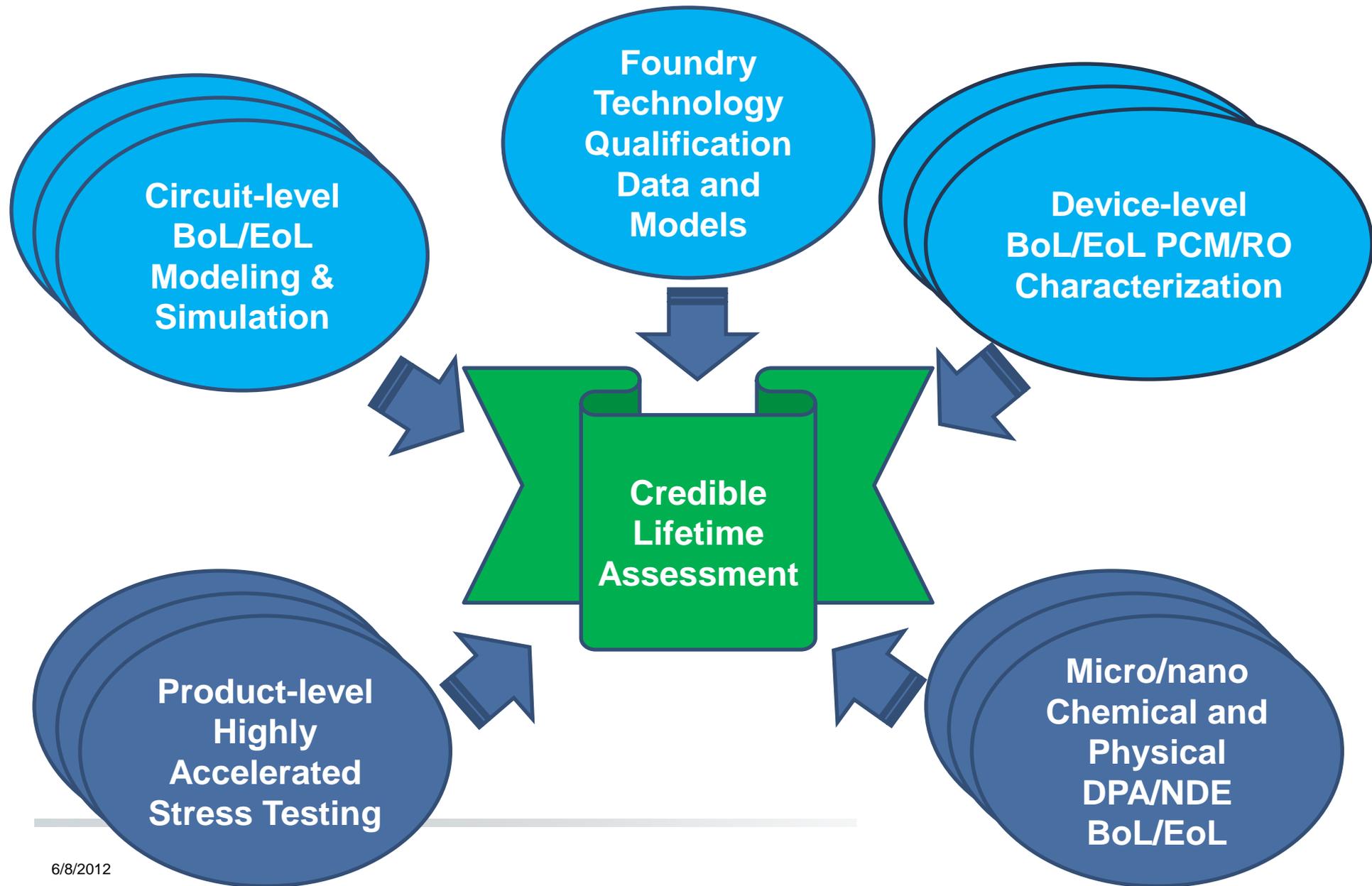




Multi-Level PoF Lifetime Modeling



FY12 HiREV/Aerospace Focus Areas



CMOS Failure Modes Under Investigation

- Front-End-of-Line (FEOL)
 - *Hot Carrier Injection (HCI)*
 - *Negative Bias Temperature Instability (NBTI)*
 - *Stress Induced Leakage Current (SILC)*
 - *Gate Oxide Time Dependent Dielectric Breakdown (GO-TDDB)*
- Back-End-of-Line (BEOL)
 - *Electromigration (EM)*
 - *Stress Voiding (SV)*
 - *Contact & Via Opens*
 - *Inter-level Dielectric TDDB (ILD-TDDB)*
- Radiation Degradation
 - *Total Ionizing Dose (TID)*
 - *Rad/Rel Synergistic Effects*
- Advanced Packaging
 - *Ceramic Strength*
 - *Interconnect Metallurgy*
 - *Adhesive Polymers*



Atomistic simulation of HCI degradation in CMOS

FY12 Mid-Year Accomplishment



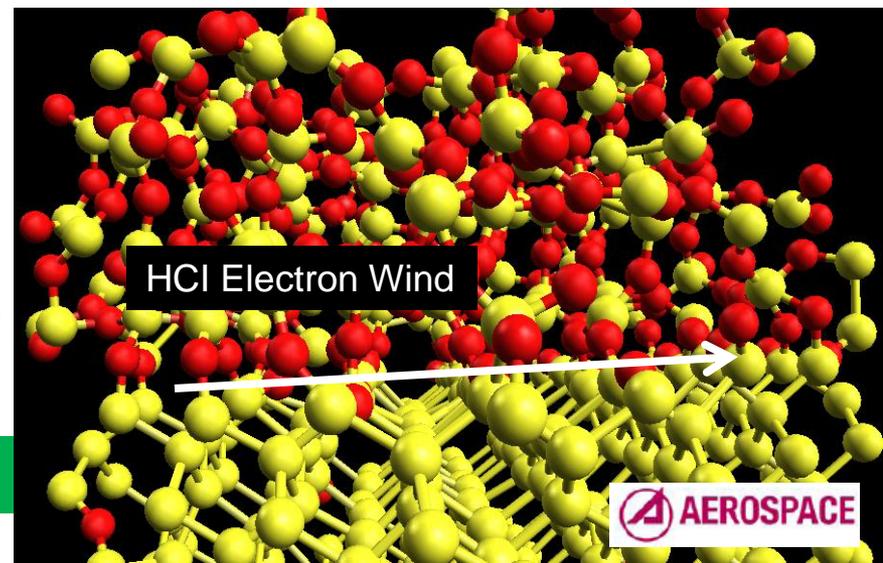
Goal: Apply atomistic simulation techniques to understand the generation and action of interface and boundary defects resulting from hot carrier injection (HCI) within the channel of CMOS transistors

Methodology:

- Molecular dynamics (MD) of initial interface structure
- Density functional theory (DFT) electronic structure calculations for latent defects (e.g. strained bonds, Si-H, etc...)
- Quantum analysis of latent defect hot carrier capture cross section
- DFT-MD simulations of atomic relaxations following carrier capture
- MD simulations of large scale oxide relaxation
- Analysis of defect trapping/charging for end-to-end degradation predictions

Current Status:

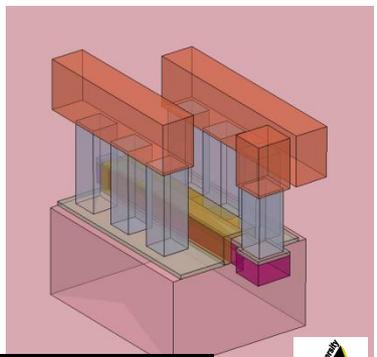
- CMOS, 2 nm thick gate oxide, polySi gate
- Amorphous gate oxide generated using MD
- Plane wave DFT calculations of defects



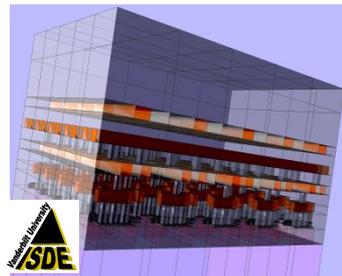
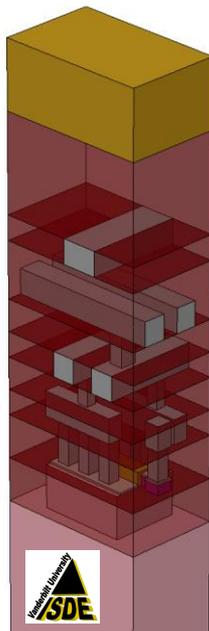
Need MD/DFT Model for Each Failure Mode



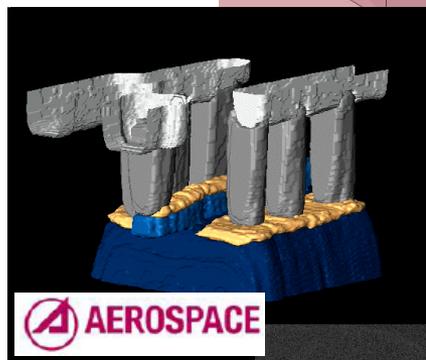
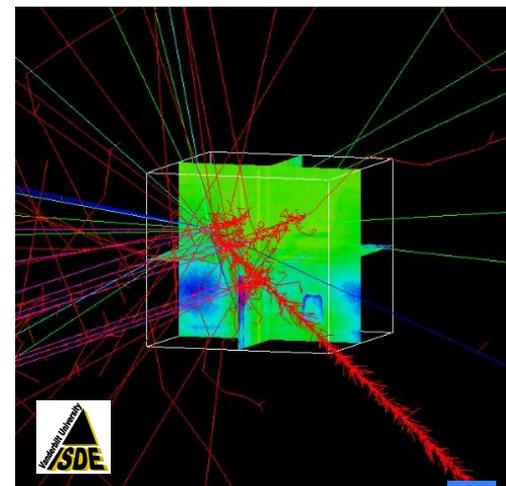
FY11 HiREV Vanderbilt University Collaboration, nano-scale 3D Imaging → TCAD → SEE Response



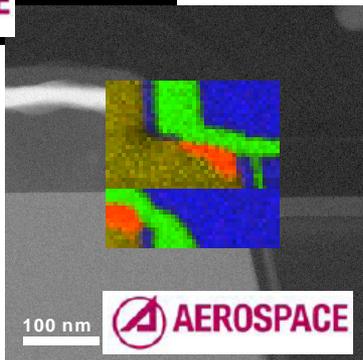
3D TCAD Model Created for MRED



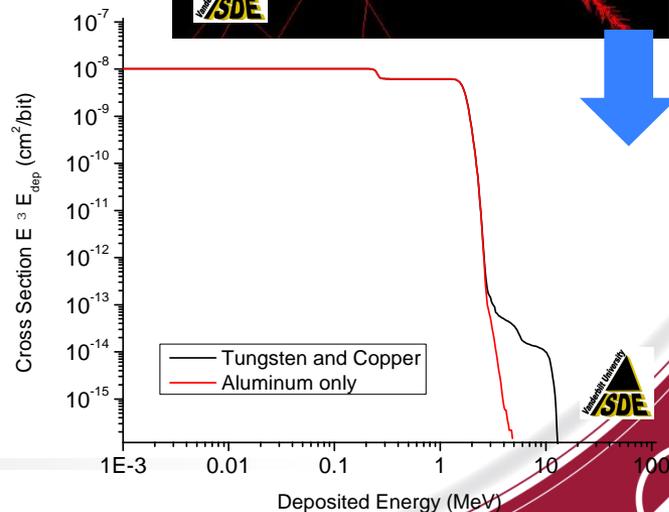
Simulate Single Event Energy Deposition for Al vs. W



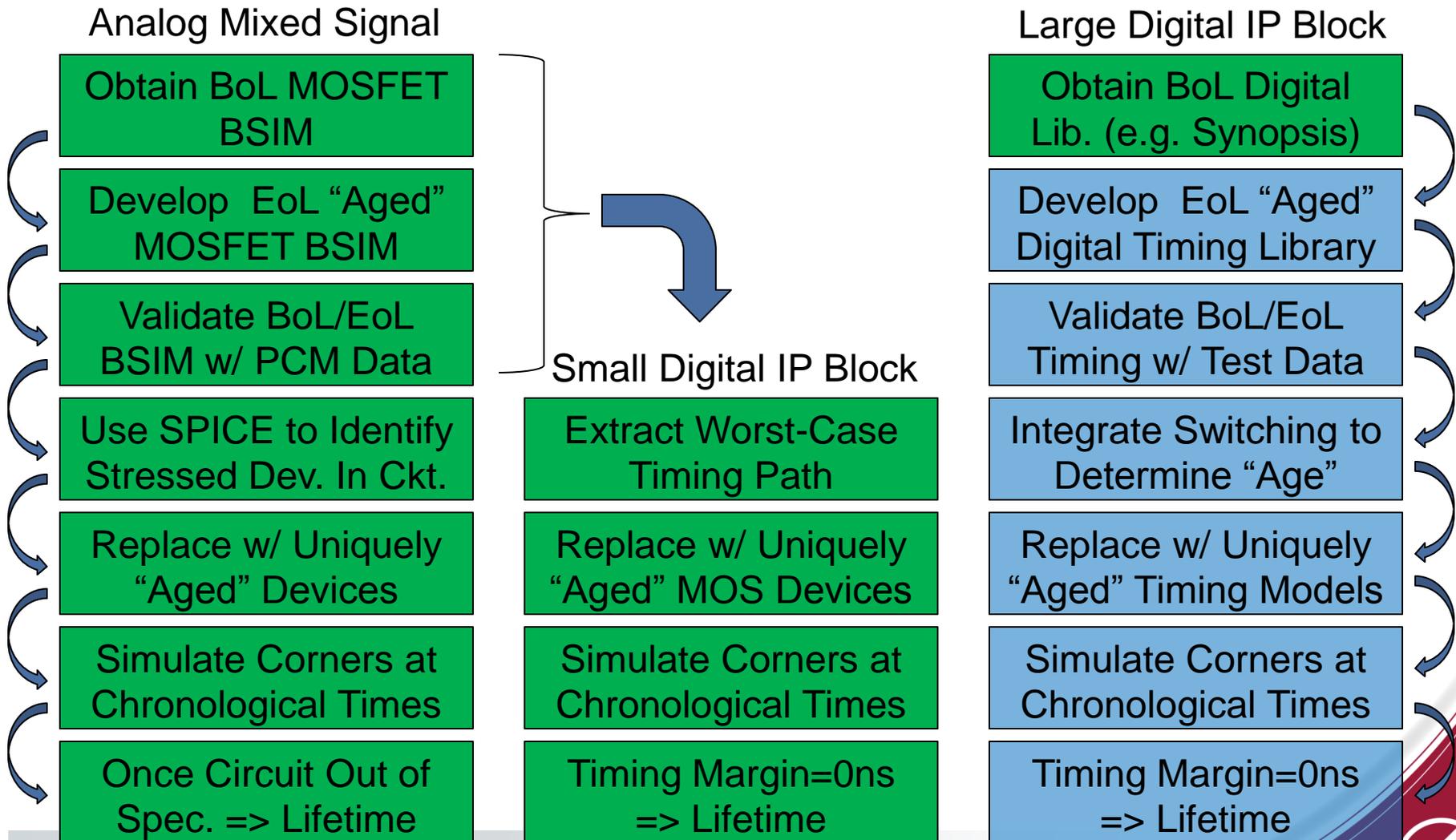
Aerospace 3D Device and Materials Map



Increase Error Rate for High Qcrit Logic



“Bottoms-Up” MOSFET Device, Analog Mixed Signal and Digital Circuit Aging Process





130nm Device Aging Simulation Methodology

- Develop a device aging calculation for each reliability wear out mechanism based on the physical understanding of the mechanism, data and models available from foundry, literature, and our experimental data
- Review the operating conditions of each transistor in the circuit to identify those that are expected to suffer degradation due to NBTI, HCI, and TDDB
- Project changes in the BSIM (Berkeley Short-channel IGFET Model) models used for these selected transistors at 10, 20 and 40 years to simulate the effects of aging on the circuit
- Compare Beginning of Life (BoL) Simulations with “aged” End Life (EoL) models to simulate degraded circuit performance that illustrates the aging effect





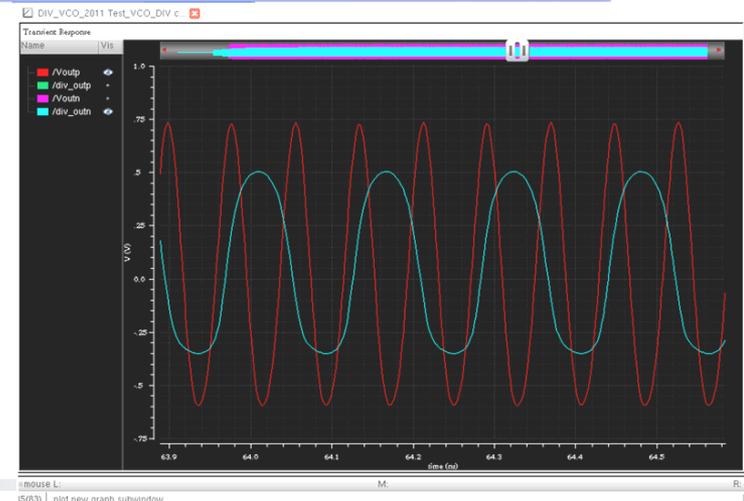
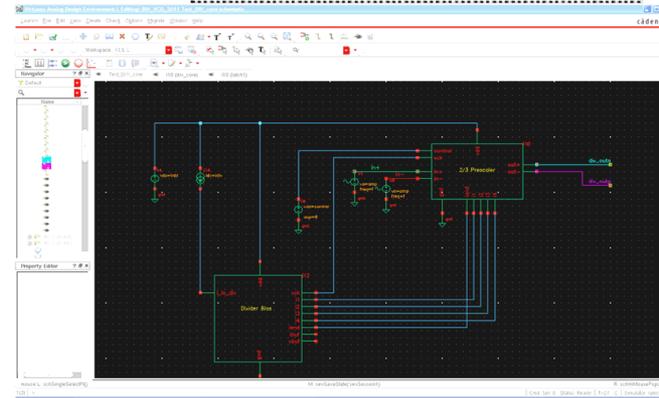
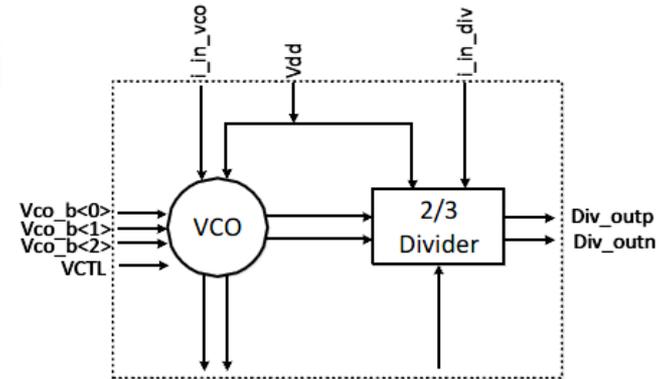
Ex: Analog Mixed Signal Circuit VCO / Divider Aging

• Inputs

- $V_{dd} = 1.5V$
- 3 Bit Programmable VCO Frequency tuning (8GHz)
- Analog input for Fine Tuning
- Control Bit Selects Divide by 2 or 3
- VCO Current Reference
- Divider Current Reference

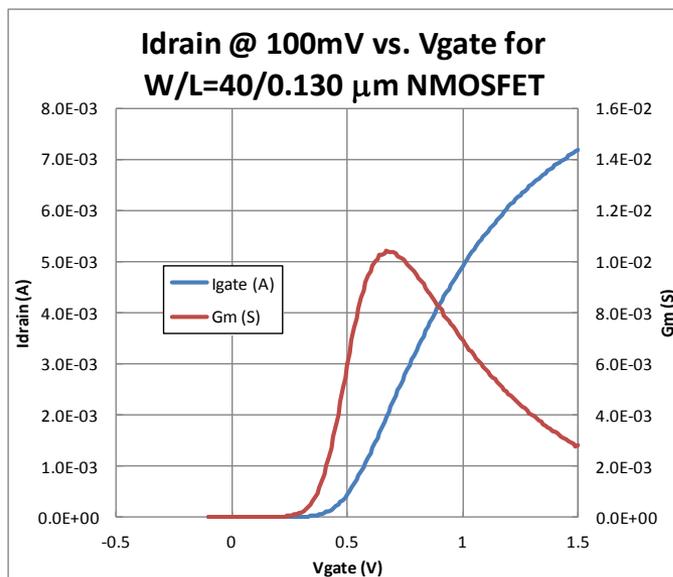
• Output

- VCO Differential Output
- Divider Differential Output

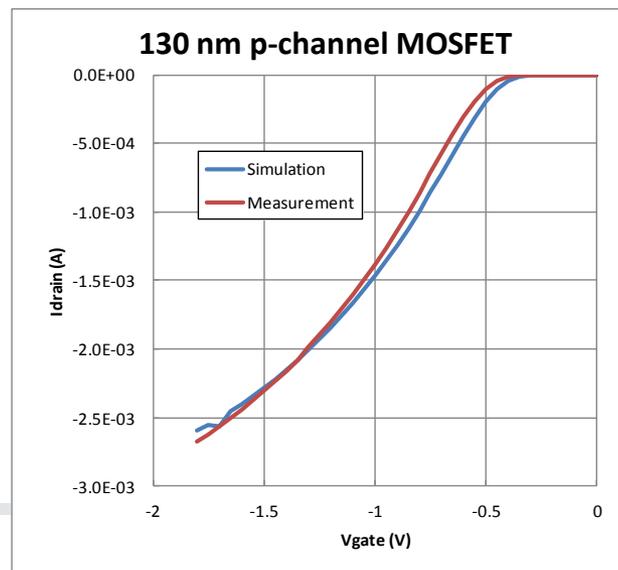
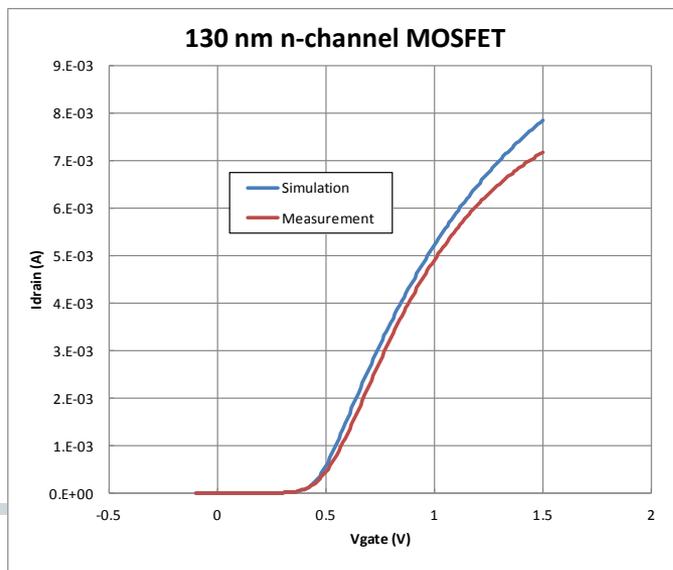


Characterization of 130 nm 8rf Models

Measurement v. Simulation for BoL NMOS and PMOS



- In this example the V_{th} is 0.432 V, G_{mmax} is 10.4 mS
- BSIM 3f5 Level 8 Foundry BoL Model





Ex: Operating Point of 130-nm MOSFETs in Circuit

FET Number	Circuit	Type	W	L	nf	m	DC				AC (peak to peak values)				
							Vs	Vg	Vd	Id(mA)	Vs	Vg	Vd	Id(mA)	Freq (GHz)
1	VCO_10GHz Ibias	pfet_rf	20	0.25	5	1	1.5	0.89	0.89	0.35	0	0	0	0	0
2	VCO_10GHz Ibias	pfet_rf	500	0.25	125	1	1.5	0.888	0.7714	8.695	0	0	0	0	0
3	VCO_10GHz Ibias	pfet_rf	38.5	0.25	10	1	1.5	0.89	0.522	0.7185	0	0	0	0	0
4	VCO_10GHz Ibias	pfet_rf	120	0.12	10	1	1.5	1.005	1.005	0.7986	0	0	0	0	0
5	VCO_10GHz Ibias	pfet_rf	120	0.12	10	1	1.5	1.005	1.005	0.7986	0	0	0	0	0
6	VCO_10GHz Ibias	nfet_rf	16	0.4	4	1	0	0.5521	0.522	0.2341	0	0	0	0	0
7	VCO_10GHz Ibias	nfet_rf	16	0.4	4	1	0	0.5521	1.005	0.7986	0	0	0	0	0
8	VCO_10GHz Ibias	nfet_rf	860	0.4	215	1	0	0.5521	0.09374	21.41	0	0	0	0	0
9	VCO_10GHz Ibias	nfet_rf	16	0.4	4	1	0	0.5521	1.005	0.7986	0	0	0	0	0
10	VCO_10GHz Ibias	nfet_rf	540	0.4	135	1	0	0.5521	0.117	15.86	0	0	0	0	0
11	VCO_10GHz_ControlBits	pfet	2	0.12	1	1	1.5	0	1.5	0	0	0	0	0	0
12	VCO_10GHz_ControlBits	pfet	2	0.12	1	1	1.5	1.5	0	0	0	0	0	0	0
13	VCO_10GHz_ControlBits	pfet	2	0.12	1	1	1.5	1.5	0	0	0	0	0	0	0
14	VCO_10GHz_ControlBits	pfet	2	0.12	1	1	1.5	1.5	0	0	0	0	0	0	0
15	VCO_10GHz_ControlBits	pfet	2	0.12	1	1	1.5	1.5	0	0	0	0	0	0	0
16	VCO_10GHz_ControlBits	pfet	2	0.12	1	1	1.5	1.5	0	0	0	0	0	0	0
17	VCO_10GHz_ControlBits	pfet	2	0.12	1	1	1.5	1.5	0	0	0	0	0	0	0
18	VCO_10GHz_ControlBits	nfet_inh	1	0.12	1	1	0	0	1.5	0	0	0	0	0	0
19	VCO_10GHz_ControlBits	nfet_inh	1	0.12	1	1	0	1.5	0	0	0	0	0	0	0
20	VCO_10GHz_ControlBits	nfet_inh	1	0.12	1	1	0	1.5	0	0	0	0	0	0	0
21	VCO_10GHz_ControlBits	nfet_inh	1	0.12	1	1	0	1.5	0	0	0	0	0	0	0
22	VCO_10GHz_ControlBits	nfet_inh	1	0.12	1	1	0	1.5	0	0	0	0	0	0	0
23	VCO_10GHz_ControlBits	nfet_inh	1	0.12	1	1	0	1.5	0	0	0	0	0	0	0
24	VCO_10GHz_ControlBits	nfet_inh	1	0.12	1	1	0	1.5	0	0	0	0	0	0	0
25	VCO_Core	nfet_rf	24	0.12	6	1	0	0.77	0.77	4.347	0	1.5	1.5	12.5	12.75
26	VCO_Core	nfet_rf	24	0.12	6	1	0	0.77	0.77	4.347	0	1.5	1.5	12.5	12.75
27	VCO_MIM_Bank	nfet_rf	8	0.12	2	1	1.5	0	1.5	0	0	0	0	0	0
28	VCO_MIM_Bank	nfet_rf	8	0.12	2	1	1.5	0	1.5	0	0	0	0	0	0
29	VCO_MIM_Bank	nfet_rf	8	0.12	2	1	1.5	0	1.5	0	0	0	0	0	0
30	VCO_MIM_Bank	nfet_rf	8	0.12	2	1	0	1.5	0	0	0	0	0	0	0
31	VCO_MIM_Bank	nfet_rf	8	0.12	2	1	1.5	0	1.5	0	0	0	0	0	0
32	VCO_MIM_Bank	nfet_rf	8	0.12	2	1	1.5	0	1.5	0	0	0	0	0	0
33	VCO_MIM_Bank	nfet_rf	8	0.12	2	1	1.5	0	1.5	0	0	0	0	0	0
34	VCO_Prefbuf	nfet_rf	32	0.12	32	1	0.1177	1.005	0.996	7.928	0	1	0.6	18	12.75
35	VCO_Buf	nfet_rf	40	0.12	32	1	0.09374	1.005	0.9438	10.71	1	0.4	1.5	4	12.75
36	DIV_Bias	nfet_rf	40	0.25	10	1	0	0.3396	0.3396	0.2	0	0	0	0	0
37	DIV_Bias	nfet_rf	200	0.25	50	1	0	0.3396	0.473	1.128	0	0	0	0	0
38	DIV_Bias	nfet_rf	400	0.25	100	1	0	0.3396	0.2095	1.905	0	0	0	0	0
39	DIV_Bias	nfet_rf	400	0.25	100	1	0	0.3396	0.2027	1.894	0	0	0	0	0
40	DIV_Bias	nfet_rf	400	0.25	100	1	0	0.3396	0.1973	1.885	0	0	0	0	0
41	DIV_Bias	nfet_rf	400	0.25	100	1	0	0.3396	0.1925	1.877	0	0	0	0	0
42	DIV_Bias	nfet_rf	28	0.25	7	1	0	0.3396	0.698	0.1686	0	0	0	0	0

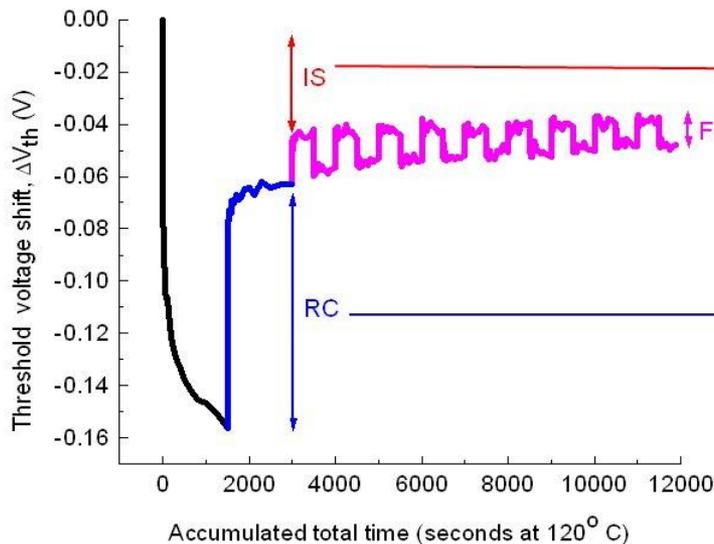
NBTI Risk

HCI Risks





Current Activity: CMOS-Based Physics of Failure - NBTI



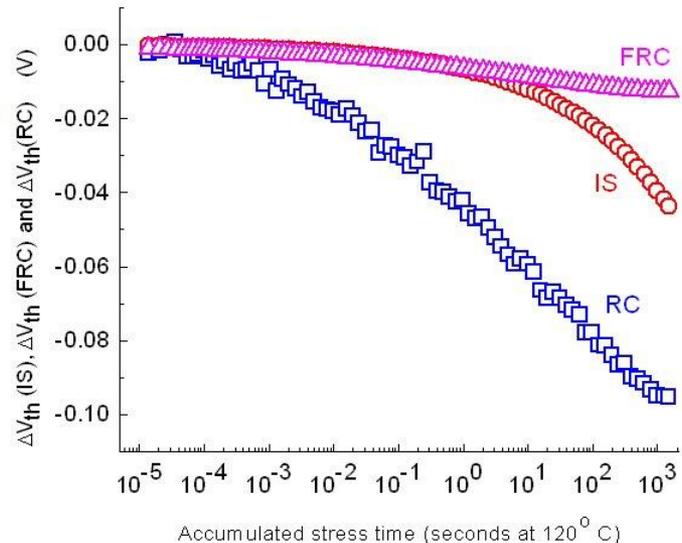
Breaking of Si-H bonds creating positive interface states

Hole traps in the oxide which require positive field to detrapp/neutralize.

Hole trapping in the oxide by preexisting defects detrapp when field drops to zero

IBM 130 nm bulk technology
Nitrided SiO₂ gate dielectric

$V_{gs} = -3.25$ volts for $0 < t < 1500$ s
 $V_{gs} = 0.00$ volts for $1500 < t < 3000$ s
 $V_{gs} = 1.50$ for $3000 < t < 3500$ s
 $V_{gs} = -1.00$ for $3500 < t < 4000$ s
 Etc



Constant stress $V_{gs} = -3.25$ volts

Point of Contact: Rod Devine (505)-846-4822
 roderick.devine.ctr@kirtland.af.mil

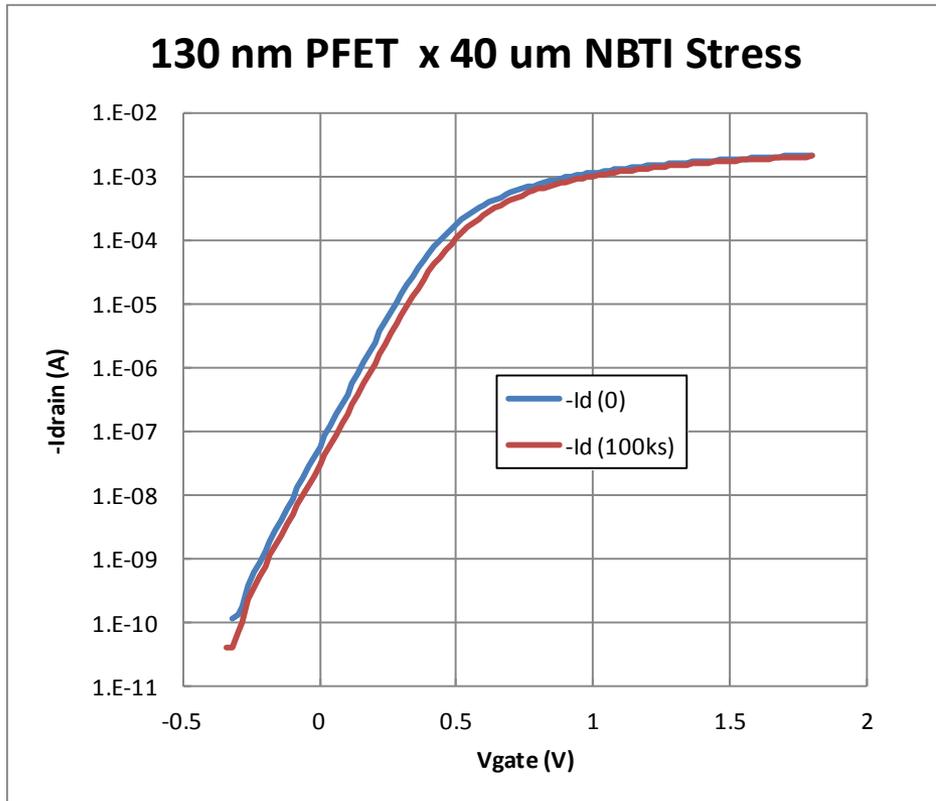
Question: Does this extend beyond 90nm?

To appear in the Proceedings of
 2012 ICDIM [Physica Status Solidi]





130nm NBTI Stress Measurement



- Device stressed at $V_{\text{gate}} = -2.3$ V at a temperature of 140 C
- Very little degradation observed even at 100 ks
- Initial BSIM model matches the initial measurement as well as it matches the post-stress measurement
- The 130nm 8rf PFET is insensitive to NBTI under these circuit conditions

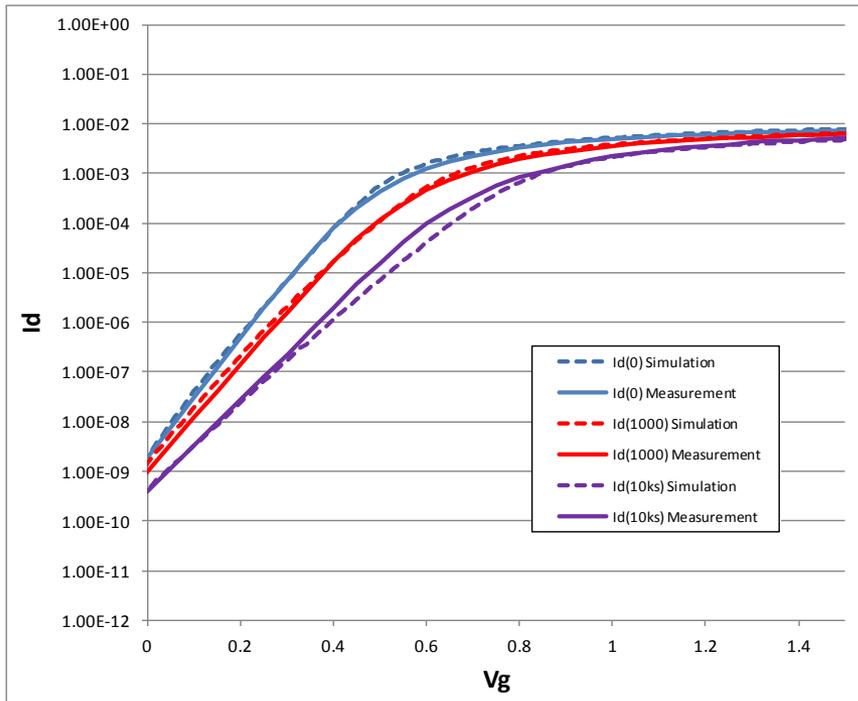


HCI Aged 130nm 8RF NFET Model Validation

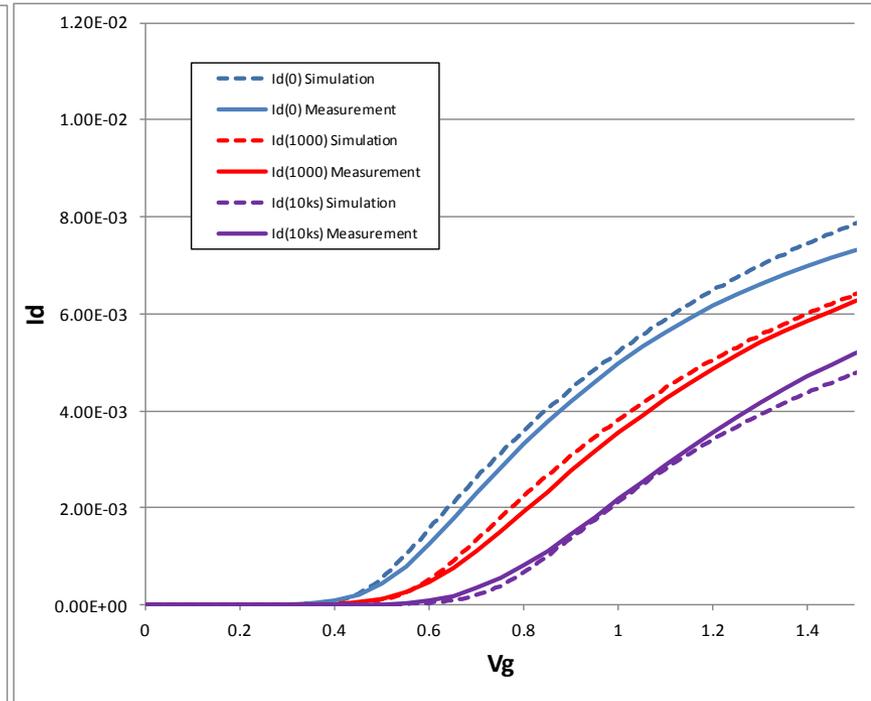


- HC Stress data for $V_d=2.5$ V and $V_g=1.25$ V
- BSIM4 Models were matched to measured devices by parametric shifts in model parameters CIT, V_{TH} , and U_0
 - *The threshold voltage increases with HCI stress due to charge trapping*
 - *Decreases in transconductance with aging were represented by a decrease in mobility resulting also from an increase in interface traps*
 - *The sub-threshold slope decreases with an increase in interface state density (CIT)*
- Results show good model correlation with this approach

40um x 0.12um NFET Id-Vg (Log plot)



40um x 0.12um NFET Id-Vg (Linear plot)



Modeling the lifetime for a particular circuit design, requires knowledge about the devices from that process lot and detailed simulation





HCI/NBTI Aging Simulation Process

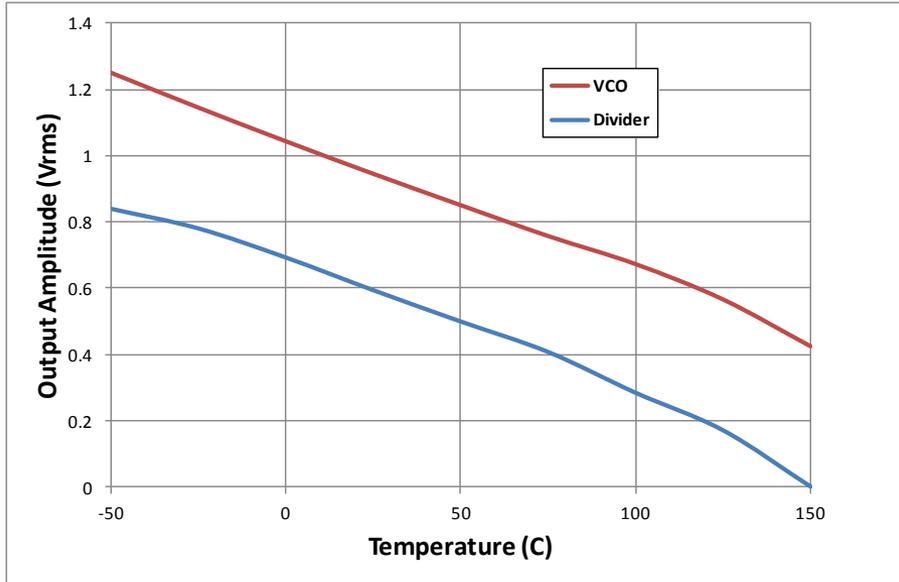
- Establish BoL Circuit Sensitivities to Voltage, Temperature and Process
- Each transistor in the VCO/ Divider Circuit was assigned a separate BSIM4 model instance.
- Variables were added to each BSIM4 model to account for parametric shifts from HCI/ NBTI stress. The variables are contained in a separate “age” file that can be efficiently updated when new calculations are available.
- Parametric Shift variables included in the model are:
 - *Mobility (U_0)*
 - *Threshold Voltage(V_{TH0})*
 - *Interface Trap Capacitance (CIT)*
- The “aged” models were validated by comparing simulated NFET Id-Vg curve traces to measurements taken from actual aged devices.
- AC and DC bias conditions for each transistor in the circuit were tabulated and used to calculate HCI/NBTI stress and parameter shifts at 0, 10, 20 and 40 years .
- Circuit was run with updated parametric shift variables





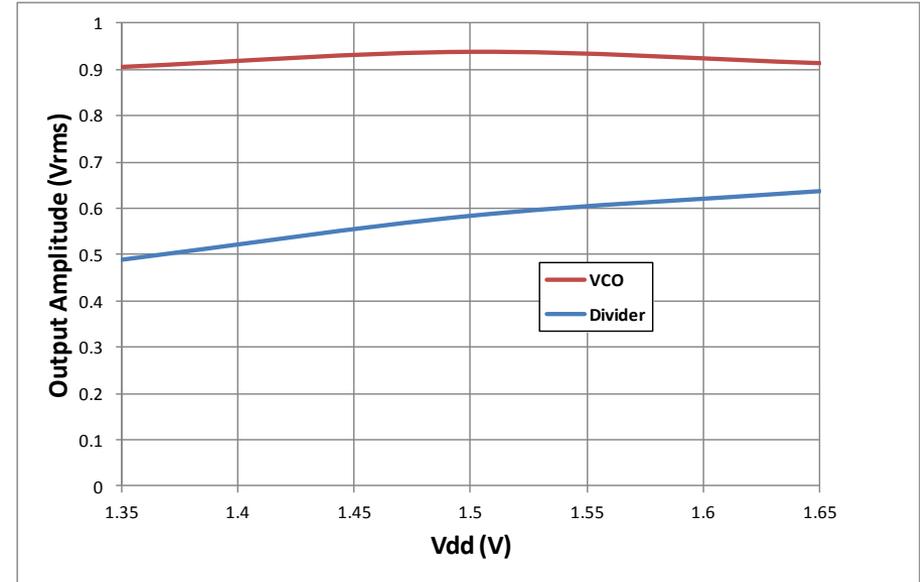
VCO / Divider Sensitivities

Temperature Sensitivity



The slope of the curve is 3.7mV/°C. To remain within the min/max data sheet specifications for output amplitude, the VCO/Divider would be restricted to an 8°C temperature range.

Bias Sensitivity



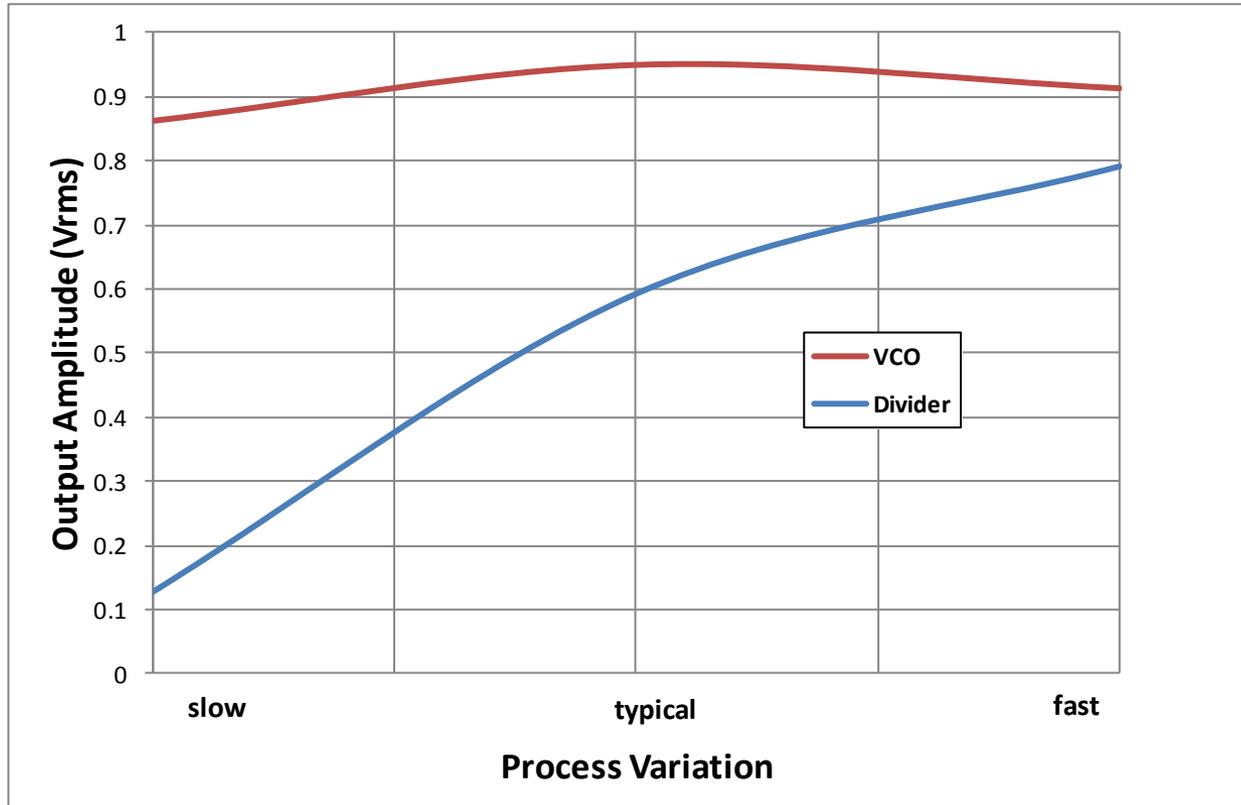
The Divider output varies by 0.5mV / 1mV Vdd. To remain within the min/max data sheet specifications for output amplitude, Vdd would be restricted to +/- 40mV.

Simulated at BOL, 27C, and nominal process





VCO / Divider Process Sensitivity



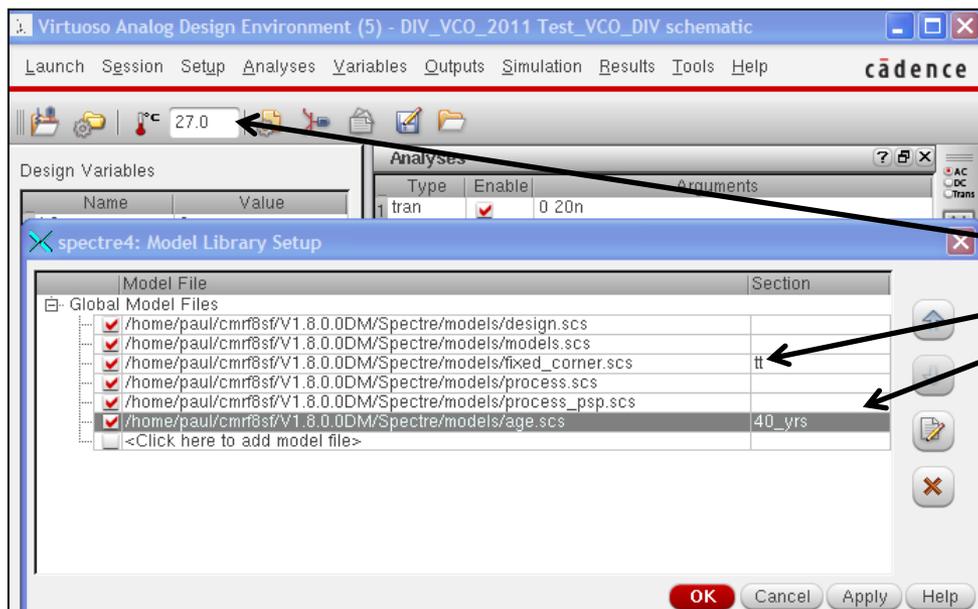
The Divider output varies by 660mV. To remain within the min/max data sheet specifications for output amplitude, the VCO/Divider would be restricted to within 6% of the process center.

Simulated at BOL, 27C, and nominal bias and process





HCI/NBTI Aging Simulation Automation



Circuit age, temperature and process parameters can be selected from a pulldown menu

```

section 40_yrs
parameters
+ vth_age_25 = 0.4
+ vth_age_26 = 0.4
+ u0_age_25 = -28
+ u0_age_26 = -28
+ int25      = 0.03
+ int26      = 0.03
endsection 40_yrs
    
```

Sample age model file with Vth, U0 and CIT parameter shifts for transistors 25 and 26





130-nm AMS Sims Summary

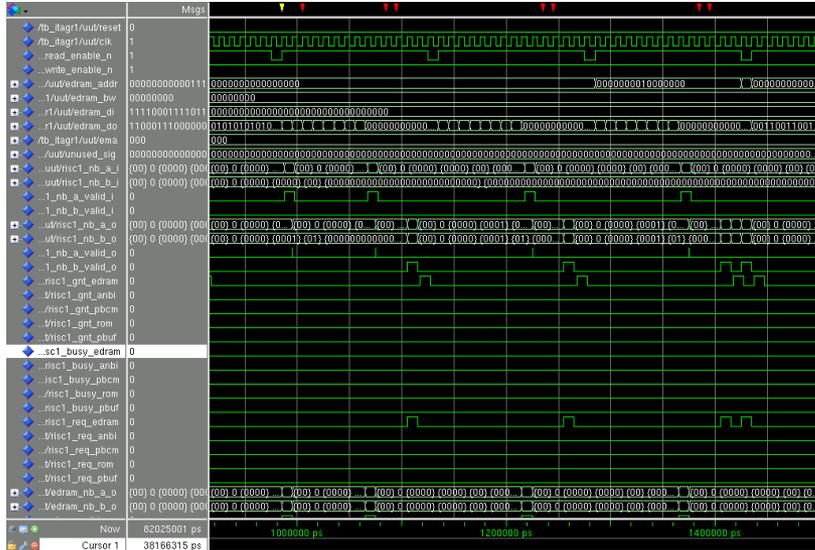
- The output amplitudes of the VCO and Divider are sensitive to shifts in temperature, process and voltage
- The time to failure depends on the use conditions and definition of failure
- The process for simulating the 130nm circuit after aging is operating efficiently and providing good correlation to measured data
 - *Performed simulations for 0, 10, 20, 40 years under worst-case bias/temperature conditions*
- Next Steps Include:
 - *Characterize phase noise as a function of age*
 - *Provide Bias/Temperature Recommendation for Life Testing Activity*
 - *Repeat for 90-nm 9SF AMS and 90/65-nm Digital Only Designs*



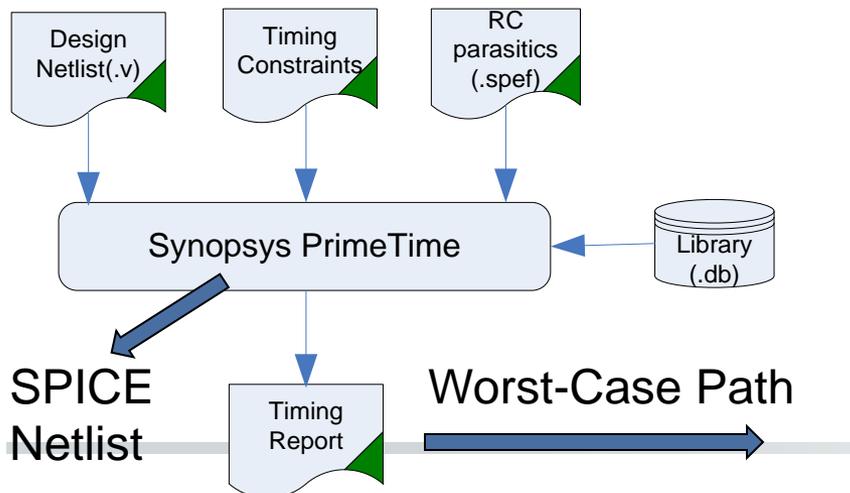


90nm Digital ASIC Circuit Aging Status

Functional Logic Simulation



- Received 90nm design database
- Full circuit logic simulation(s) performed
- Primitime Static Timing Analysis Done
- Primitime Si SPICE Netlist extraction of worst-case path(s) complete
- HSPICE Simulation of timing paths begun
- 90nm Aged MOS models under development



```

clock sysclk (rise edge)          7.19000    7.19000
clock source latency              0.00000    7.19000
PAD_clk (in)                     0.00000    7.19000 r
PAD_clk (net)                    1          0.00003 & 7.19003 r
clk_pad/PAD (SS_INBUF)           0.57724 & 7.76727 r
clk_pad/O1 (SS_INBUF)           1          0.00003 & 7.19003 r
clk (net)                        1          0.01825 & 7.78552 r
clk_L1_I0/in0 (inv_30x)          13         0.25742 & 8.04294 f
clk_L1_I0/y (inv_30x)            13         0.00822 & 8.05117 f
clk_L1_N0 (net)                  13         0.23654 & 8.28770 r
clk_L2_I2/in0 (inv_30x)          22         0.05380 & 8.34150 r
clk_L2_I2/y (inv_30x)            22         0.25680 & 8.59830 r
clk_L2_N2 (net)                  22         0.00000 & 8.59830 r
clk_L3_I55/in0 (buf_18x)         30         0.01017 & 8.60847 r
clk_L3_I55/y (buf_18x)           30         -0.74201 & 7.86646 r
clk_L3_N55 (net)                 30         0.00000 & 8.59830 r
core/clk_L3_N55 (itagr1)         0.00000 & 8.59830 r
core/clk_L3_N55 (net)           0.00000 & 8.59830 r
core/nb_risc1_i_24_ram0/CLKA (SRAM_DP_256_69) 0.01017 & 8.60847 r
library setup time               -0.74201  7.86646
data required time               7.86646
-----
data required time               7.86646
data arrival time                -7.78522
-----
slack (MET)                      0.08124
  
```



Next Step: Physics of Failure - Based Circuit Modeling

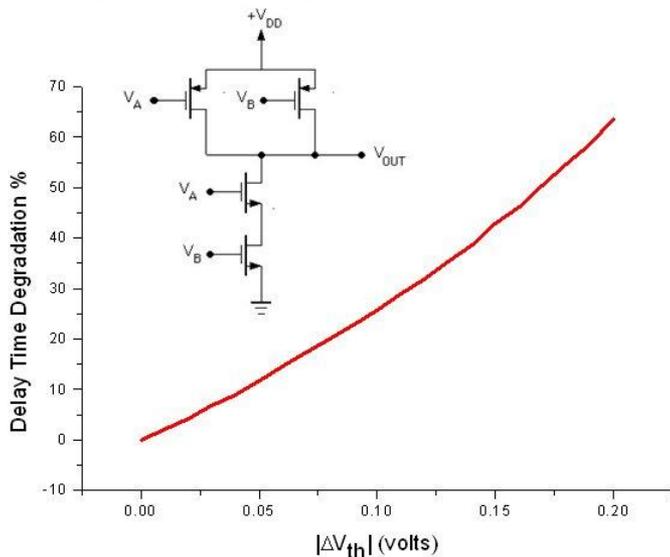


- Done using Xyce™ developed at Sandia National Lab
- Designed for large-scale problems
- Potential access to source code
- Access to local expertise
- Xyce has radiation modeling, which could be obtained in the future.

Future Work

- PoF based development of $V_{th}(t)$
- Experimental dependence on bias, T, duty cycle and frequency must be developed and then extrapolated to years.

Single NAND gate with a 1fF load



Multiple NAND gates

Initial Circuit Testing Done on a Ring Oscillator

- 50% duty cycle is ideal
- Common circuit
- 11 NAND gates using the 65 nm PTM models
- Base frequency of 3.5 GHz
- For $\Delta V_{th} = -0.1$ volts the frequency drops by 15%

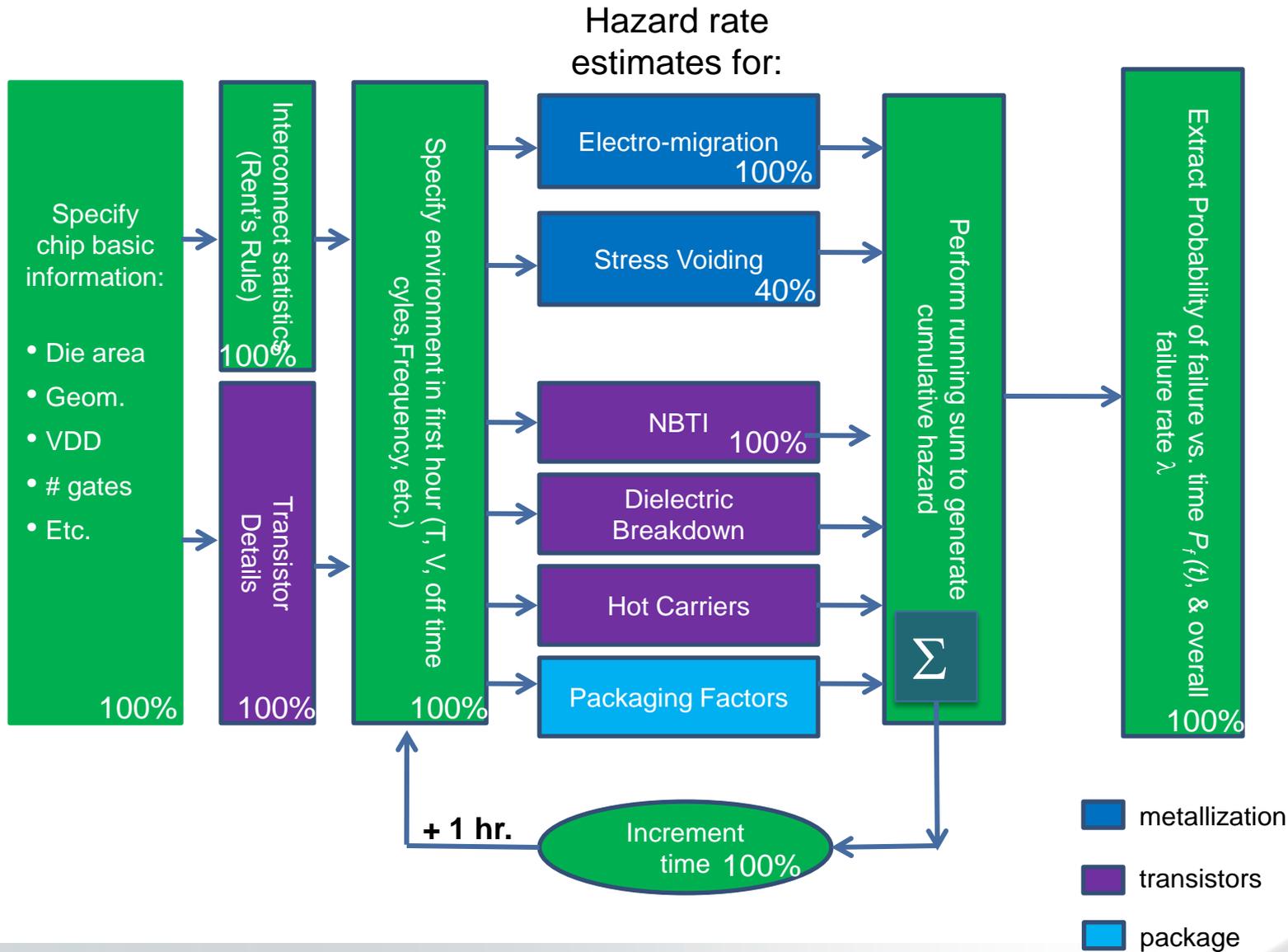
Point of Contact: Kenneth Kambour (505) 853-3157
kenneth.kambour.ctr@Kirtland.af.mil

Presented at MRQW Dec. 2011





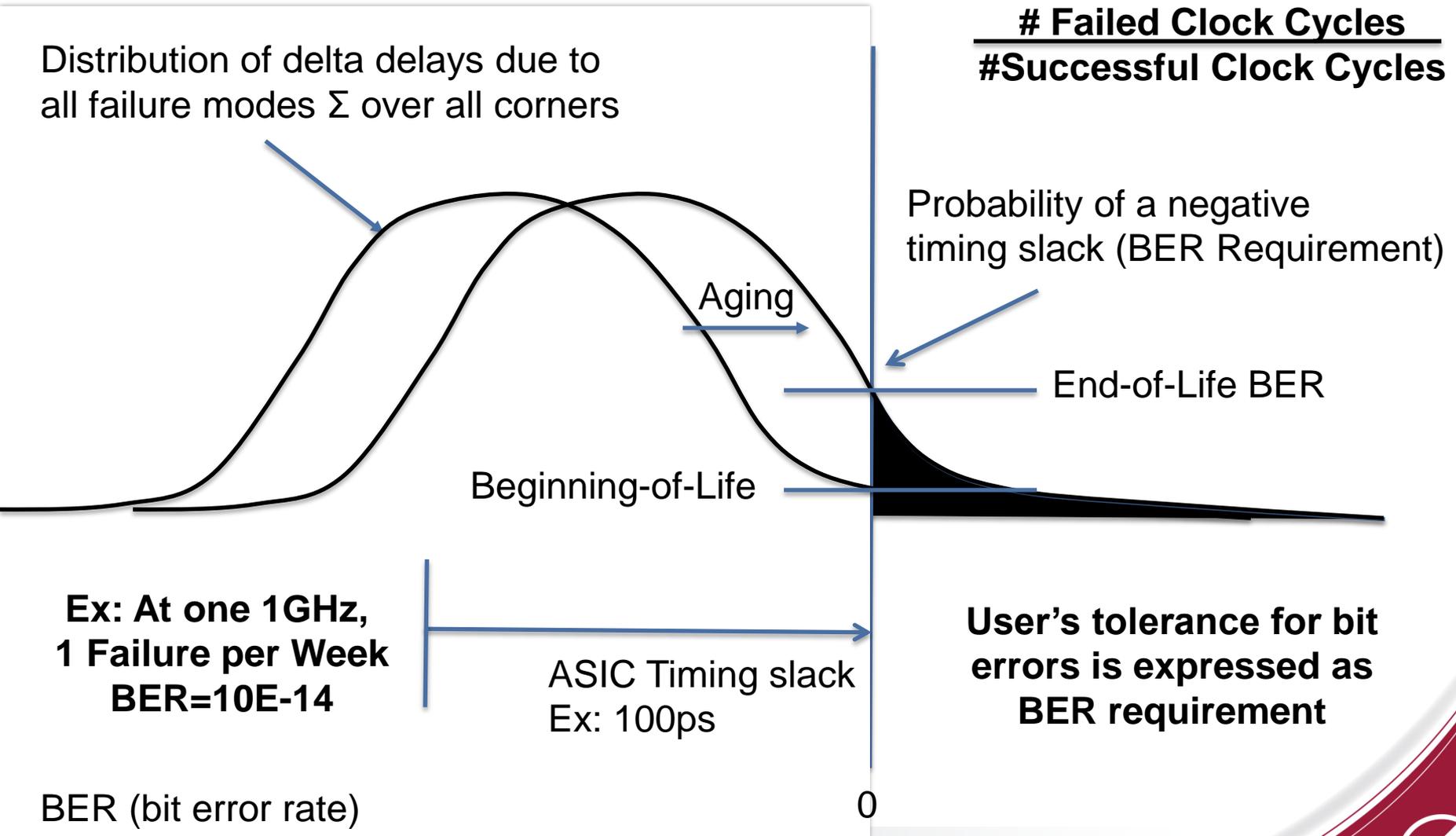
Full Chip 90nm CMOS ASIC Reliability Modeling Tool





Digital ASIC Lifetime Failure Criterion

(i.e. 1 failure per week or per year, ...etc.)



Ex: NBTI User Dashboard Inputs



Microsoft Excel window showing a spreadsheet for 'G134' with various charts and tables related to NBTI (negative bias-temperature instability) analysis.

PMOS Transistor characteristics of minimum design rule size device

VDD	1.4	drain saturation voltage (V) at VGS = VDD
ID0	50	drain current (uA) at VGS=VDS=VDD
VDD	3	nominal Power supply voltage (Volts)
VTp	0.5	threshold voltage (V)
alpha	1.3	velocity saturation index (dimensionless). Must be >= 1
TCVT	0.001	temperature coefficient of threshold voltage shift (1/C)

Min. pmos transistor

transistor IV calculations

	0	1	2	3	4	5	6	7	8	9	10	11	12	13
40 VDS	0	0.075	0.15	0.225	0.3	0.375	0.45	0.525	0.6	0.675	0.75	0.825	0.9	0.975
8 VGS	0	0.075	0.15	0.225	0.3	0.375	0.45	0.525	0.6	0.675	0.75	0.825	0.9	0.975
1	0.375	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0.75	0.53966	1.19331	1.79837	2.39863	2.50534	2.50534	2.50534	2.50534	2.50534	2.50534	2.50534	2.50534	2.50534
3	1.125	0.10874	2.17568	3.26351	4.35135	5.43919	6.52703	7.61487	8.24632	8.24632	8.24632	8.24632	8.24632	8.24632
4	1.5	0.147653	2.35056	4.42953	5.306119	7.36255	8.85316	10.3537	11.822	13.2659	14.7653	15.1932	15.1932	15.1932
5	1.875	0.19161	3.63219	5.44629	7.264387	9.00046	10.8966	12.7127	14.5288	16.3449	18.161	19.9771	21.7932	22.3648
6	2.25	0.212431	4.24661	6.37232	8.497222	10.6215	12.7458	14.8701	16.9944	19.1187	21.2431	23.3674	25.4317	27.616
7	2.625	0.241005	4.82009	7.23014	9.640188	12.0502	14.4603	16.8703	19.2804	21.6904	24.1005	26.5105	28.9206	31.3306
8	3	0.267857	5.35714	8.03571	10.71428	13.3928	16.0714	18.75	21.4286	24.1071	26.7857	29.4628	32.1428	34.8214

Critical timing chain specifications and gate delay parameters

M	7	number of stages in critical chain (integer) 5 ≤ M ≤ 15
ts	100	timing slack (ps)
N	10	number of equivalent critical timing chains (integer)
L	0.5	total interconnect length (mm)
a	1.1	cascode factor (dimensionless) must be > 1
f	2.5	average stage effort (units of minimum inverter effort)
npar	1.5	average parasitic effort (units of minimum inverter parasitic)
tau	10	basic minimum inverter delay (ps)
Co	3	input capacitance of min. inverter (fF)
Ro	3.33	output resistance of min. inverter (kΩ)
pinv	1	parasitic cap. of a min. inverter (units of min. inverter input cap.)
c	200	interconnect capacitance per unit length (fF/mm)
r	80	interconnect resistance per unit length (ohm/mm)
rd2	8	interconnect time constant per square of unit length (ps/mm ²)
l	52.7	first segment length (um)
af	2.8	a x f convenient factor (dimensionless)
af	0.4	a / f another convenient factor (dimensionless)
D	324.8	Total chain delay (ps)
D+ts	424.8	total chain delay plus timing slack (ps)

Critical Timing Chain Delay

Calculation of the components of the stage delays in the critical timing path

Term	segment length (um)	segment length (mm)	logical effort delay (ps)	interconnect delay (ps)	combination delay (ps)	sum (ps)	cumulative sum (ps)	events (ps)	odds (ps)	cumulative events (ps)	cumulative odds (ps)	multiplier for DVT (ps^1/2)
segment length (um)	52.7	58.0	63.8	70.1	77.2	84.3	33.4	0.0	0.0	0.0	0.0	0.0
segment length (mm)	5.27E-02	5.80E-02	6.38E-02	7.01E-02	7.72E-02	8.43E-02	3.34E-02	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
logical effort delay (ps)	40	40	40	40	40	40	40	0	0	0	0	0
interconnect delay (ps)	2.22E-02	2.63E-02	3.25E-02	3.94E-02	4.75E-02	5.76E-02	6.97E-02	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
combination delay (ps)	1.41E+01	6.18E+00	2.72E+00	1.20E+00	5.27E-01	2.32E-01	1.02E-01	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
sum (ps)	54.1553	46.4281	43.3525	42.8806	45.0356	52.7228	40.1717	0	0	0	0	0
cumulative sum (ps)	54.1553	100.583	143.9347	186.815	231.311	284.634	324.805	0	0	0	0	0
events (ps)	0	46.4281	0	42.8806	0	45.0356	0	40.1717	0	0	0	0
odds (ps)	54.1553	0	43.3525	0	45.0356	0	40.1717	0	0	0	0	0
cumulative events (ps)	0	46.4281	46.42808	89.3087	83.3087	142.031	142.031	142.031	142.031	142.031	142.031	142.031
cumulative odds (ps)	54.1553	54.1553	97.50659	97.5066	142.602	142.602	182.774	182.774	182.774	182.774	182.774	182.774
multiplier for DVT (ps^1/2)	5.41E+00	6.81E+00	6.57E+00	6.53E+00	6.71E+00	7.27E+00	6.42E+00	6.31E+00	6.31E+00	6.31E+00	6.31E+00	6.31E+00

NBTI pmos transistor threshold shift model parameters

ΔV0	32.00	threshold voltage shift scale factor at ref. stress voltage & temp. (Volts)
γ	0.24	time power coefficient for threshold shift (dimensionless)
t0	1000.00	time scale factor (sec)
V0	3.50	pmos stress voltage exponential coefficient (Volts)
Ea	0.20	activation energy for development of threshold voltage shift (eV)
K	0.85	fraction of threshold shift that is annealable (dimensionless)
B0	8	recovery scaling coefficient at ref. temp. (dimensionless)
Eb	0.08	activation energy for annealing of threshold voltage shift (eV)
β	0.3	recovery time dispersion parameter (dimensionless)
Ds	5	min. stress duty factor within logic gate(s) (percent)
Db	35	max. stress duty factor within logic gate(s) (percent)
N	100	no. of pts. to sweep duty factor

NBTI pmos transistor threshold shift

Process variables related to NBTI

Vmin	800.00	minimum gate width (nm)
Lmin	150.00	minimum gate length (nm)
tox	50	nominal gate oxide thickness (nm)
KRCF	0.50	constant for random charge fluctuation
KRDF	0.10	constant for random charge fluctuation
σV	0.20	standard deviation of VDD fluctuation
FThru	1.68E+02	fail criterion is average duration between bit errors (hours)
fop	1	frequency of operation (GHz)

NBTI duty factor dependence

For the following four plots:

Tplot	150.00	temperature for plot display of NBTI model (°C)
Vplot	4.10	stress voltage for plot display of NBTI model (V)
tplot	1000	stress time for plot display of NBTI model (sec)
y0	0.42778	threshold voltage shift multiplicative constant dependent on stress voltage and temperature

No. of pts for plot

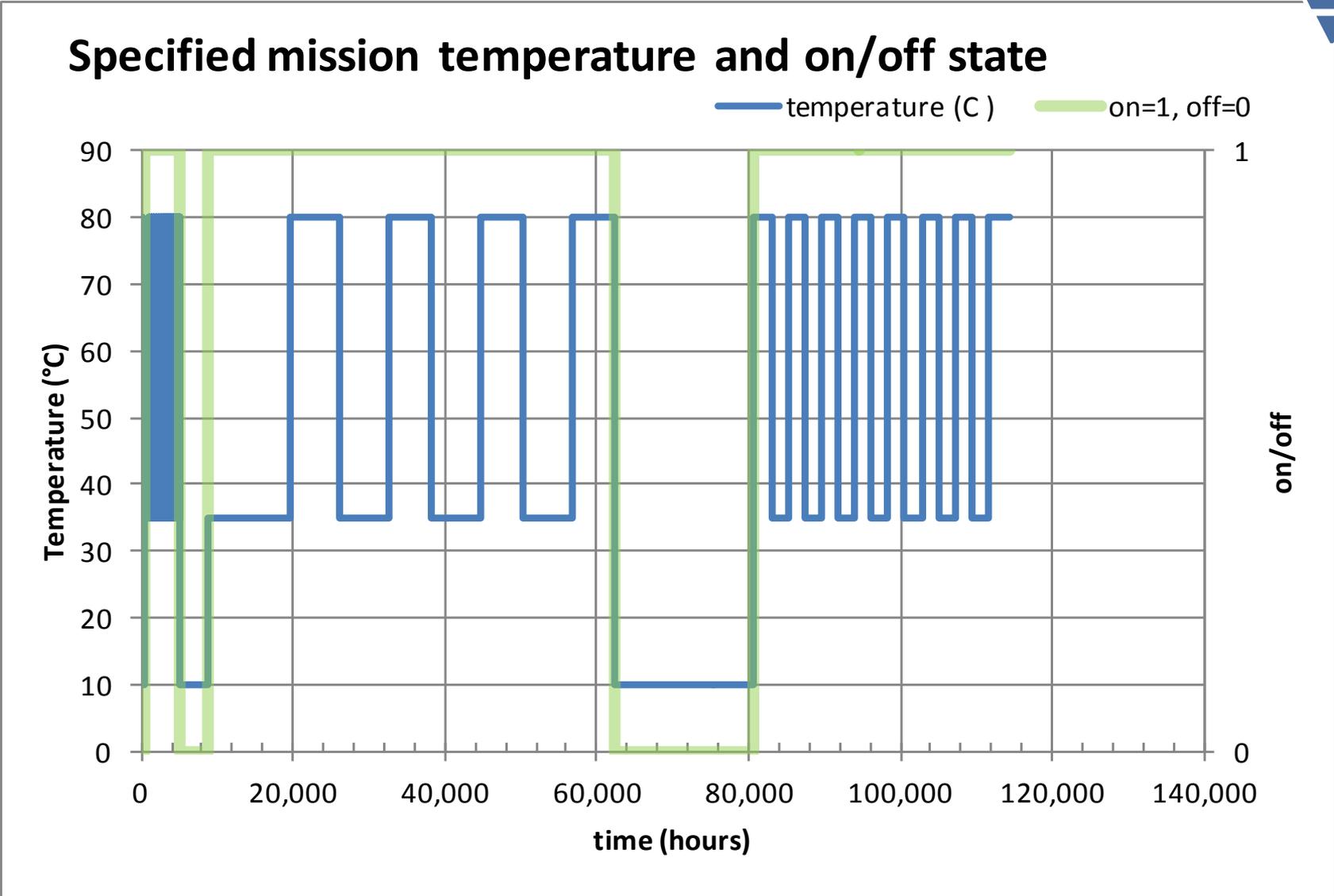
delta t (s)	10	20	30	40	50	60	70	80	90	100	110	120	130
Total	8.15E-02	1.42E-01	1.67E-01	1.84E-01	1.98E-01	2.08E-01	2.18E-01	2.26E-01	2.33E-01	2.40E-01	2.46E-01	2.52E-01	2.57E-01
Permanent	1.22E-02	2.12E-02	2.51E-02	2.77E-02	2.96E-02	3.13E-02	3.27E-02	3.39E-02	3.50E-02	3.60E-02	3.69E-02	3.78E-02	3.86E-02
Recoverable	6.93E-02	1.20E-01	1.42E-01	1.57E-01	1.68E-01	1.77E-01	1.85E-01	1.92E-01	1.98E-01	2.04E-01	2.09E-01	2.14E-01	2.19E-01

As percentages of final ΔVT under DC stress (equivalent to 100% duty cycle):

Permanent	5.45E-01	3.45E-01	1.64E+00	0.97E+00	0.73E+00	0.63E+00	0.57E+00	0.52E+00	0.48E+00	0.45E+00	0.43E+00	0.41E+00	0.40E+00
Recoverable	0.00E+00												
Total	0.00E+00												



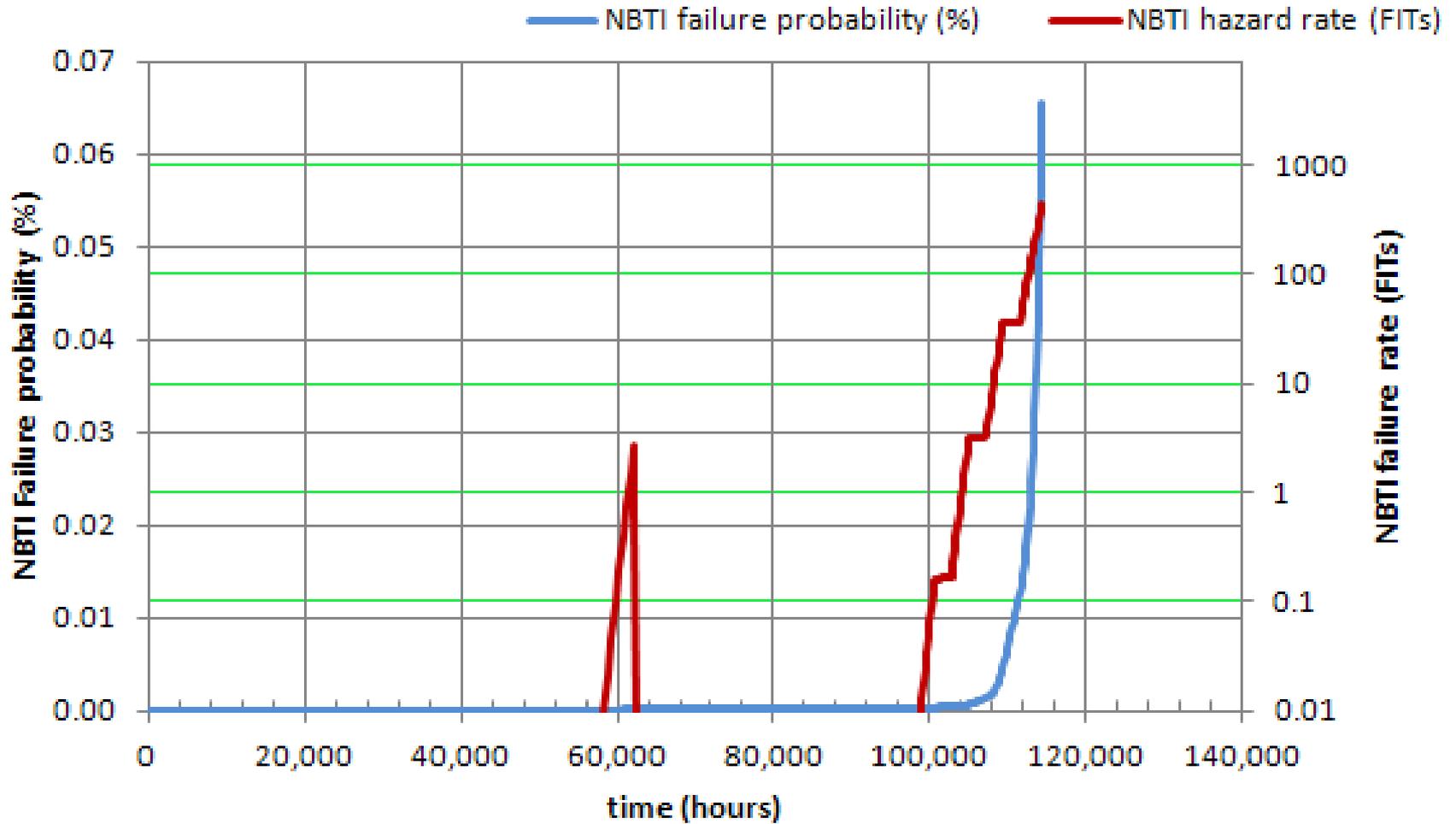
Ex: Mission Use Condition





Ex: Time evolved FIT rate calculation

NBTI failure probability and failure rate



CMOS ASIC PoF Lifetime Modeling – Looking Forward

- Develop PoF MD/DFT models of each of the major CMOS Failure Modes (Atomistic-Level)
 - *Provides better understanding of PoF and basic mechanisms*
 - *Coupled with nano-scale DPA, may enable **in silico** reliability prediction*
- Develop automated process to extract RelExpert compatible aged MOS models for any process node (Device-Level)
 - *BSIM Pro+ AgeMOS does not do SOI and Foundry Models are proprietary*
 - *Enables process specific End-of-Life Analog Mixed Simulation of circuits*
- Develop process to include BEOL wear-out mechanisms into circuit-level reliability simulator (Circuit-Level)
- Develop automated process to extract time evolved digital cell library timing degradation models (Circuit-Level)
- Complete Full-Chip 90nm CMOS ASIC Simulator (ASIC-Level)
- Develop advanced packaging time evolved failure rate models (ASIC-Level)



Summary

- HiREV nanoCMOS PoF Modeling Progress is Steady
 - *Primarily addressing device/circuit/ASIC lifetime reliability*
 - *Expanding into basic mechanisms and packaging*
- Multiple Technology Nodes Under Investigation
 - *Program Pull at 130/90/45nm*
 - *IR&D Interest at 32nm*
- Many opportunities for NEPP and HiREV to collaborate on PoF reliability data collection and model development at device/circuit/ASIC as well as package/board/unit levels of integration

Need more info?

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and

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