NEPP Electronic Technology Workshop
June 11-13, 2012

National Aeronautics
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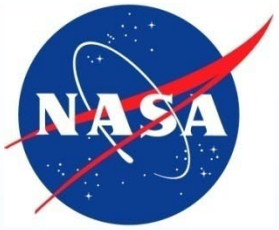

A Newly Developed Approach to Total Ionizing Dose (TID) Testing for Field Programmable Gate Array (FPGA) Devices

Melanie Berg, MEI Technologies/NASA GSFC

E. Wilcox, M. Friendlich, J. Lakeman, H. Kim: MEI Technologies/NASA GSFC

K. LaBel, J. Pellish: NASA GSFC

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NASA Goddard Radiation Effects and Analysis Group (REAG) FPGA TID Testing Supporters and Collaborators

- **Supporters:**
  - **Defense Threat Reduction Agency (DTRA)**
  - **NASA Electronics Parts and Packaging (NEPP)**
- **Collaborators:**
  - **Microsemi**

Major Accomplishments

- **Developed new TID testing technique**
- **Performed two phases of TID technique validation in December 2011 and March of 2012. Testing utilized the Microsemi ProASIC3 FPGA as the device under test (DUT)**
- **NSREC 2012 paper accepted as oral presentation: "A Robust Strategy for Total Ionizing Dose Testing of Field Programmable Gate Arrays", E. Wilcox, M. Berg, M. Friendlich, J. Lakeman, H. Kim, J. Pellish and K. LaBel**

> ***We present a novel method of FPGA TID testing that measures propagation delay between flip-flops operating at maximum speed. Measurement is performed on-chip at-speed and provides a key design metric when building system-critical synchronous designs.***

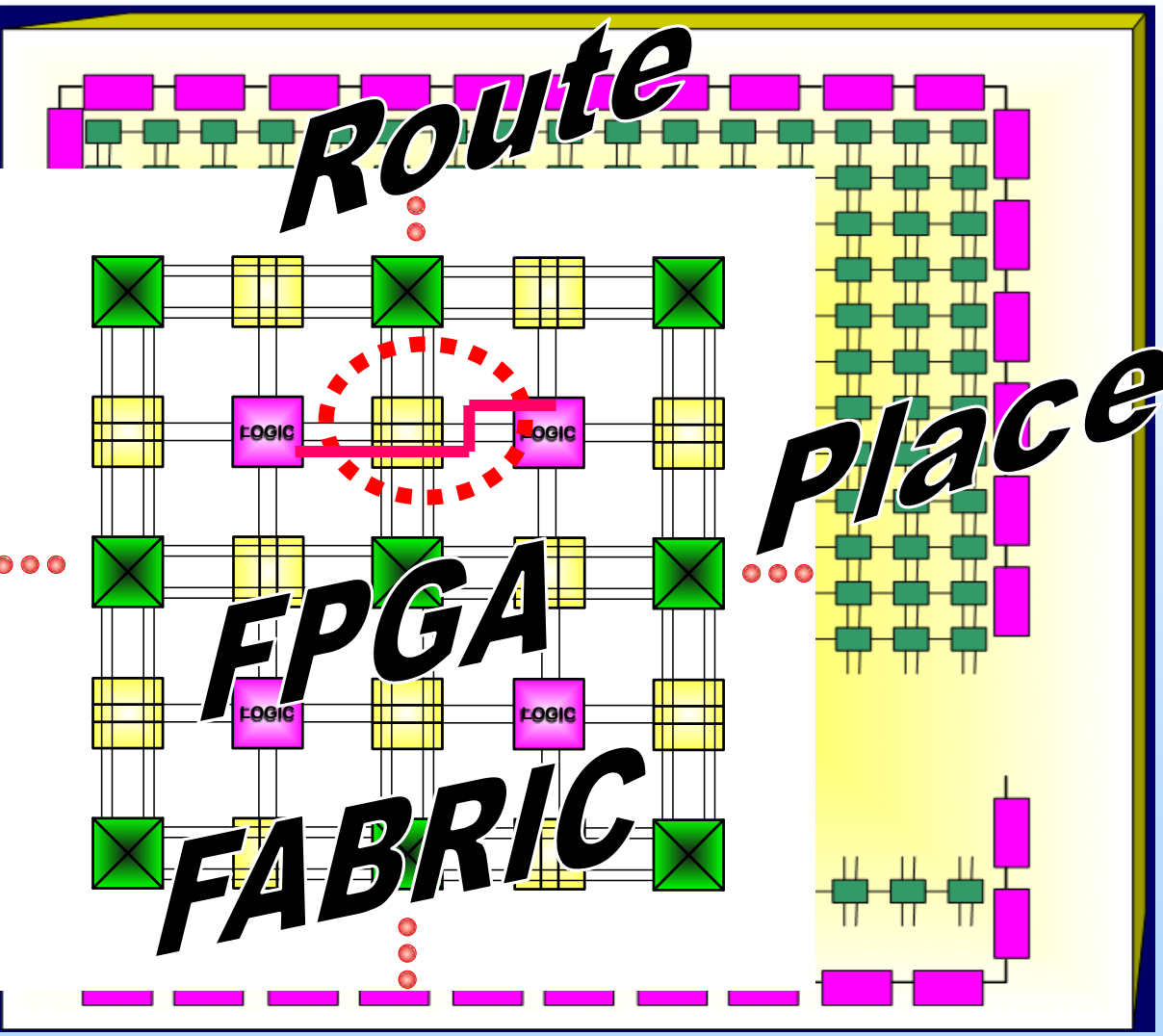
Impact to Community

- **The new method of TID FPGA testing focuses on functional data path delay degradation**
- **Enhancements of new method versus the conventional method:**
  - **Internal data path delay measurements are able to be performed without the inclusion of input and output technology within the measurement path.**
  - **No averaging**
  - **Finer resolution timing degradation data per dose**
  - **In terms with designer data path delay measurements**

Background:
Validation of the new TID testing technique using the Microsemi ProASIC3 FPGA

Overview of Design Development and FPGA Element Utilization

Hardware design language (HDL)



HDL

MAP

INTO FPGA LIBRARY

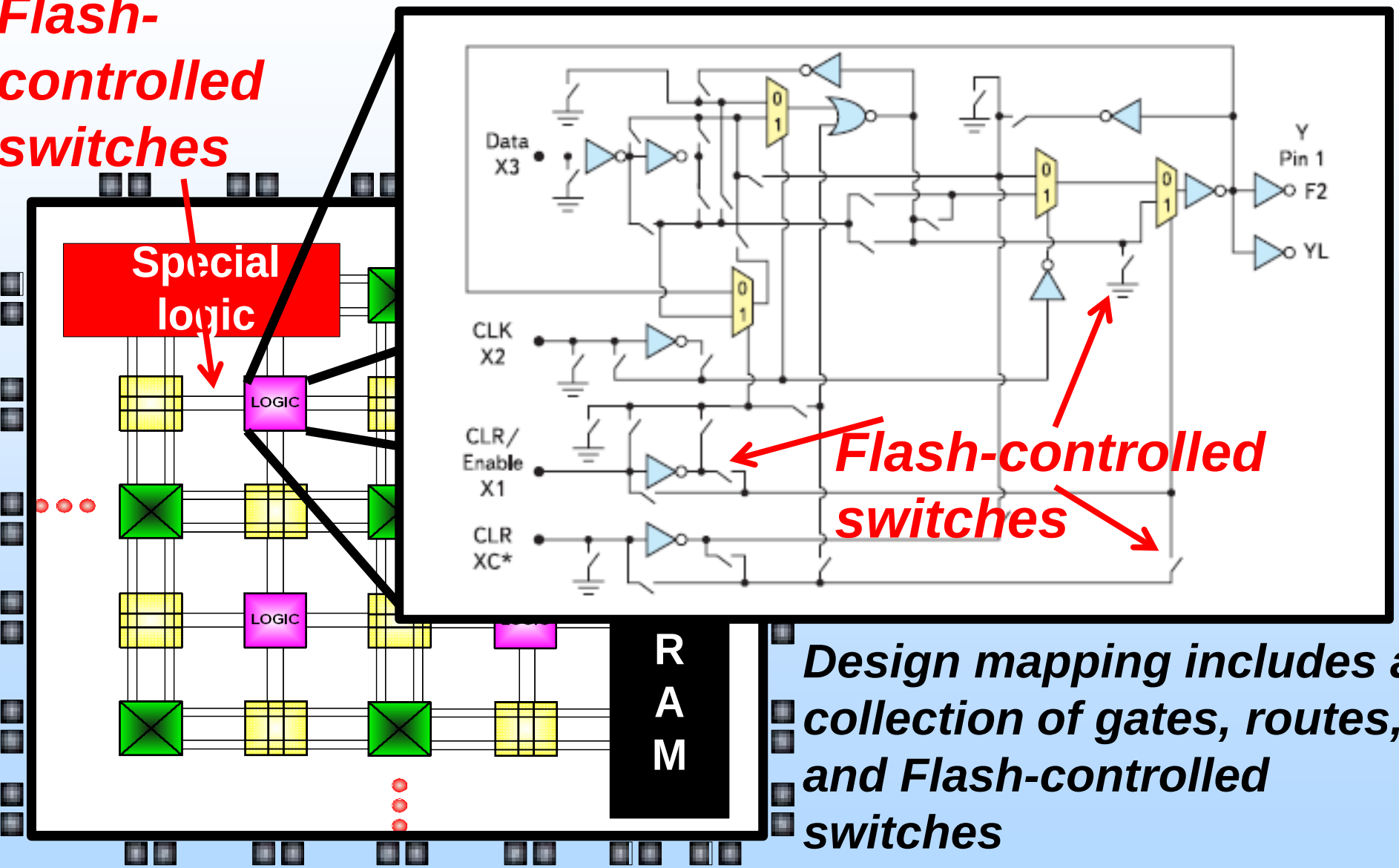
Combinatorial FPGA Block

MUX

DFF FPGA Block

D SET Q CLR Q

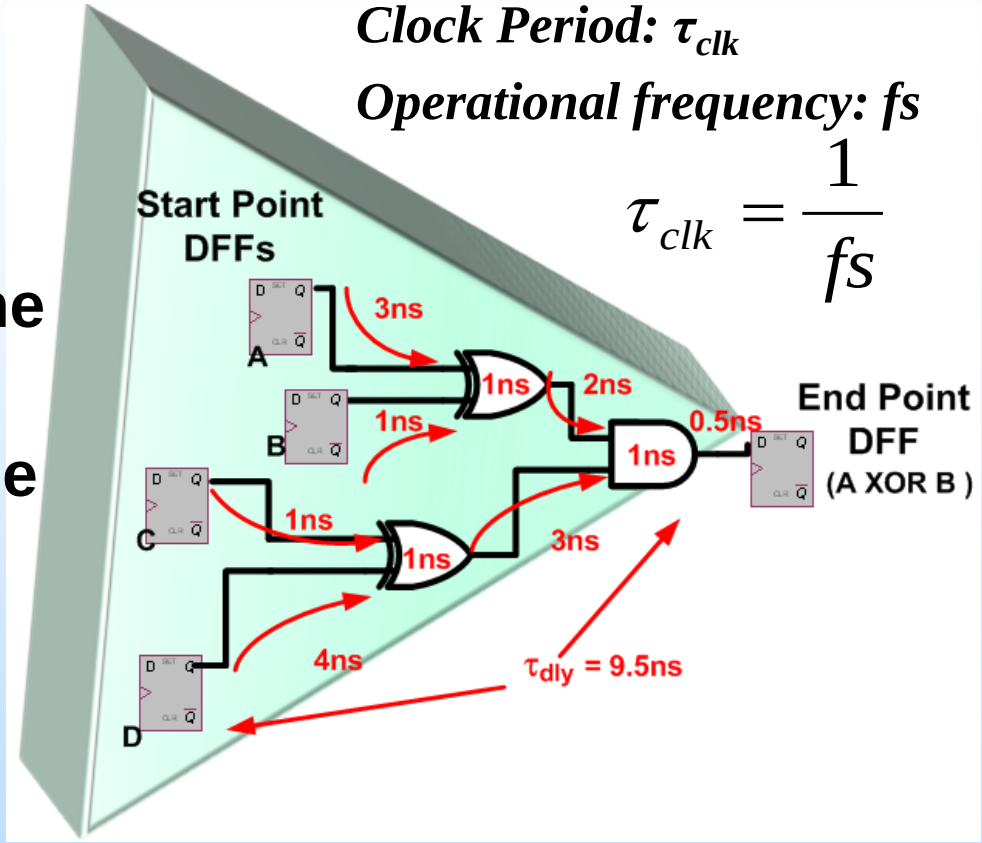
A Closer Look at an FPGA Logic Cell: Microsemi ProASIC3

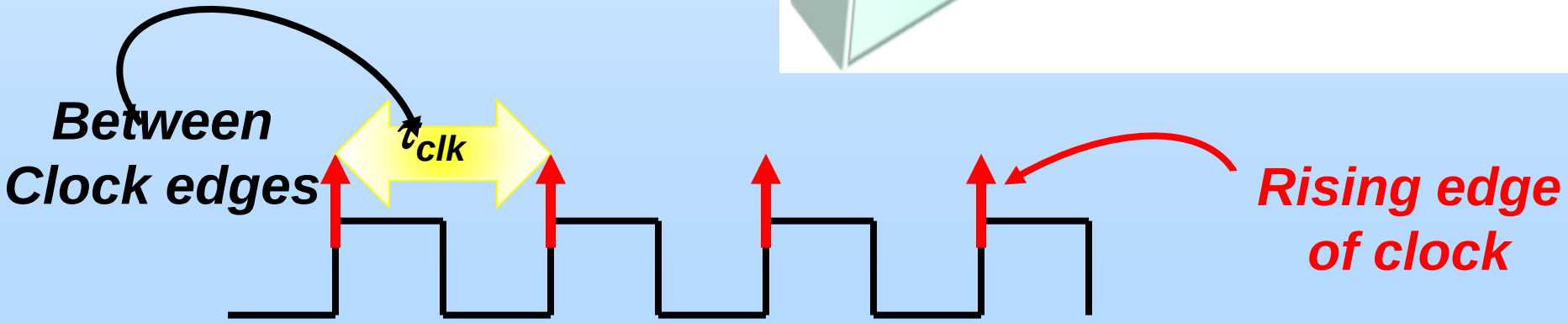


Design mapping includes a collection of gates, routes, and Flash-controlled switches

Terminology and Definitions for Synchronous Designs

- **Combinatorial Logic (CL): Compute between clock edges**
- **DFFs: Hold (or sample) at the rising edge of a clock**
- **Each StartPoint has a unique delay path (τ_{dly}) to reach an EndPoint**



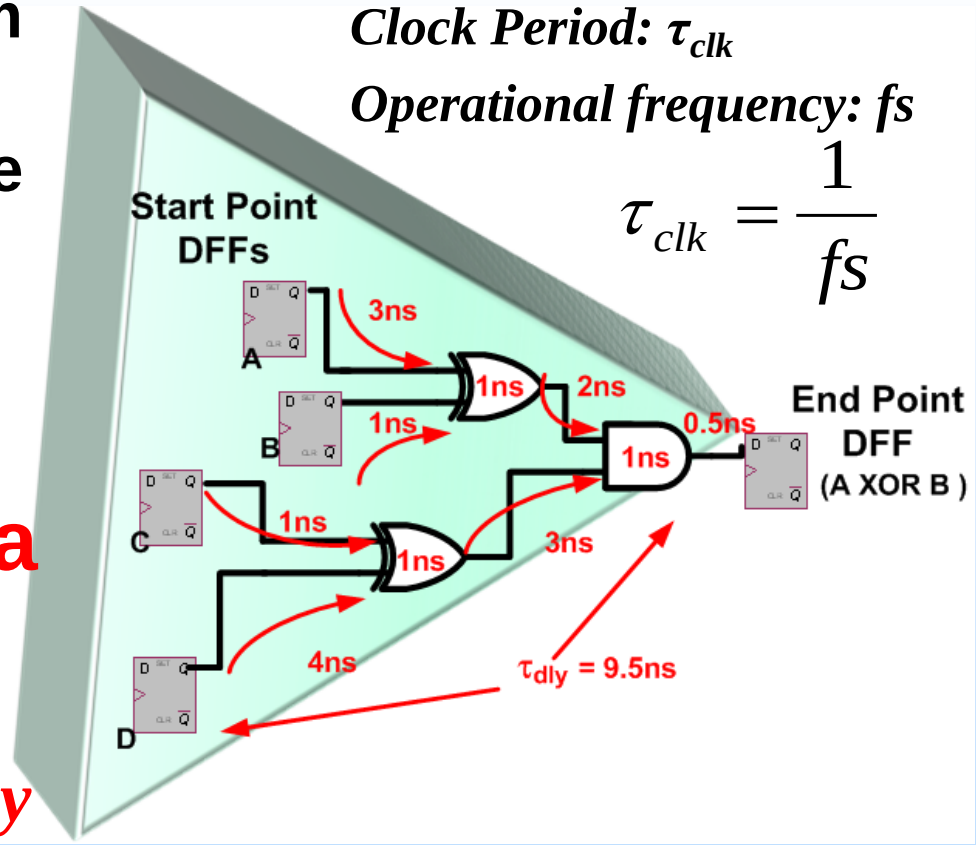


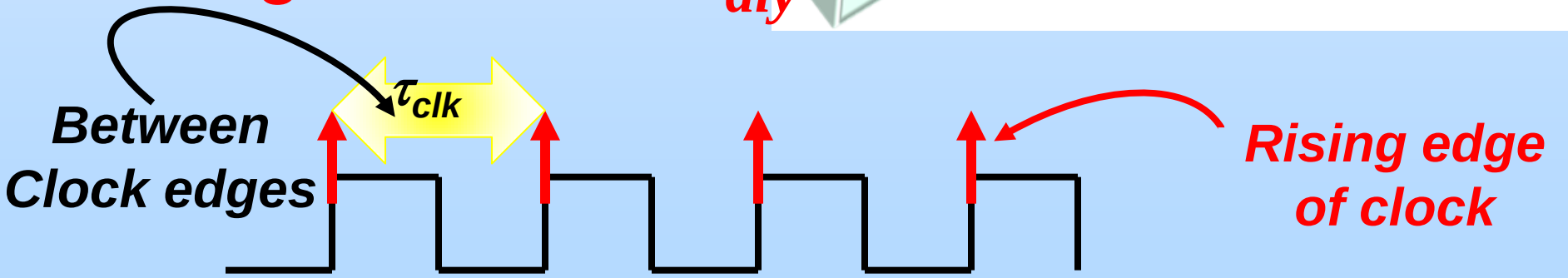
The Effects of Data Path Delay to Synchronous Operation

- If the time it takes to get from a StartPoint to an EndPoint exceeds the clock period, the circuit will not work

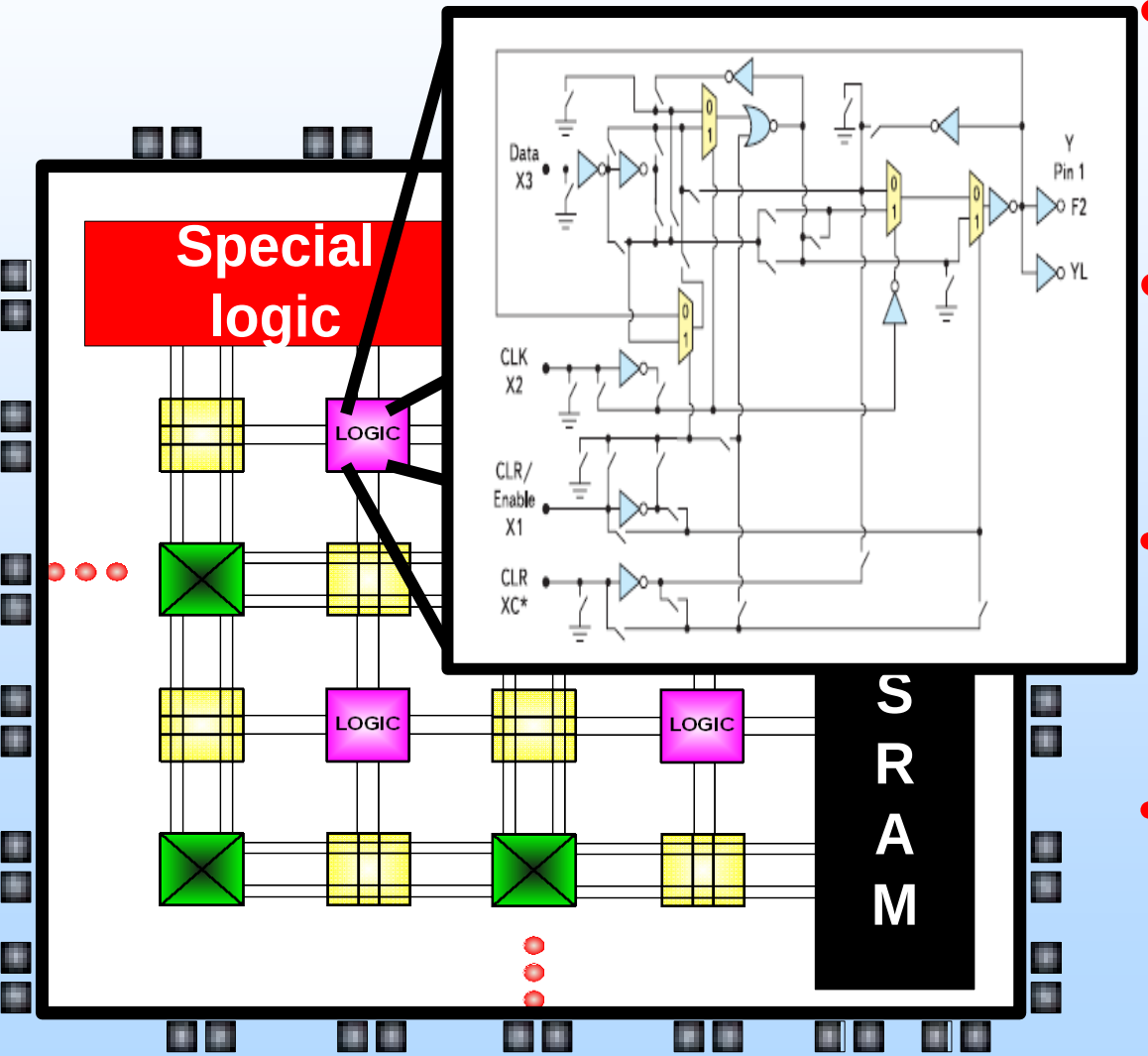
$$\tau_{dly} < \tau_{clk}$$

- We have established a method to measure the degradation of τ_{dly}





Microsemi ProASIC3 TID Effects and τ_{dly}

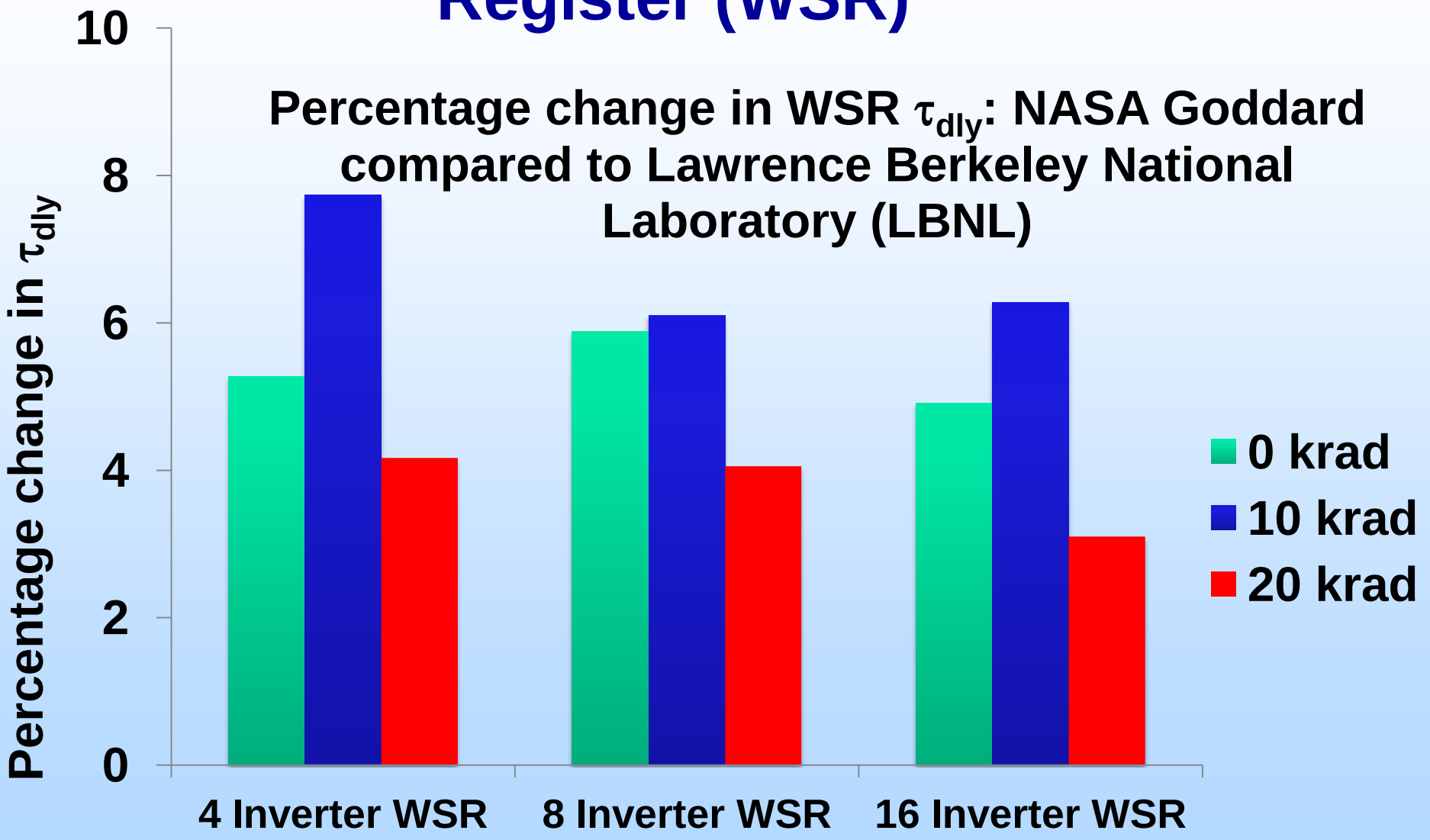


- τ_{dly} *is affected by the number gates a data path traverses*
- τ_{dly} *is affected by temperature, voltage and other noise*
- *Degradation in a gate's performance will affect* τ_{dly}
- *Degradation in a flash cell can also affect* τ_{dly}

Considerations: TID Effects and Design Operation

- **Designers are required to have a 10% timing margin in their design. This accommodates for:**
  - **Degradation in process**
  - **Voltage fluctuation**
  - **Temperature fluctuation**
  - **TID effects**
- **TID should not account for the full 10% margin.**

Change in Timing due to Ground-Level Environment with Windowed Shift Register (WSR)

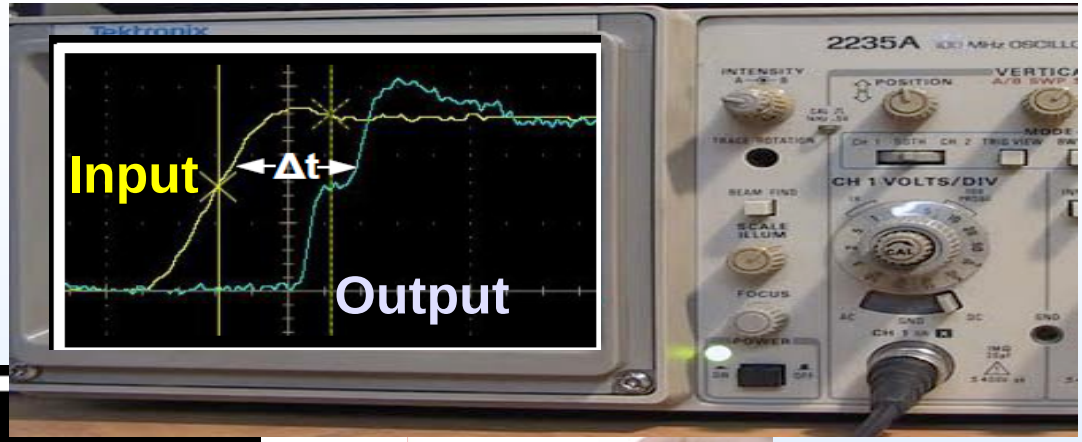


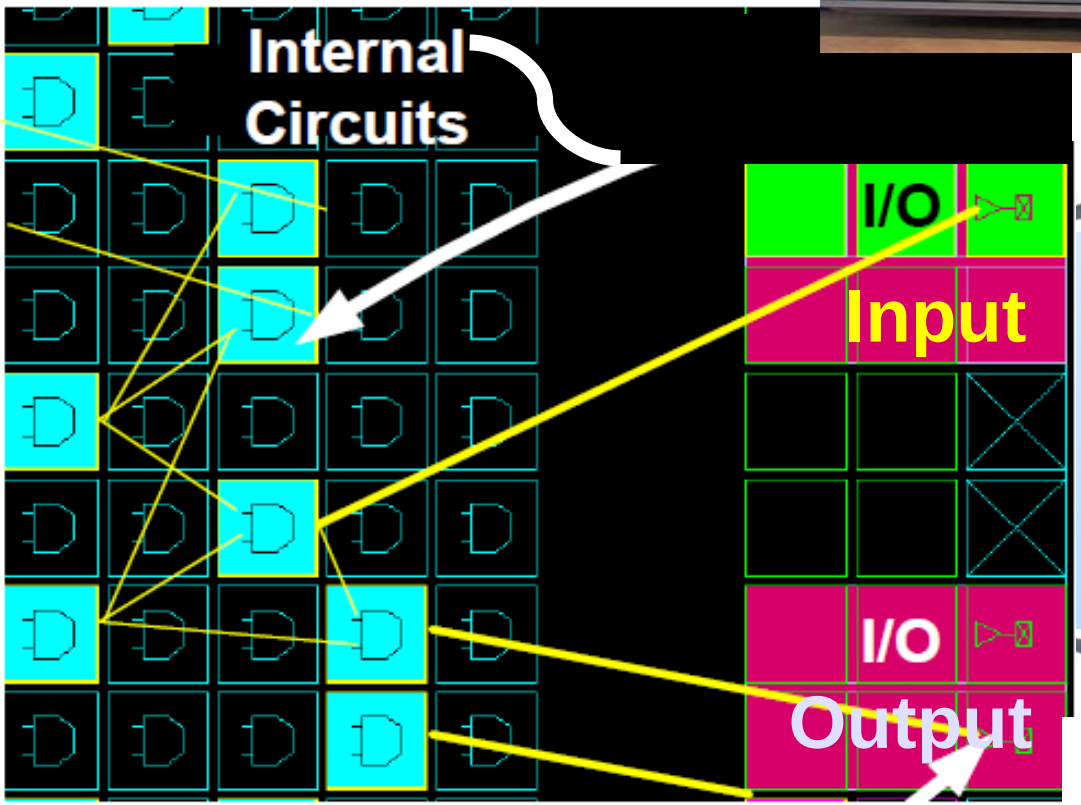
Motivation

- **Our focus is to evaluate the trend of data path degradation based on ionizing dose.**
  - **Does design complexity impact degradation**
  - **Degradation can be in the pico-second to nano-second range… how do we measure with this type of resolution?**
  - **How do we determine worst case?**

Conventional TID Testing Method

Measurement of delay from input to output (Δt) is taken using an Oscilloscope





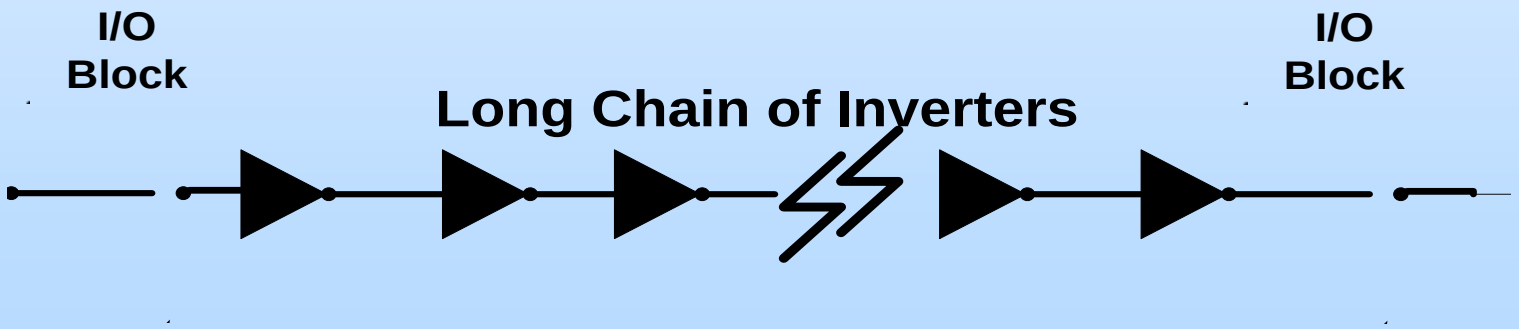
Internal technology is not the same as I/O technology: Mixed technology in the measurement path

Issues with Conventional Testing Methodology

- **Delay Path Measurements:**
  - **Delay measurements are crude: performed by determining the delay of signal input to signal output.**
  - **Mix of I/O circuits and internal circuits within the measurement path**
  - **Test noise can significantly degrade measurement quality**

Conventional Test Structures: Long String of Inverters

- Need long string of elements due to the test method and resolution test apparatus.
- Averaging of delay degradation (long string)
- Cannot include flip-flops or clocks
- Unable to characterize design complexity effects

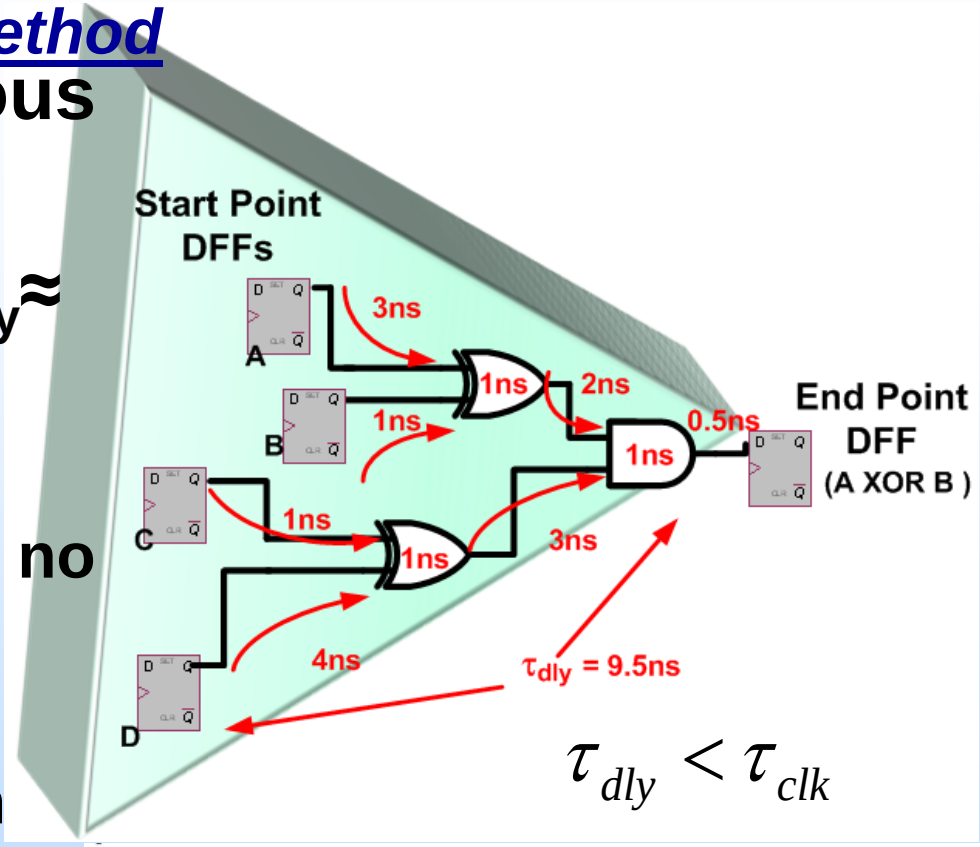


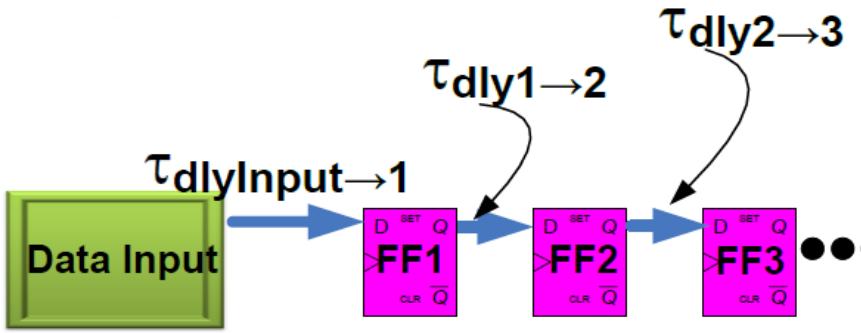
New TID Test Methodology

Technical Highlights

TID Test Methodology Development – Logistics of New Test Method

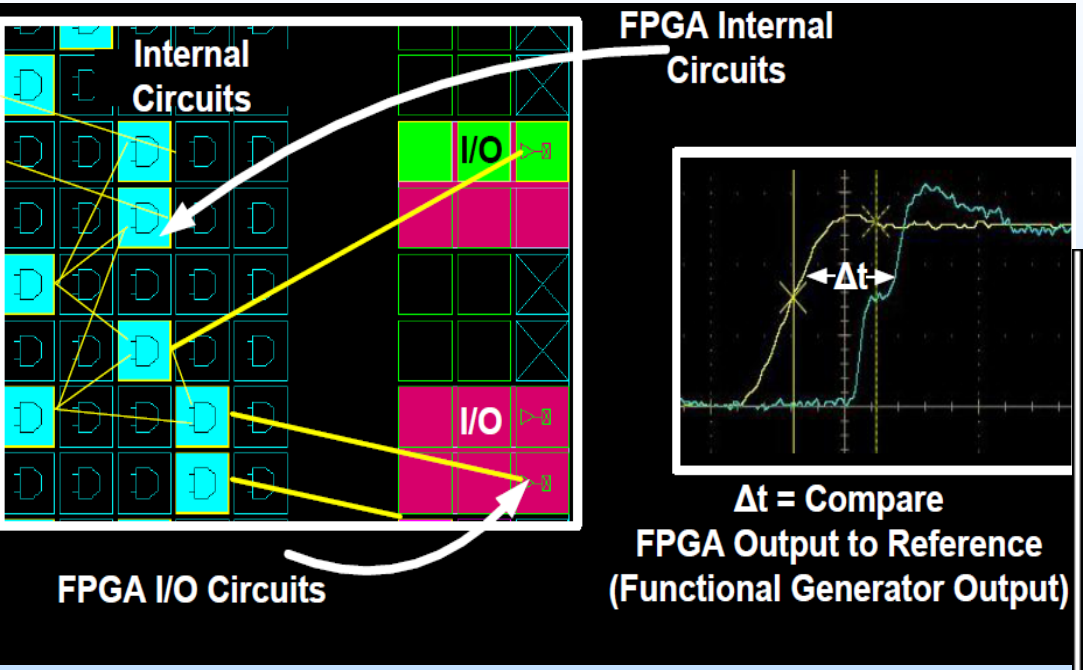
- $\tau_{dly} < \tau_{clk}$ for a synchronous design to work
- We find τ_{dly} such that $\tau_{dly} \approx \tau_{clk}$.
  - Find closest frequency where circuit fails versus no failures
  - Shift registers: τ_{dly} is manually controlled such that all are equal throughout a string
- Hence degradation in τ_{clk} reflects degradation in τ_{dly}

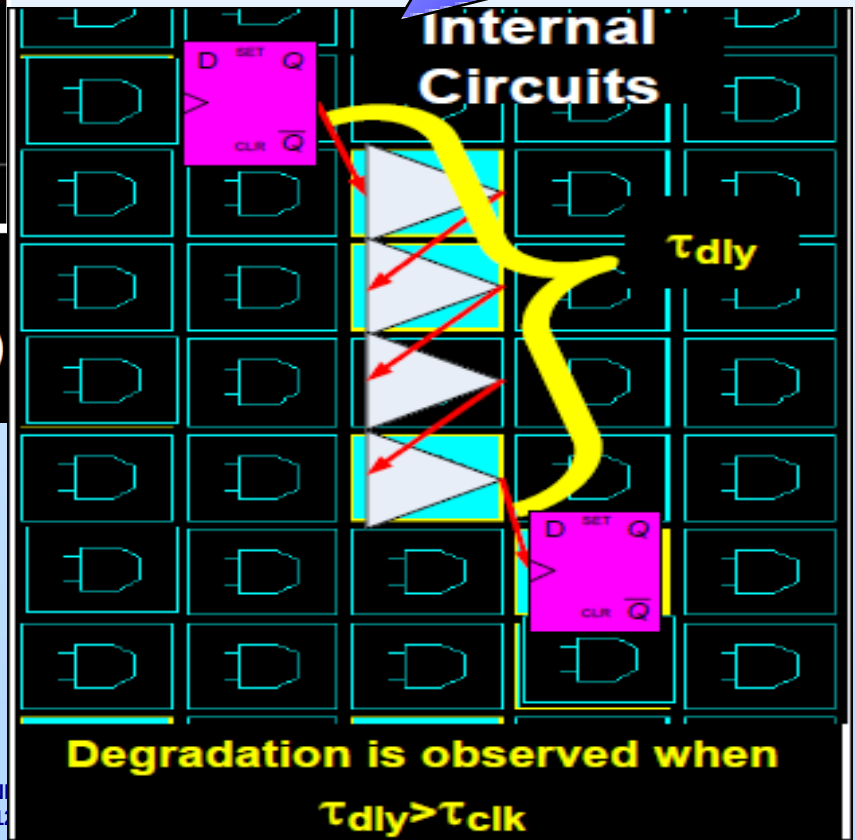




Schematic Comparison of Methods

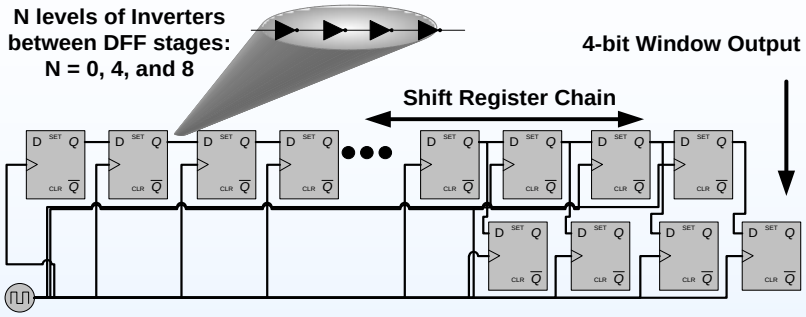
Delay measured from input to output with granularity in the range of 100's of nanoseconds





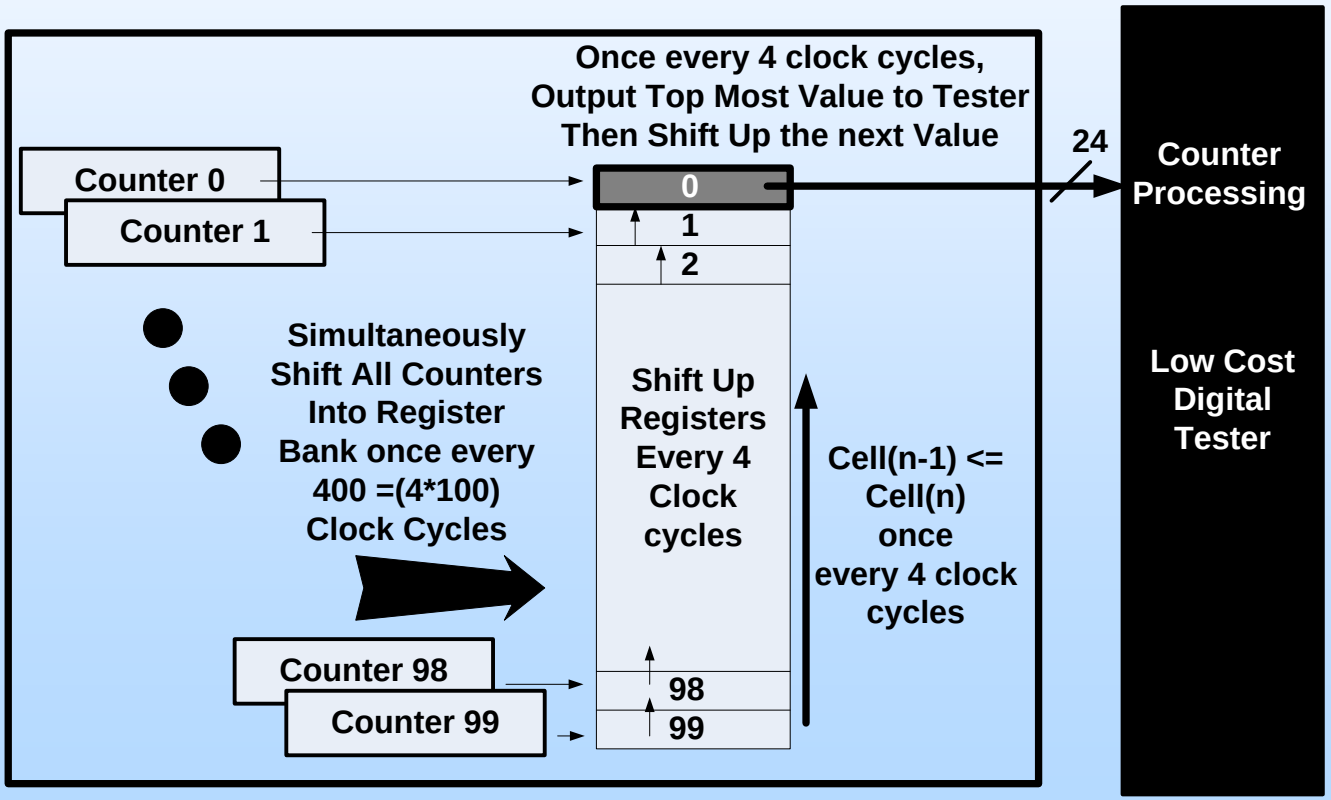
Delay measured internally: degradation will cause $\tau_{dly} > \tau_{clk}$ and will cause circuit to be inoperable

TID Test Structures



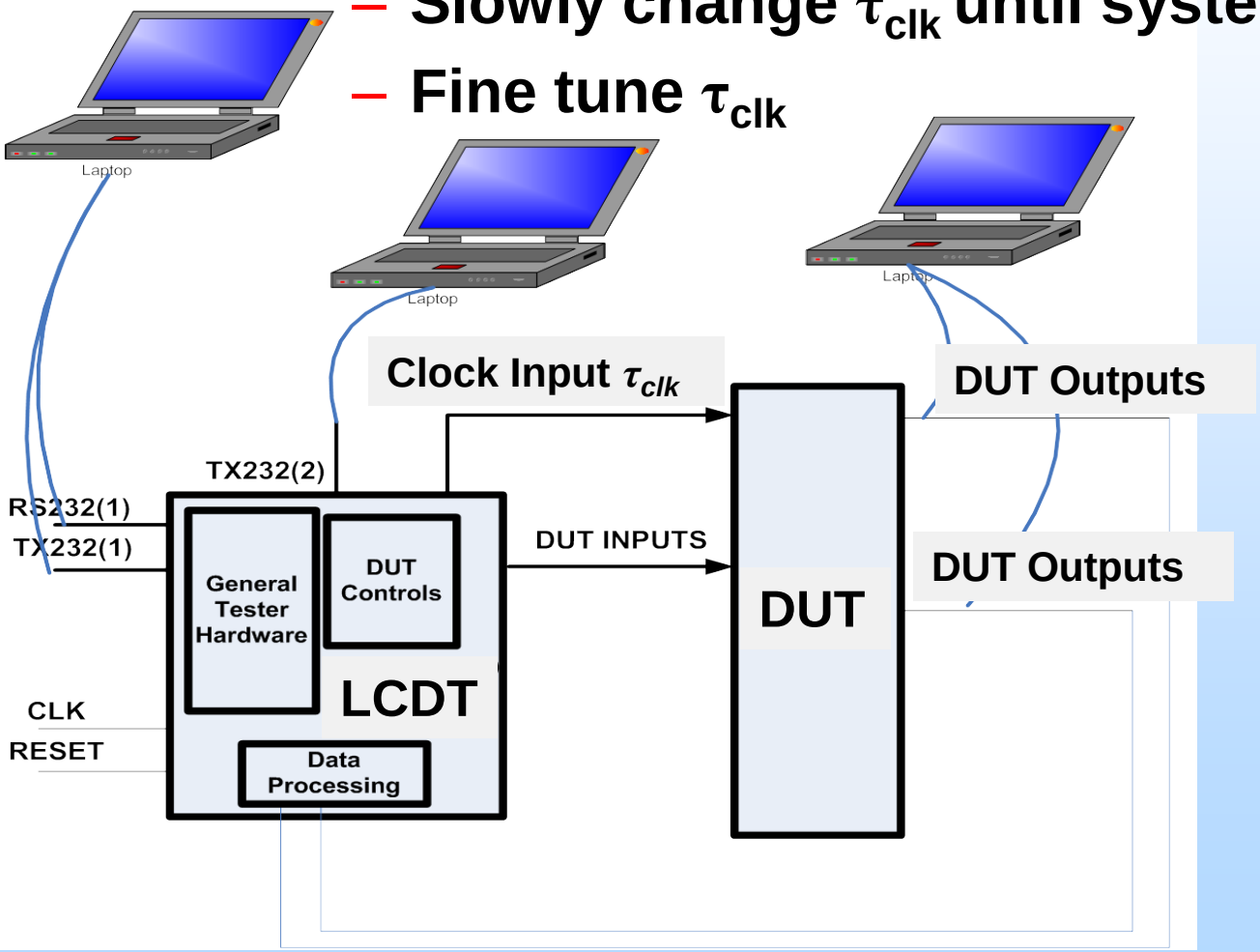
Windowed Shift Registers: (WSRs)

Counter Arrays



Finding τ_{dly} by Changing τ_{clk}

- We control τ_{clk} within the FPGA tester
  - Start with $\tau_{clk} < \tau_{dly}$ (system fails)
  - Slowly change τ_{clk} until system is functional
  - Fine tune τ_{clk}

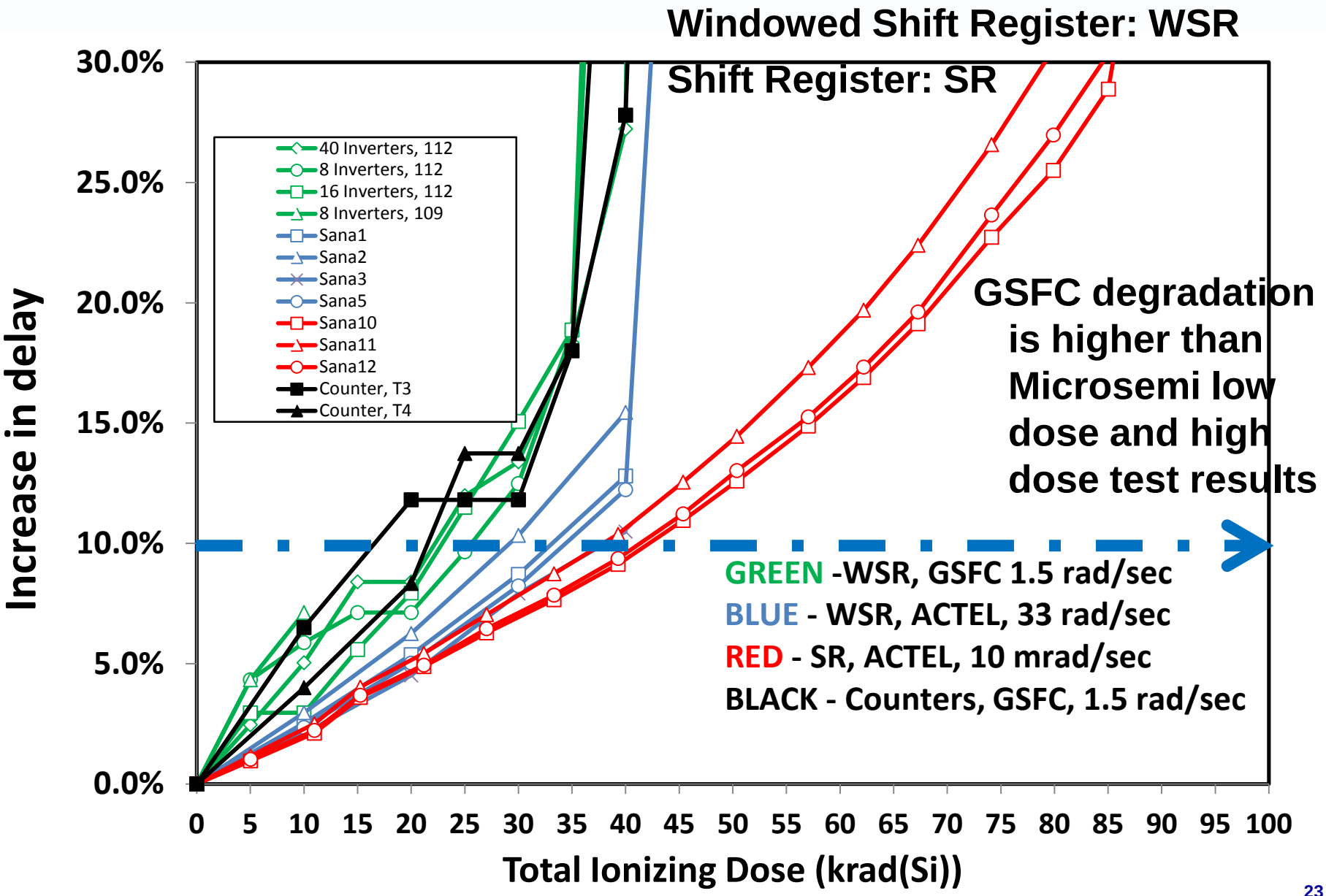


Comparison of TID Test Methods Regarding Presented Data

	Proposed Methodology	Conventional Methodology
Test Architectures	• Shift Register • Counter Arrays	Inverter Strings (no clocks, no DFFs)
Measurement	Internal: worst case path delay from DFF to DFF	External: average path delay through input, inverters, and output
Data Dose Rates	1.5 rad/s	Low: 10mRad/s High: 33Rad/s
Source	Co-60	Co-60

Technical Highlights

GSFC Versus Microsemi ProASIC3 TID Test Results-1



Notes Regarding Observed Timing Degradation

- Timing degradation observed with no changes in device current
- Remember: Device fails when it can no longer operate as expected.

If $\tau_{dly} > \tau_{clk}$ we have failure

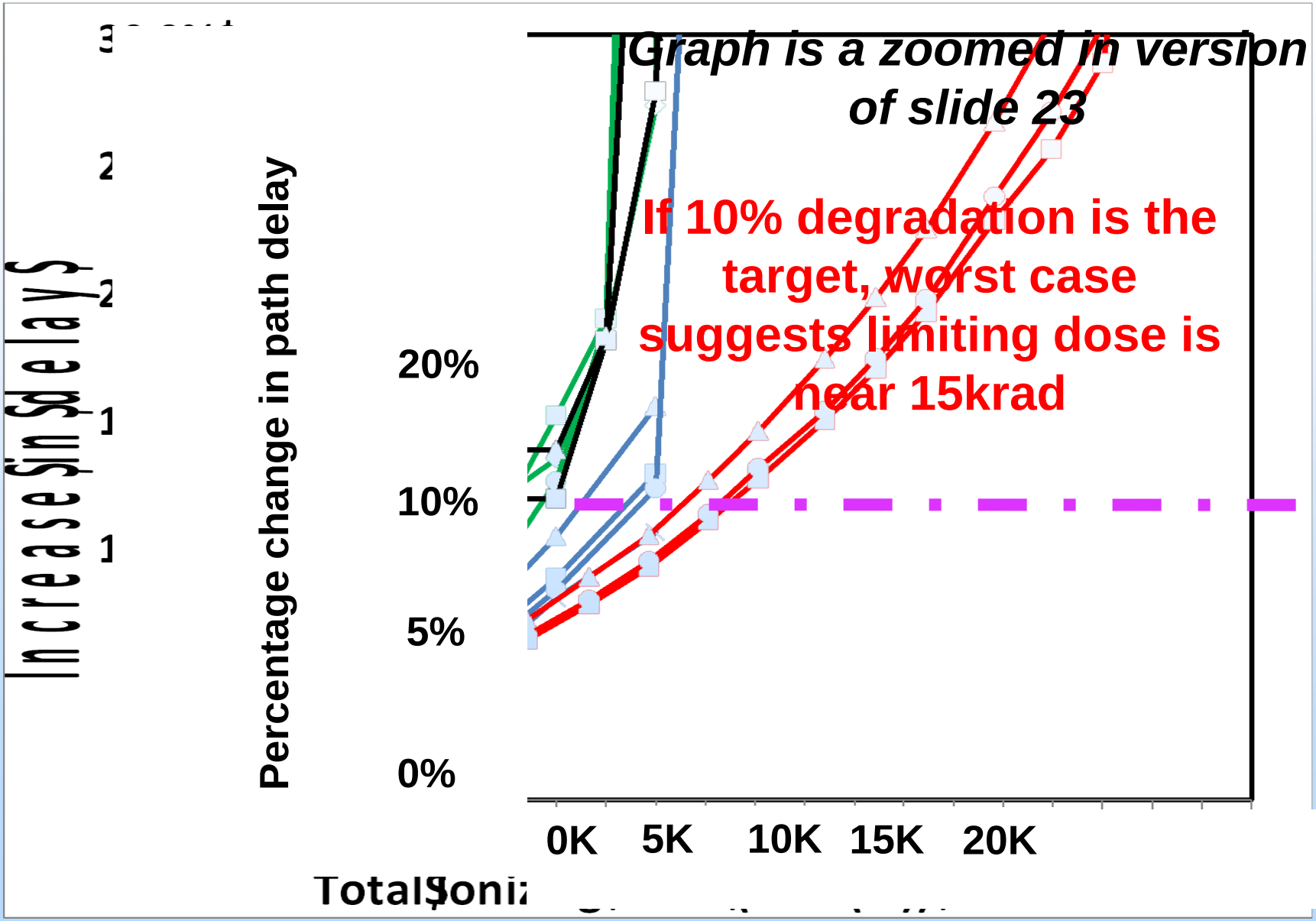
- Although it is important to monitor current during TID testing, more detailed measurements regarding device operation are essential

Relating the Proposed TID Test Method to the Design Environment: Static Timing Analysis (STA) tool

- **STA usage in the design cycle:**
  - **Validates that every data path is faster than one clock period ($\tau_{dly} < \tau_{clk}$). Usage is mandatory**
  - **Worst case τ_{dly} will include derating factors:**

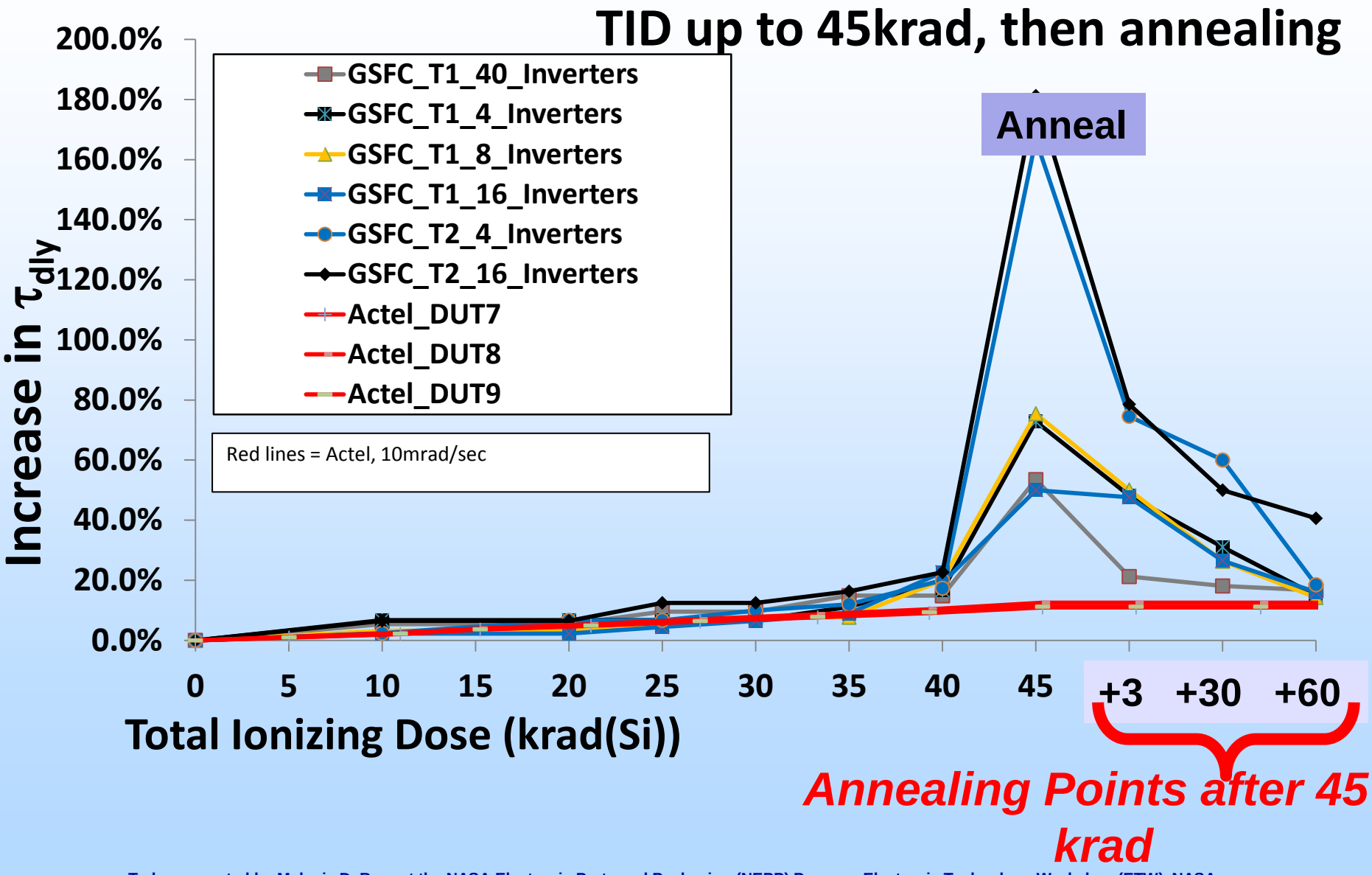
    Example: Although part can run at 200MHz – STA will report that the maximum speed is 180MHz
  - **Guides designers – rule of thumb: maximum reported STA τ_{dly} shall be < 90% of τ_{clk}**
- **STA τ_{dly} is conservative in most cases**
  - **Depending on the environment, STA may not be so conservative**
  - **We should also be conservative when selecting the allowable dose per flight-mission**

Conservative Selection of Dose Limitation



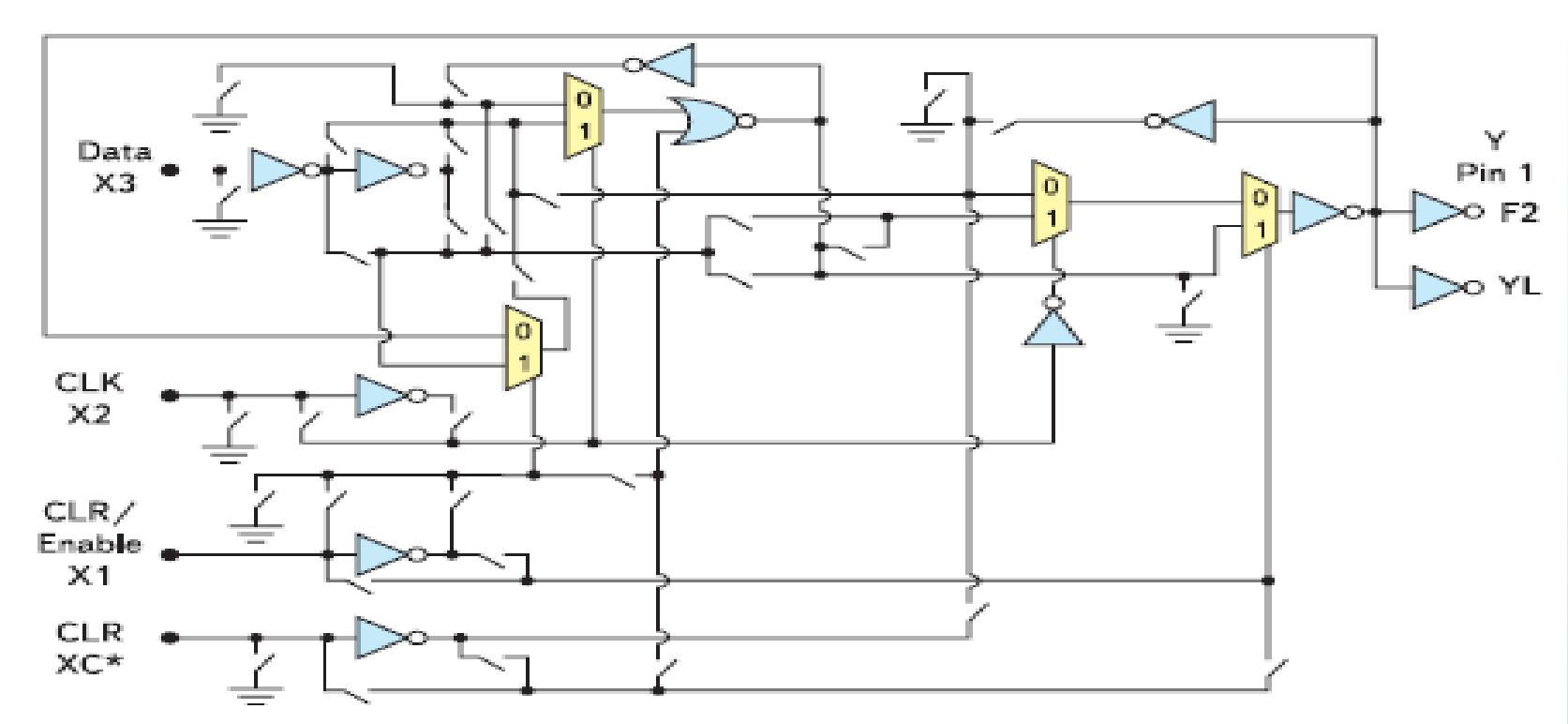
Technical Highlights

GSFC Versus Actel ProASIC3 TID Test Results-2



Technical Highlights

GSFC Versus Actel ProASIC3 TID Test Results-3



- Analysis shows that timing degradation comes from the flash controlled switches within the ProASIC3 data path.
- Increase in complexity can increase timing degradation
- Counters had more degradation than shift registers
- New methodology exposes more extreme cases of degradation

To be presented by Melanie D. Berg at the NASA Electronic Parts and Packaging (NEPP) Program Electronic Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 11-13, 2012 and published on http://nepp.nasa.gov/.

Plans FY12

- Enhance resolution of I_{clk}
- Explore correlation of circuit complexity by testing various complex test structures; *e.g.*, Digital Signal Processing (DSP) blocks
- Utilize this technique in the combined effects (Single Event Effects and TID) study

Conclusion

- **Proposed TID testing methodology benefits:**
  - **Provides a means of measuring internal path delay – removes mixed technology measurements**
  - **Provides worst case…No averaging**
  - **Finer resolution timing-degradation data per dose**
  - **In terms with designer data path delay measurements**
- **We are currently investigating how to improve the proposed methodology (noise reduction)**
  - **Better test equipment**
  - **Additional test structures**
  - **Improved application of clocks.**