

Update on Reliability Testing of CGA/LGA Packages

by

Reza Ghaffarian, Ph.D.

JPL-Caltech

(818) 354-2059

Reza.Ghaffarian@JPL.NASA.com



Jet Propulsion Laboratory

**National Aeronautics & Space Administration
California Institute of Technology**

Copyright 2012 California Institute of Technology

Government sponsorship acknowledged

NASA Electronic Parts and Packaging Program (NEPP)

3rd Annual Electronics Technology Program (ETW)

NASA Goddard Flight Center (GSFC) , Greenbelt, MD

June 11-13, 2012

Published on nepp.nasa.gov

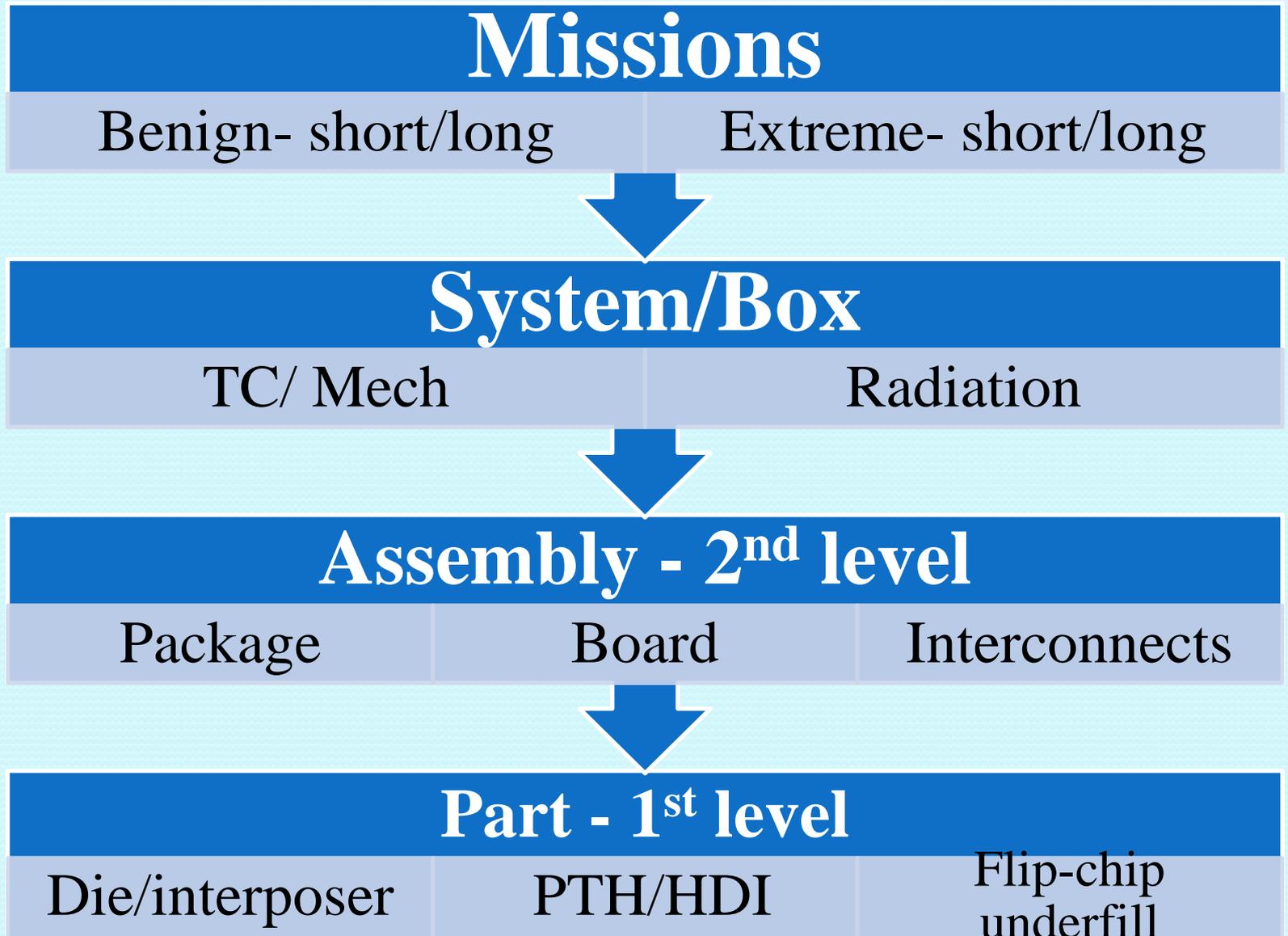


Outline

- Reliability Approaches
 - Mission requirement/system level
 - 2nd level, assembly/package
 - 1st level, part
- CGA/LGA Reliability Test Results
 - LGA/CGA
 - Chip Cap., Optical/SEM characterization
 - LGA/CGA assemblies
 - CGAs, thermal cycles status
 - Chip Cap., SEM/X-section/elemental maps after TCs
- Summary



Reliability Levels

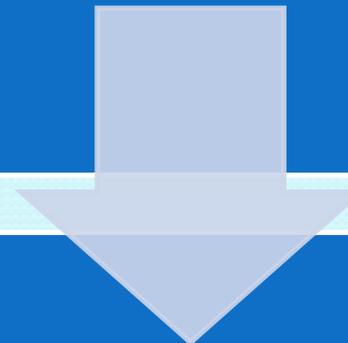




SMT Array Reliability - I

SMT

- Area Array (single/stack)
- PCB, (PTH/HDI)
- Interconnects (CBGA/CGA)
- Stake/Coat/Underfill



Advanced Arrays

- Hermetic/Non-H
- LGA
- FCBGA/interposer



SMT Array Reliability- II

SMT/Advanced Arrays

Assembly, 2nd level

- Class Y, >1000 I/Os
- Hermetic, <1000 I/Os
- Interconnects, Pb & Pb-free

Part, 1st level

- Chip cap
- FC balls/underfill
- Interposer



Reliability Testing of LGA/CGA

FCBGA

- Assembled Pb & Pb-free
- Completed thermal cycles/Drop Test
- X-ray & X-sectional evaluation

LGA

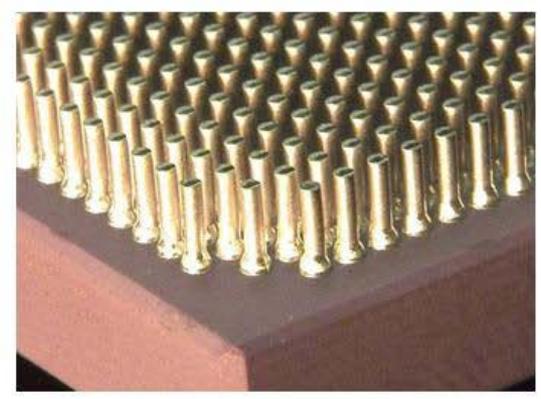
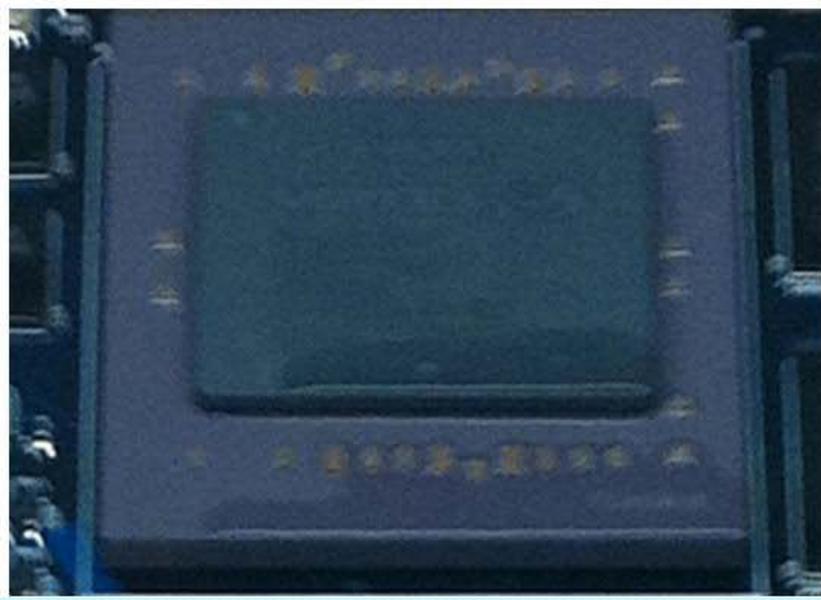
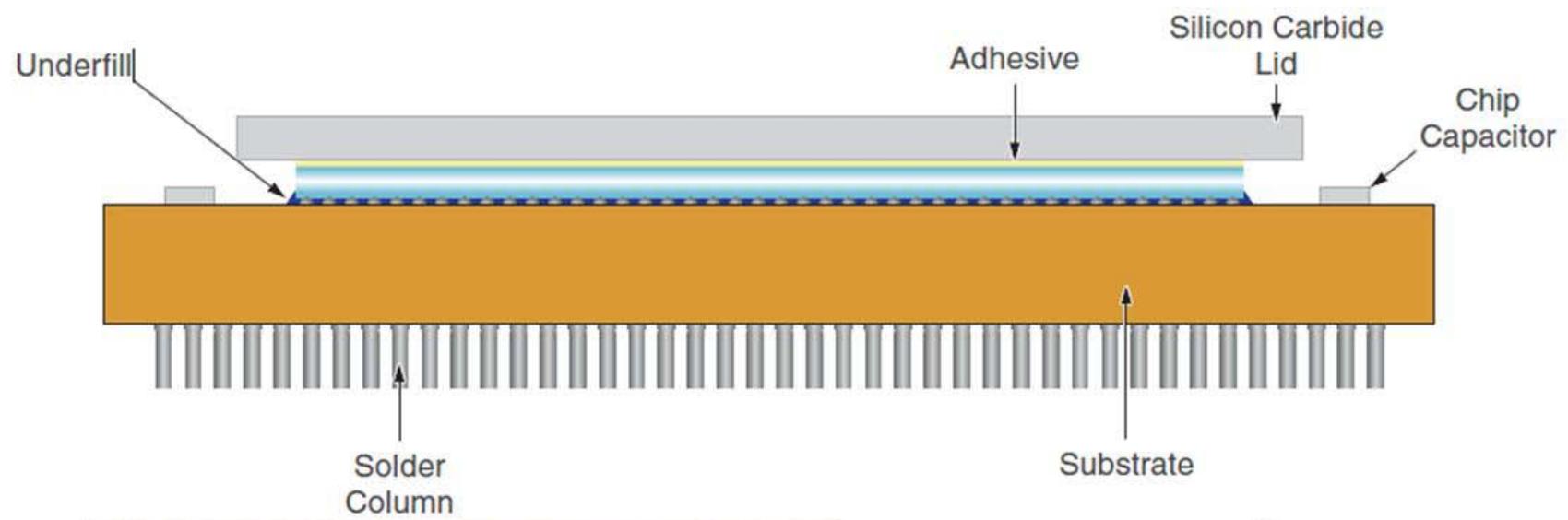
- Column attach/pull test/age-pull test
- CGA (4 package sizes) assembly onto PCB
- LGA version

CGA

- Package/capacitors reliability evaluation
- Successful Assembly CGA onto PCB
- Environmental tests
- CGA Cap TC- X-section/SEM/Map

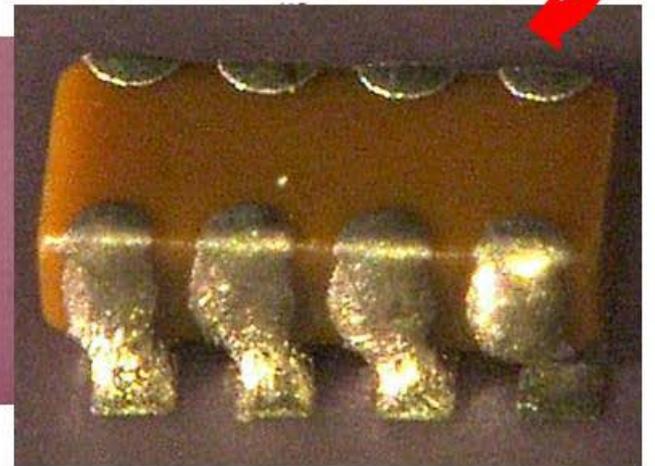
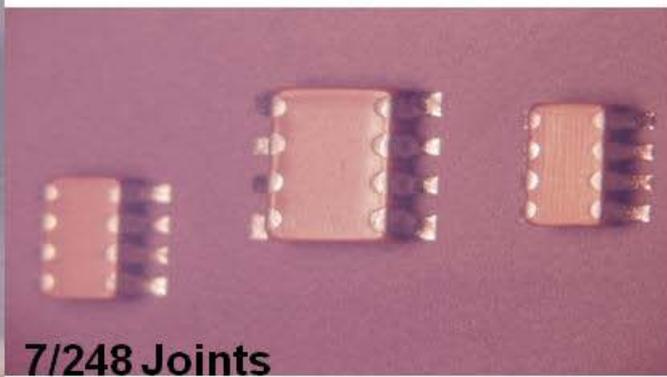
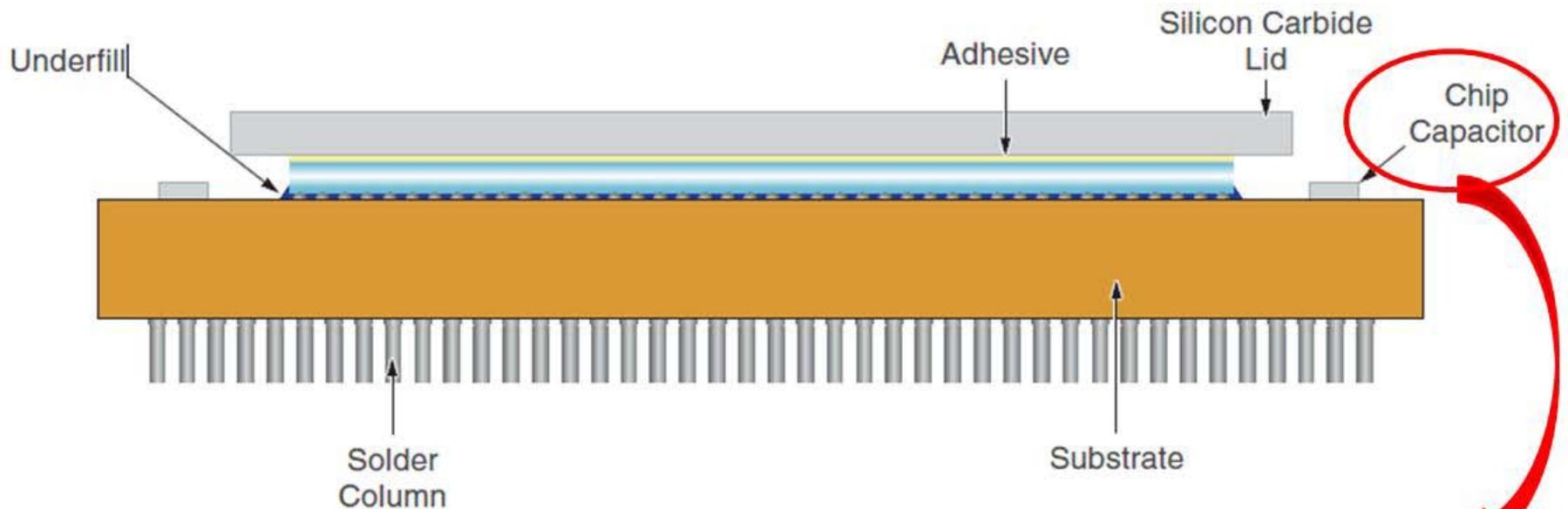


CGA with 31 Chip Capacitors



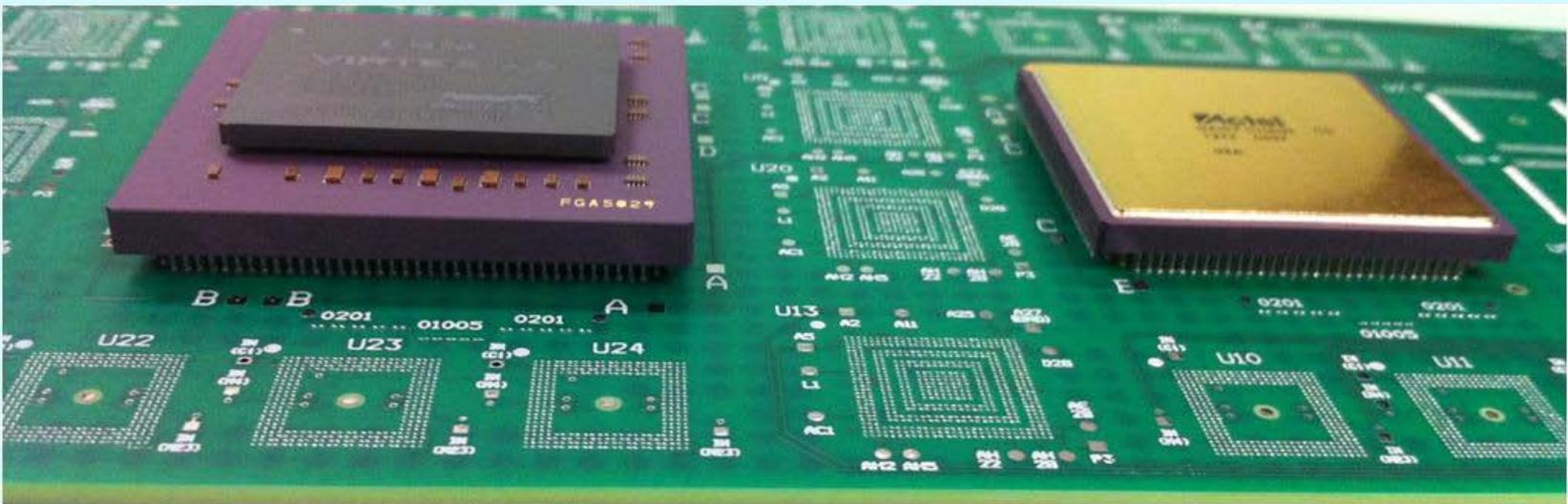


CGA with 31 Chip Caps



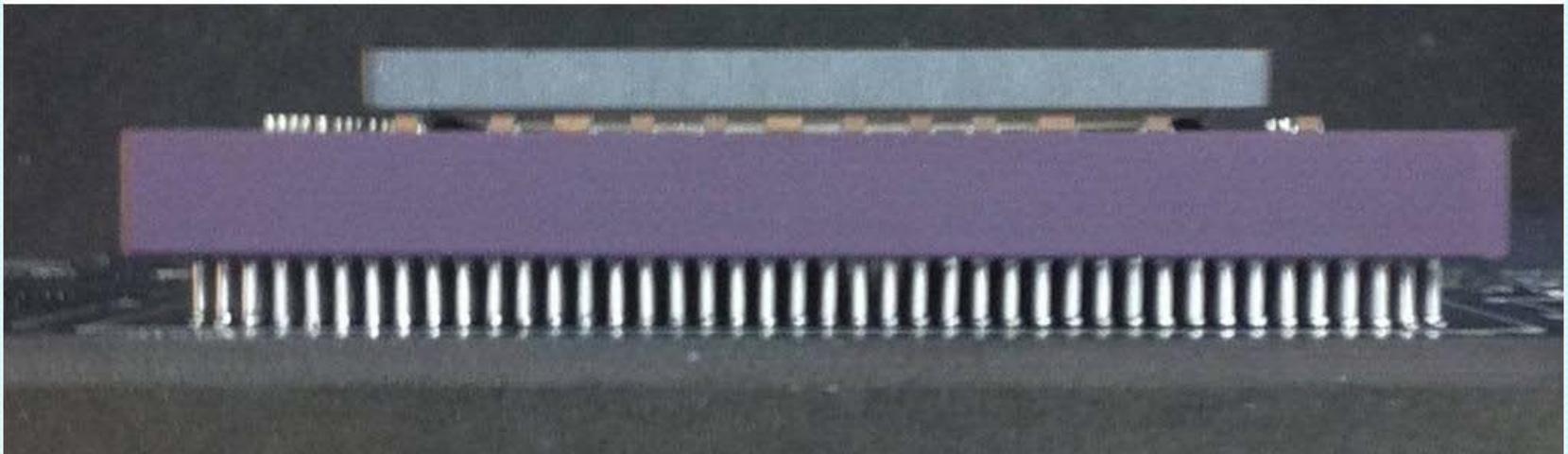
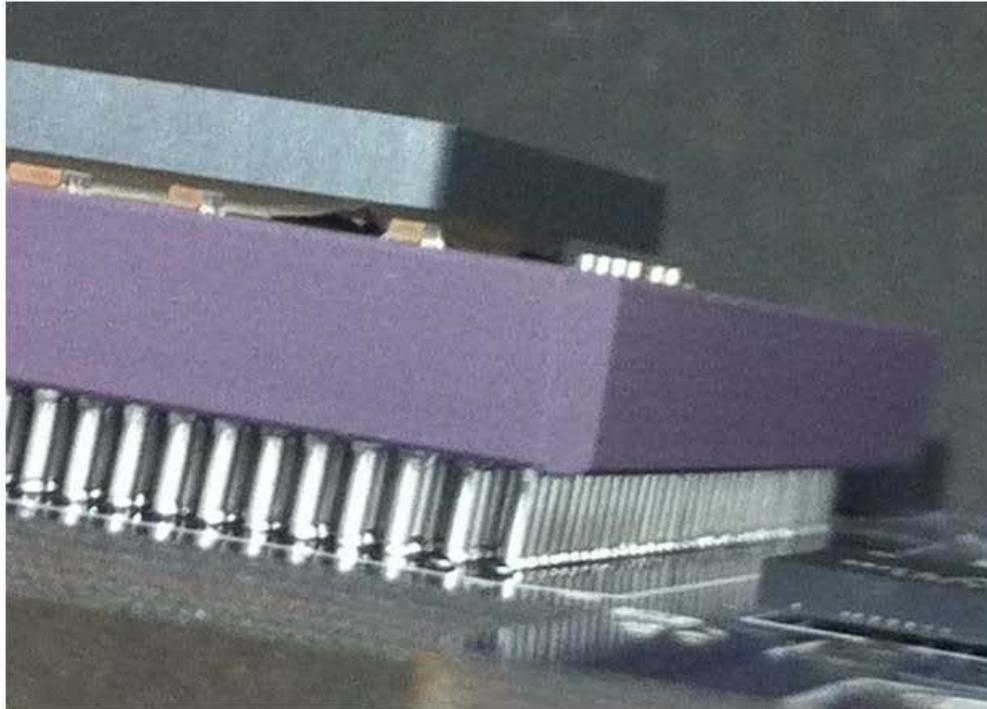


Two CGA Assembly



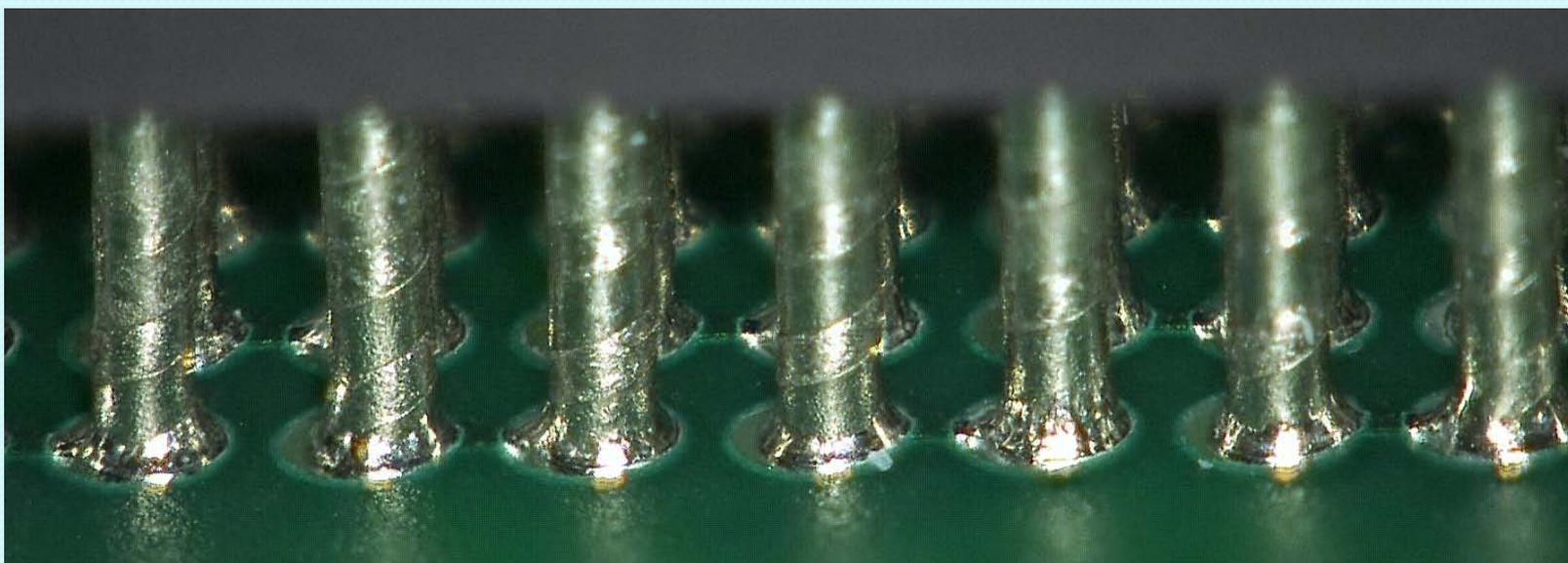
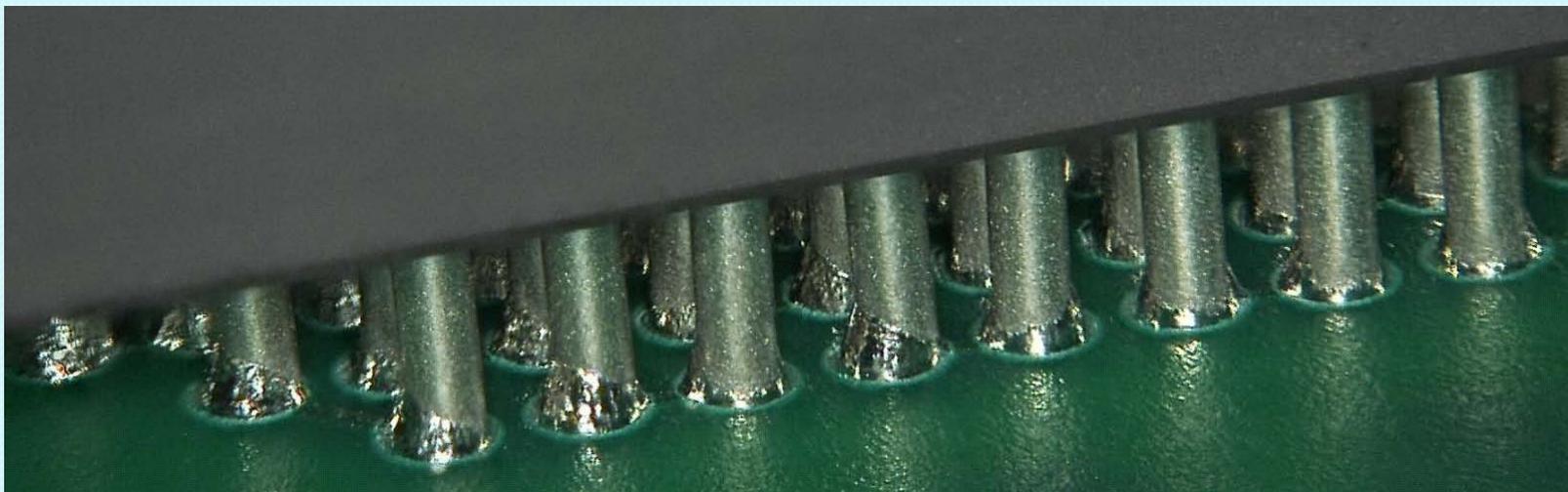


CGA Solder Joint Assembly



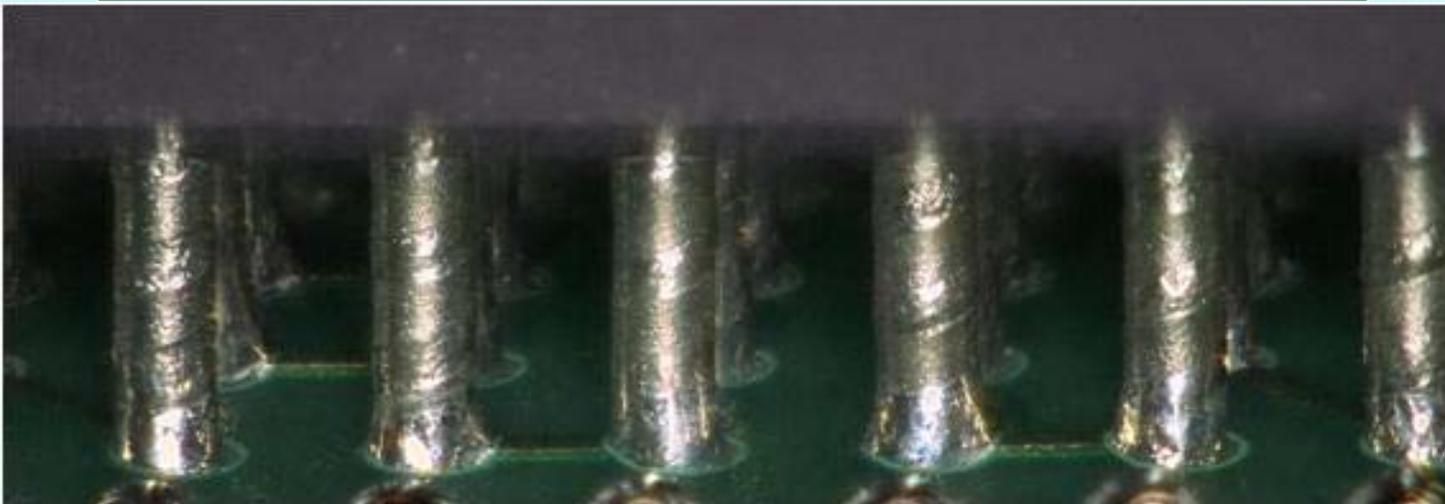
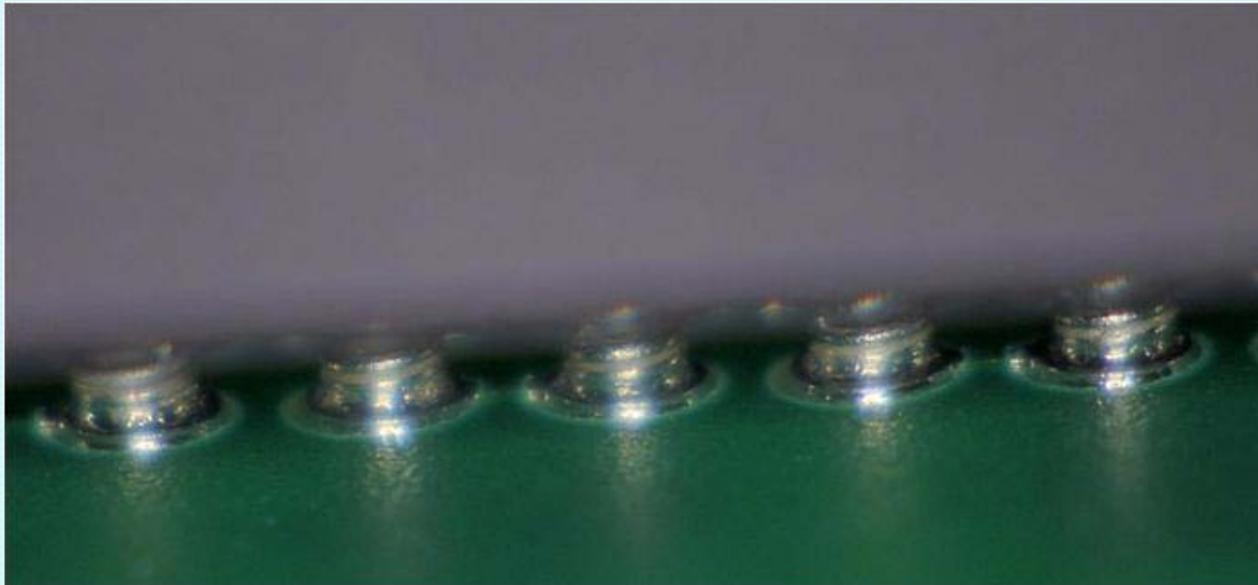


Solder Joints/Columns for 2 CGAs





LGA/CGA/Assembly





NASA Micro-Coil Spring License to STI Electronics Inc

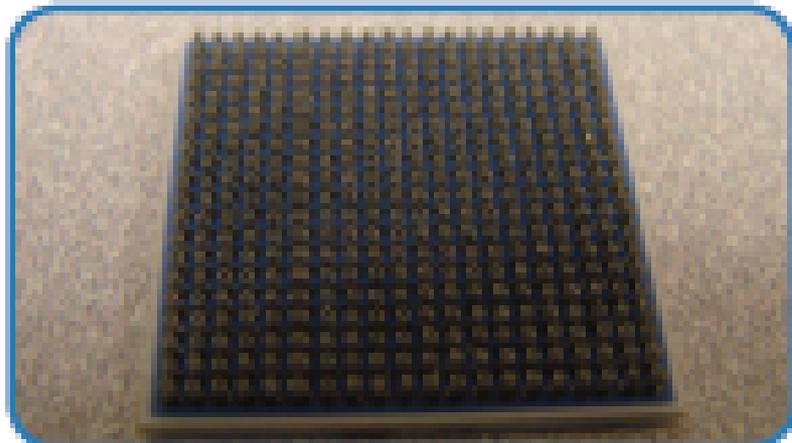
MICRO-COIL SPRING ARRAY

BY: MARK MCMEEN

INTRODUCTION:

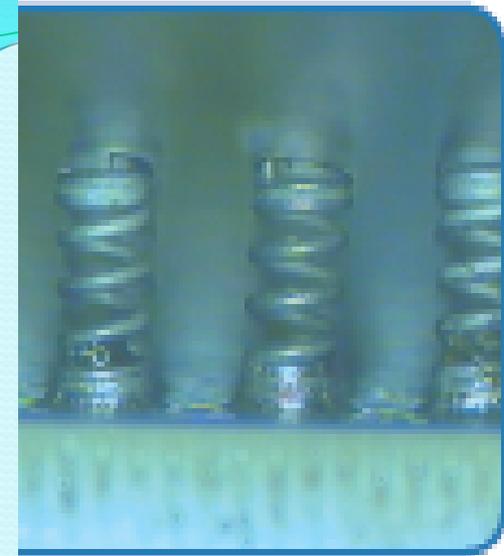
Micro-Coil Spring Array is being introduced as an improved alternative to standard rigid arrays to replace the Column Grid Array (solder columns) commonly used on Integrated Circuits (IC) with a very high lead count. The Micro - Coil Spring Array was developed by NASA for higher degree of reliability over conventional Column Grid Arrays and this technology was licensed to STI Electronics, Inc. for its commercialization and production capability.

Micro springs will form a more robust solder joint. The interconnect of the spring to the substrate consists of the wire on one side of the spring resting on the solder pad in a circular pattern. The result is two separate solder joints along the length of the circular pin, one internal to the spring and one external to the spring.





Micro-Coil Spring Column



INNOVATION:

The Micro-Coil Spring Array consists of an IC connected to PC Board via micro springs. The springs are soldered to the IC substrate then the package is mounted to the PC substrate using conventional Pick and Place equipment.

The flexibility of the micro springs provide a robust Interconnect from the IC substrate to the PC substrate that is much more reliable than rigid interconnects such as Column Grid Arrays. The ability to be compliant and not rigid aids in long term reliability

SPEED/ THROUGHPUT IMPROVEMENTS:

Micro-Coil Spring Array is installed using conventional Surface Mount Pick and Place equipment. This technology allows for the elimination of underfills because its capability for handling and distributing stress – compliance under loading allows the stresses to be negated.

QUALITY CONTRIBUTION:

The use of the micro coil springs provides conformity from the PC substrate to the IC substrate. The flexing of the springs will prevent solder cracks from forming by absorbing thermal or mechanical stress that would normally transfer to the solder joint via rigid interconnects.

COST BENEFITS:

Competitively priced to be lower than column grid array solder columns as well as lower production assembly costs for manufactured of the column grid array package.

ENVIRONMENTAL CONSIDERATION:

The objective from day one was to develop a solder column that could be compliant to environmental loading such as mechanical and thermal stress and thus create a more robust solder connection. The end of objective is greater reliability by surviving longer thermal cycles and minimizing fatigue fracturing.

EASE OF USE/IMPLEMENTATION:

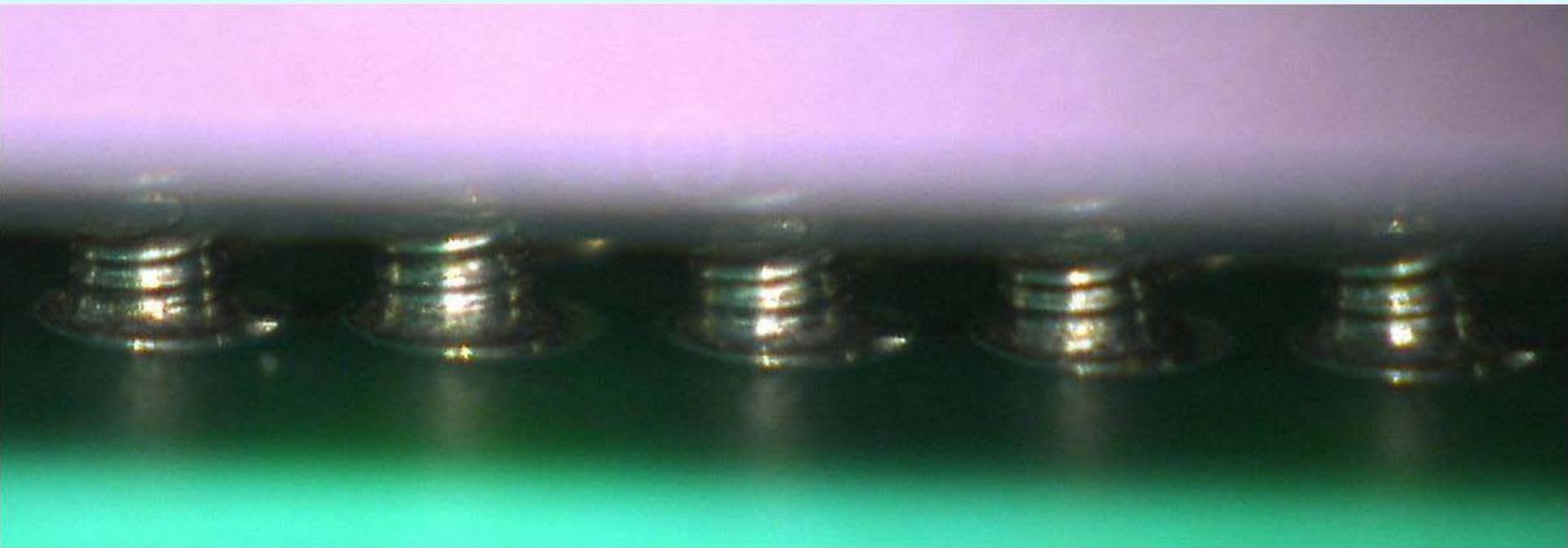
The Micro-Coil Spring Array is a drop in replacement for a BGA column grid array packaging applications that want greater reliability and long term robustness.

MAINTAINABILITY/REPAIRABILITY:

The Micro-Coil Spring Array can be easily repaired using a standard BGA rework station and reworking of the column grid array. High temp solder is used for attachment to the component BGA package and then one can use leaded or lead free solder when attaching to the printed circuit board itself.

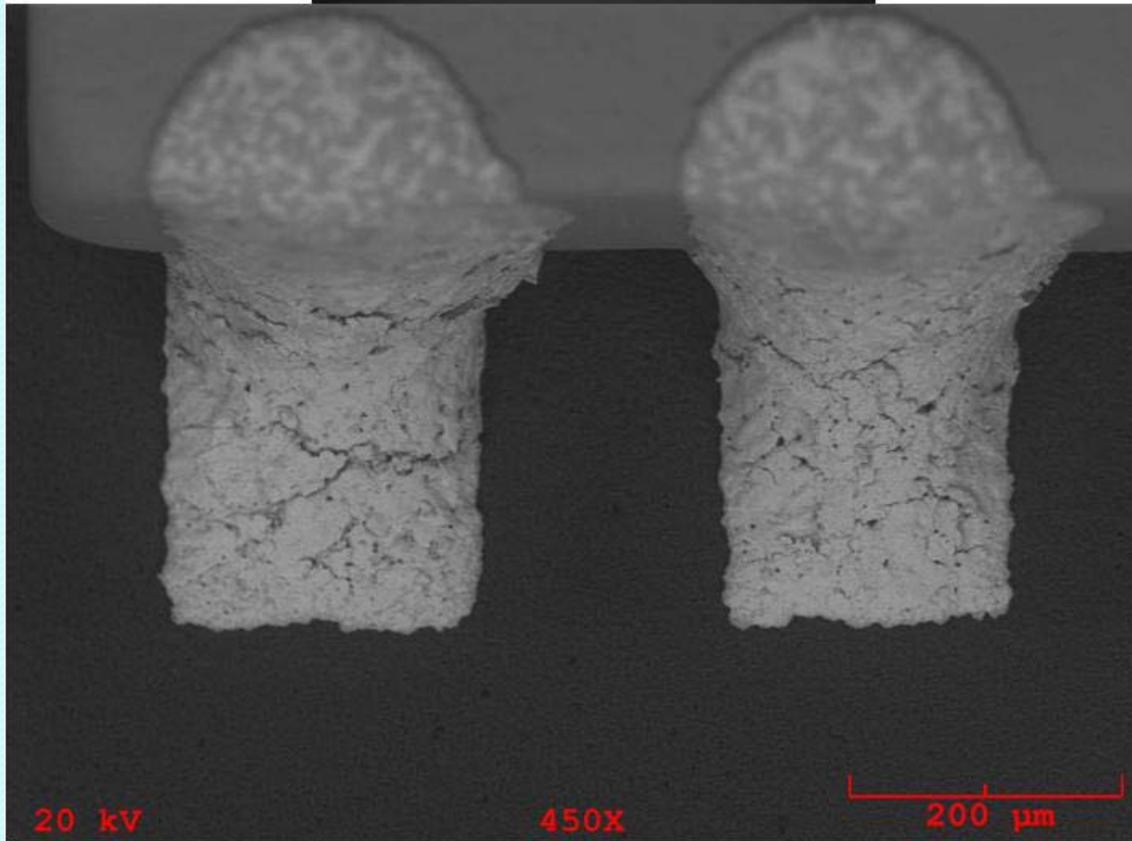
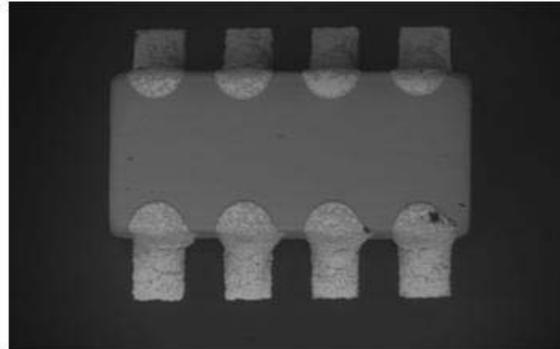


Micro-coil Spring- 200 TCs





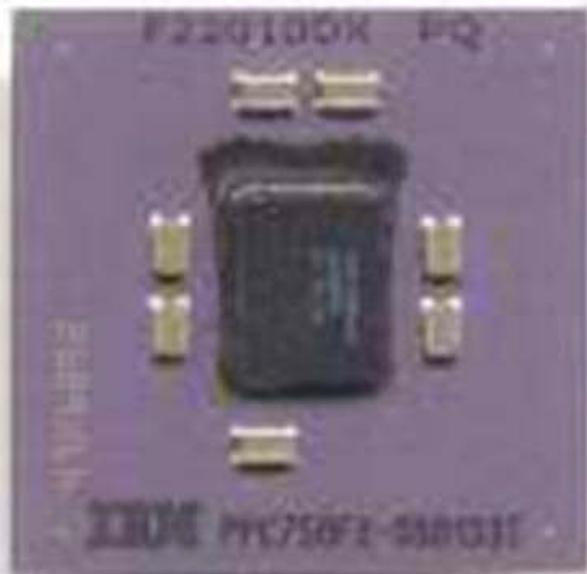
Cap. Solder Joints after TCs





BME History

- BME Caps
 - Decoupler Caps on Power PC, BGA type
 - Advanced CGAs





Reliability of BME Caps

- **BME/PME** (NASA: Liu/Sampson, 2011, NEPP)
 - Higher dielectric variations for same BME
 - Denser and uniform microstructures
 - 0.3-0.5 microns
 - Thinner and more layers
 - PME random failures under HALT
- **HALT** (25volt rated Caps, 155/165/175°C, 150/200/250Volts)
 - BME early failure/Avalanche break down
 - Fabrication defect
 - Critical : Number of stack grains
 - Longer- Wear out of dielectric
 - MTTF, 10^5 years at RT (excluding early failures)
- **Recom.**
 - Improve processing controls/defects
 - Use below extrinsic defect triggering

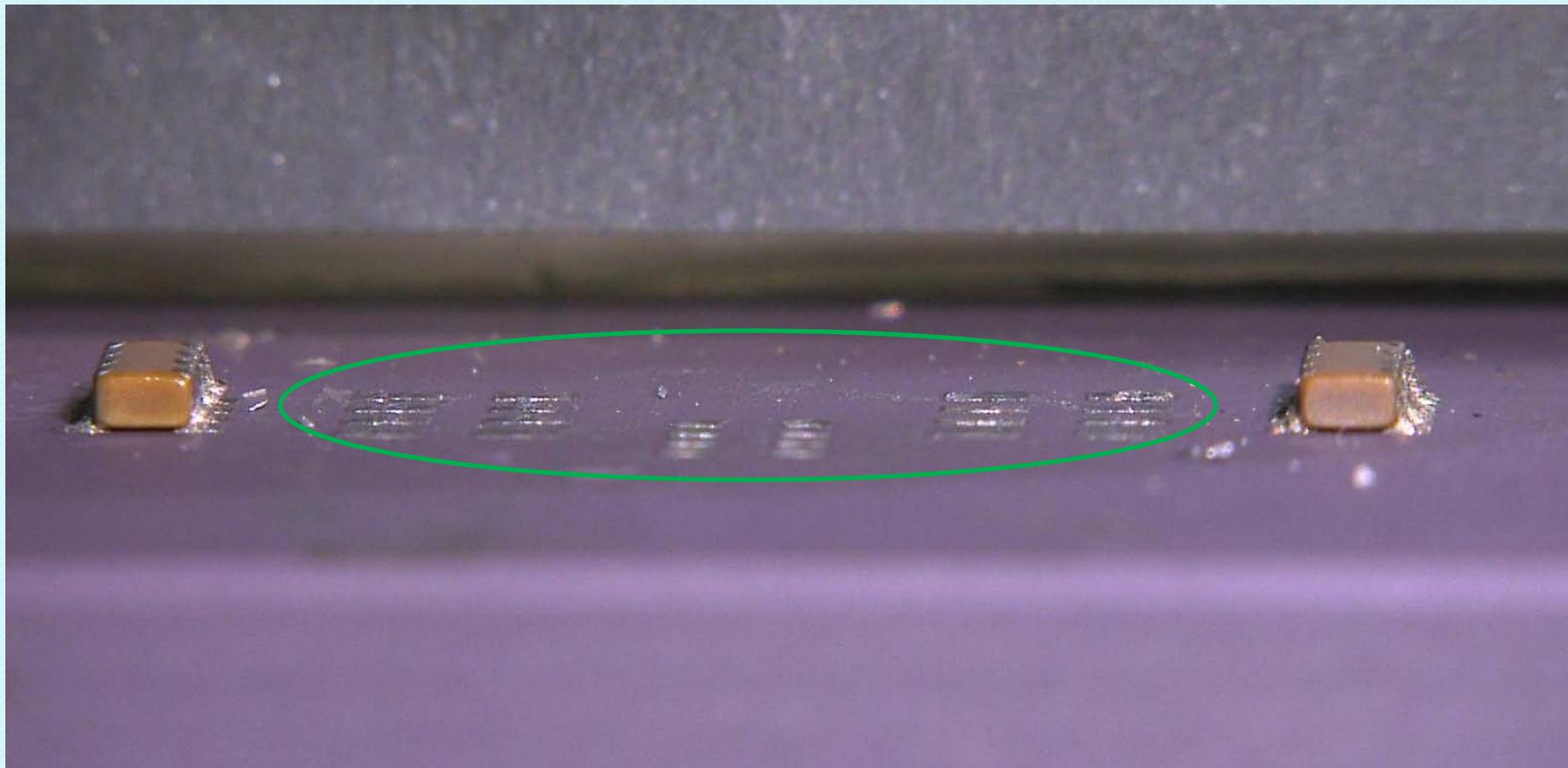


MLCC Capacitors

- **PME** (precision Metal Electrode)
 - Reliability (bias/temp) well established
 - Mix of Palladium Silver Electrode
- **BME** (Base Metal Electrode)
 - High density, commercial/cost
 - Ni electrode
 - Barium Titanate- BaTiO_3
 - Tetragonal (0/130C) on face centers, Barium at corners
 - Titanium, 1% nanometer offset, voltage/move/storage
 - Thinner dielectrics/more layers than PME
 - Increase in capacitance/volumetric efficiency
- Reliability compromise?



Caps Removed for Eval



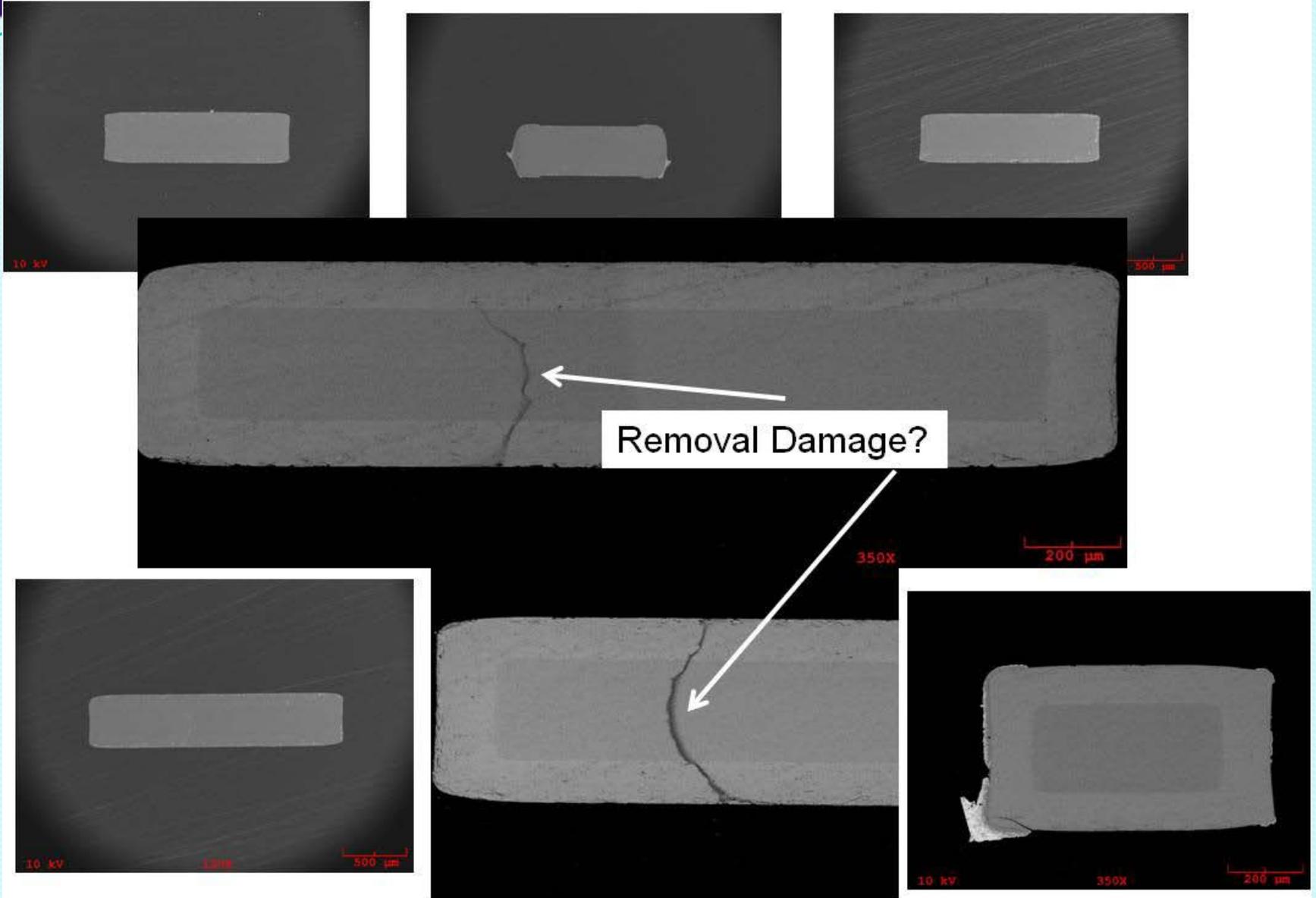


Caps on CGA after TCs

- CGA Thermal History
 - Package subjected to thermal shock (-55/130°C)
 - Reflow for Assembly (218°C)
 - Additional TCs package on board
- Characterize CGA assemblies
- Caps Removal
 - Mechanical
 - Solder cut, then Caps pushed/removed
 - Shear off by twisting, concern, mechanical damage
 - De-soldering
 - High Temp Solder
 - Not tried yet, concern thermal shock

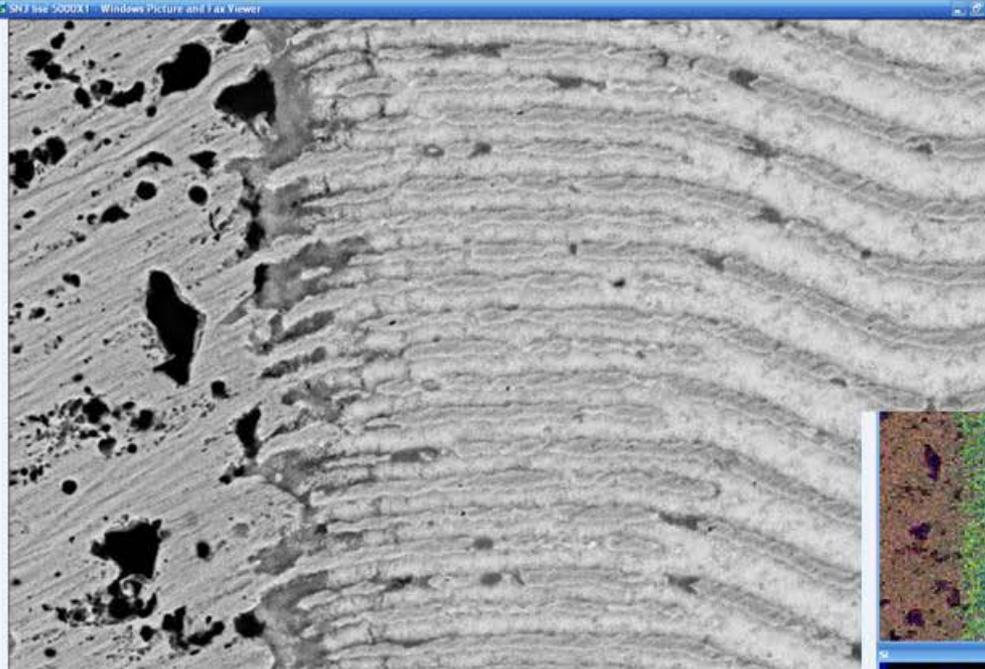


X-sections of Caps

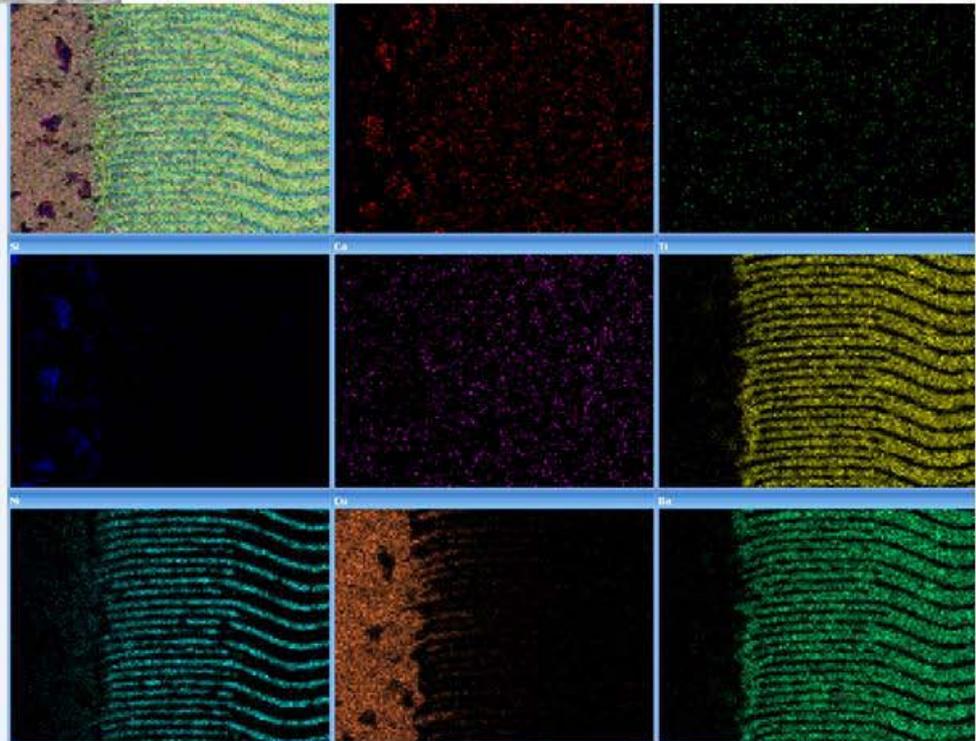




Elemental Map



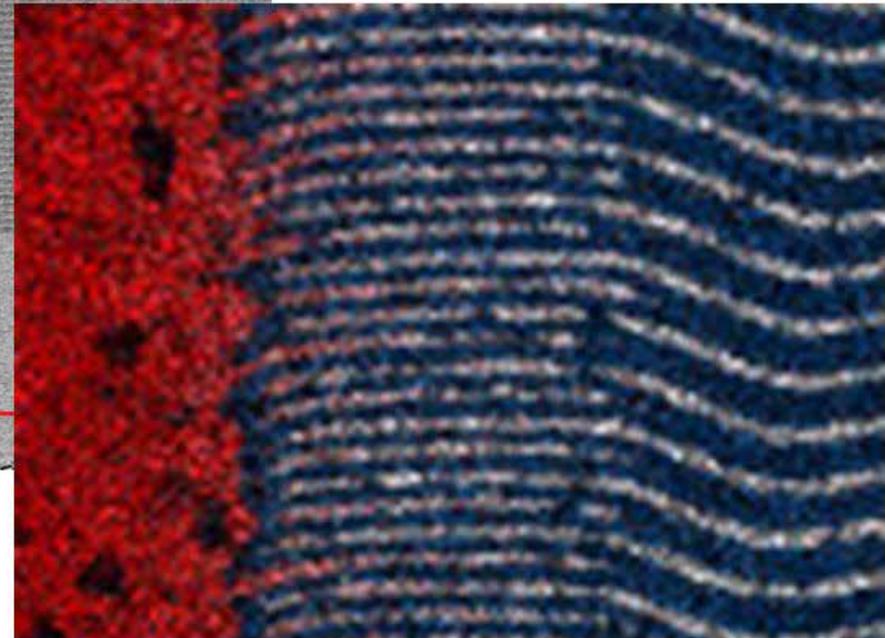
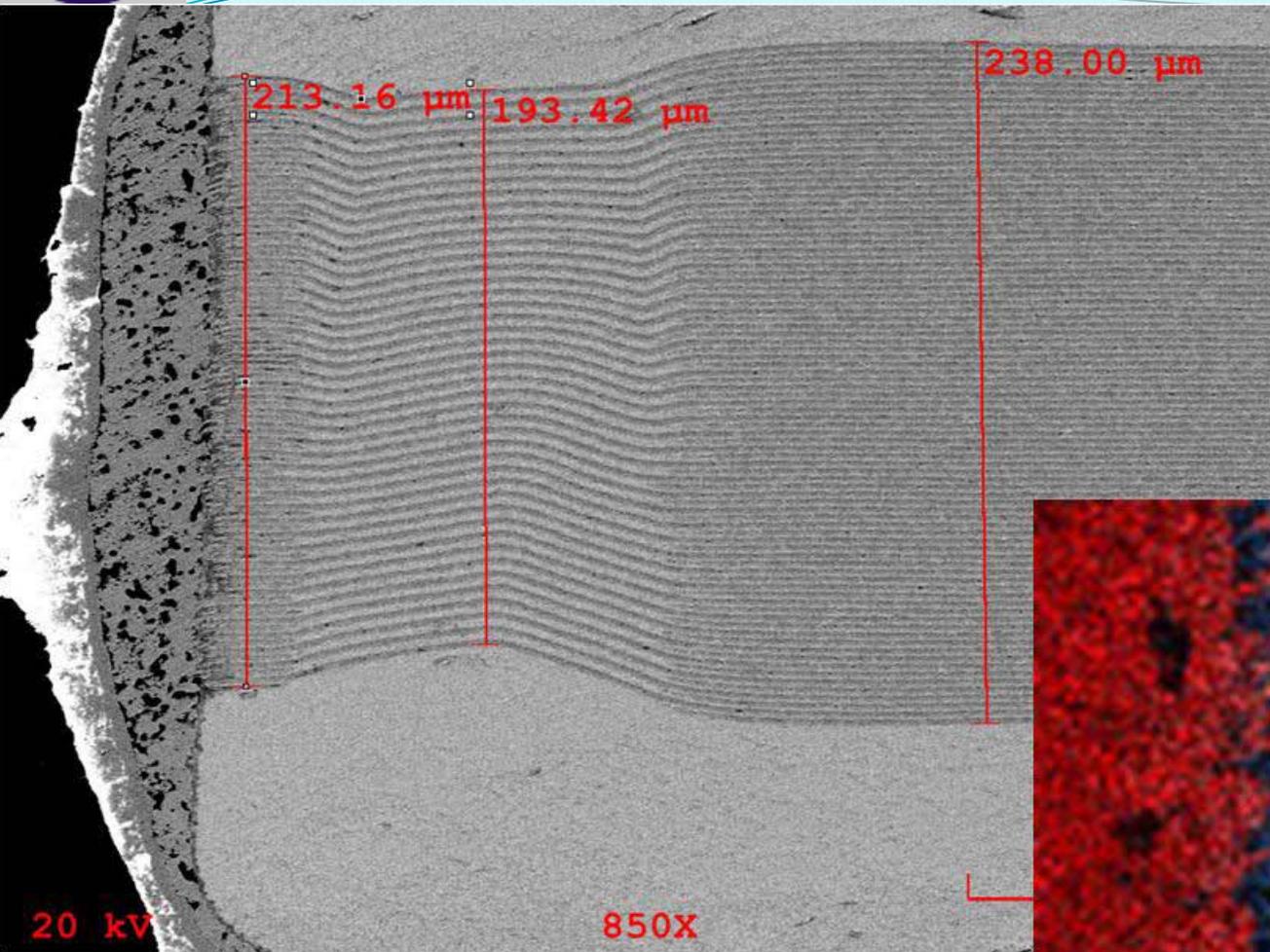
10 μm^* Mag = 5.00 K X EHT = 20.00 kV Signal A = BSD Date : 16 May 2012
WD = 10.7 mm Time : 11:33:19



Ready



Elemental Map





Summary-I

- **Advanced LGA**
 - Success on Cu wrap column attach
 - Column pull test as attached
 - Column pull tests at intervals of aging at 125°C/500 hrs
 - Success on Micro-coil spring column attach
 - No signs of damage after 200 thermal cycles
- **Advanced CGA**
 - Caps on CGA
 - Inspected solder joint quality
 - CGA thermal shock cycles
 - No failures of caps
 - One solder joint apparent separation



Summary- II

- Success on LGA/CGA on PCB Assembly
 - Released interim report
- Advanced LGA/CGA
 - Reliability testing of CGA assemblies
 - LGA/CGA & assembly on standard PCB
 - Daisy chain monitoring when applicable
 - Damage monitoring and NDE/SEM evaluation
- Caps after TCs
 - Literature search understand reliability
 - X-sectioned 6 caps, SEM evaluation
 - Elemental Maps
 - Caps are BME with BaTiO₃ cap/Ni electrodes/Cu terminals
- Design boards with HDI (microvia)
 - Assemble onto HDI board/optimize process
 - Reliability testing
- Active die, HDI, Reliability
 - Use lessons learned for efficient resource utilization
 - Release report



Acknowledgment

The research described in this publication is being conducted at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

Copyright 2012 California Institute of Technology. Government sponsorship acknowledged.

The author would like to acknowledge industry/university partners. Special thanks to the JPL fabrication and failure analysis lab personnel including Atul Mehta and Ronald Ruiz for their supports. The author also extends his appreciation to program managers of NASA Electronic Parts and Packaging Program (NEPP) including co-managers Michael Sampson and Kenneth LaBel at GSFC, and Drs. Charles Barnes and Douglas Sheldon at JPL, for their continuous support and encouragement.

References

<http://NEPP.nasa.gov>