Through Silicon Via (TSV) Technology Status

Jerry Mulder, JPL

R. Peter Dillon, JPL

June 12, 2012

To be presented by Jerry Mulder at the 3rd NASA Electronic Parts and Packaging (NEPP) Electronics Technology Workshop (ETW),
NASA Goddard Space Flight Center in Greenbelt, MD, June 11-13, 2012 and published on nepp.nasa.gov

Through Silicon Via (TSV) Technology Status Outline

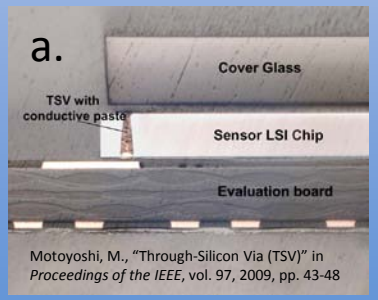
- Task Overview
- TSV Technology Overview
- Application Examples
  - Imager CSP
  - Memory Cube
  - Logic and Memory
  - 2.5D/Xilinx Virtex 7
- 2.5D and 3D TSV Commercialization
- TSV Processing: Many Choices
- Other enabling technologies
- Potential reliability issues
- Future of technology
- Coexisting with 3D TSV
- Conclusions and Future Work
- Acknowledgements

Through Silicon Via (TSV) Technology Task Overview

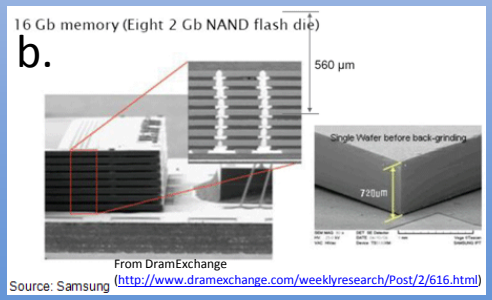
- Our goal is to review the technology readiness and current state-of-the-art of through silicon via technology as it relates to NASA missions, applications, and environments.
- Examine industry trends, applications, manufacturing methods and concerns, cost considerations, vendors, reliability issues and potential show stoppers, and the future of TSV technology.
- Approach in this phase: Literature review of TSV industry, services, methods and processes, applications, issues and reliability, and forecasts. Directly engage TSV service providers and users.

TSV Technology Overview

- Through silicon vias (TSVs): electrical interconnects through a silicon die or wafer.
- Alternative to wire bonding and printed electrical interconnects in 2.5D and 3D packaging.
- Technology Driver: Reduced interconnect length for increased performance.
- Commercial applications continue to emerge for sensors, memory, and FPGAs.

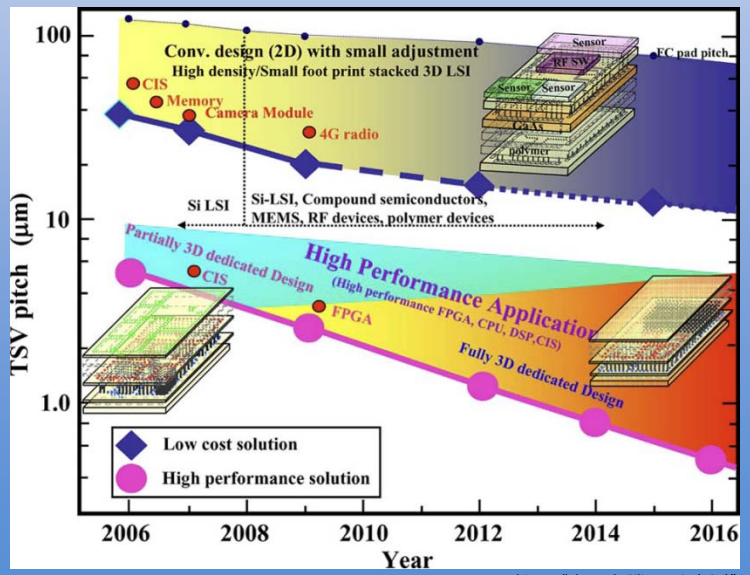


Motoyoshi, M., "Through-Silicon Via (TSV)" in *Proceedings of the IEEE*, vol. 97, 2009, pp. 43-48



From DramExchange
Source: Samsung (http://www.dramexchange.com/weeklyresearch/Post/2/616.html)

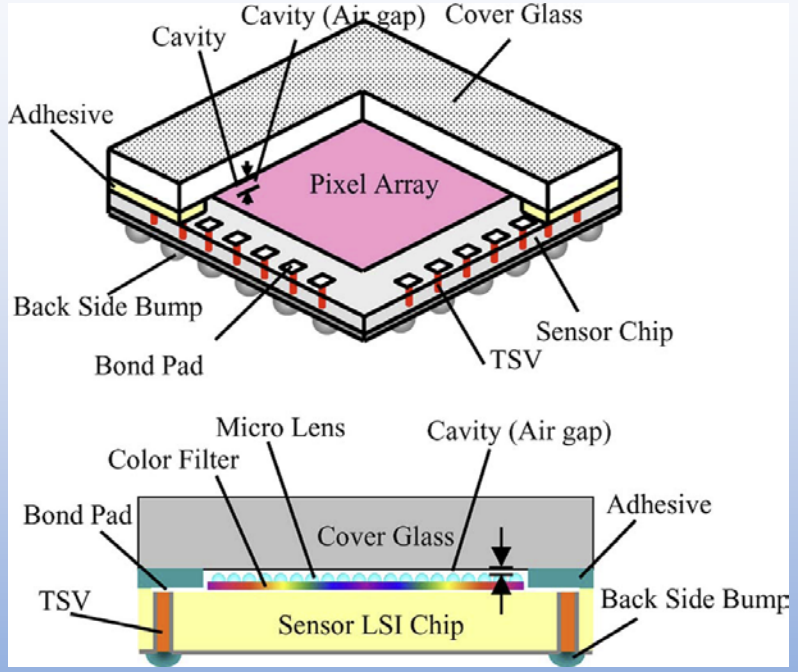
Fig. 1 Commercial applications emerging for TSV technology include (a) sensors, (b) memory, and FPGA (not shown).



Motoyoshi, M., "Through-Silicon Via (TSV)" in *Proceedings of the IEEE*, vol. 97, 2009, pp. 43-48

Application Example: Imager CSP

- Early adopters
- Interconnects do not interfere with top side imaging sensor.
- Direct attach can be made to processing chip, reducing interconnect length, and increasing performance.

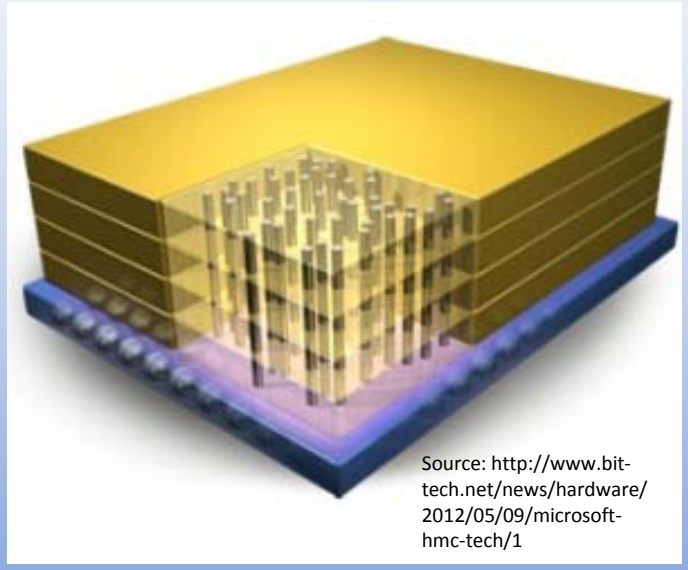


Source: Motoyoshi, M., "Through-Silicon Via (TSV)" in *Proceedings of the IEEE*, vol. 97, 2009, pp. 43-48

Source: Jerray A., "From 3D technology to 3D-IC demonstrators and associated design flow", GSA EDA Interest Group, 2011 Feb. 25th

Application Example: Memory cube

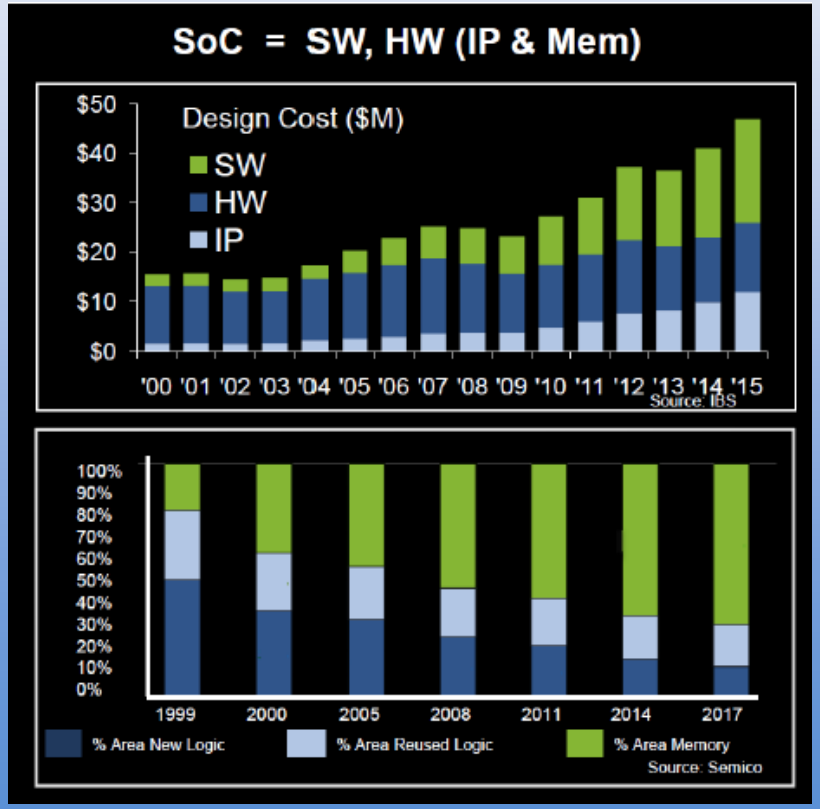
- The Hybrid Memory Cube (HMC) Consortium
  - Memory industry leaders including Micron and Samsung.
- Recent Micron demonstration:
  - Peak throughput of 128GB/s compared to the 12.8GB/s.
    - commercial-grade DDR3 modules created on a planar process.
  - Micron's prototype modules showing a 70 per cent reduction in power draw during data transfer in a module one-tenth the size of current-generation technologies.
- The Hybrid Memory Cube Consortium and industry leaders (e.g. Altera, IBM, Open-Silicon, Xilinx and Microsoft) readying draft interface specification for HMC memory.
- Drivers: improved memory bandwidth and performance; decreased energy and latency for moving data between memory arrays and processor cores.

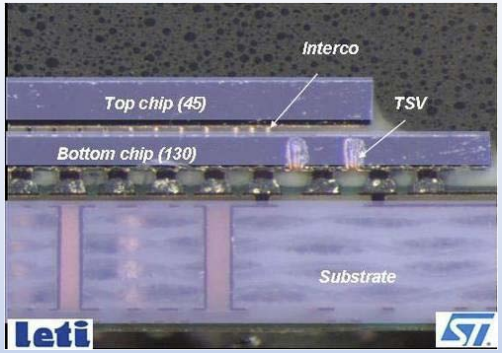


Source: http://www.bit-tech.net/news/hardware/2012/05/09/microsoft-hmc-tech/1

Application Example: Logic and Memory

- Improved processor/ memory performance.





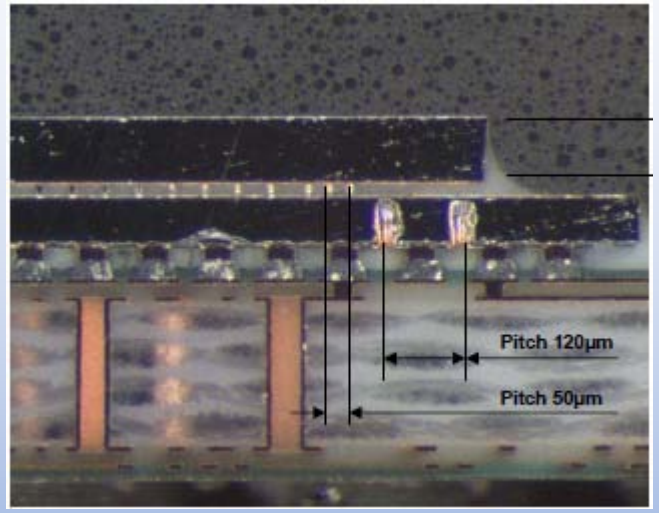
Source: CTI Leti/ST Micro

- 3D appears to be a cost effective approach to manage increasing memory needs and shrinking share of logic area.
  - Fewer packages, improved device yield from chip partitioning, lower power…fewer extras needed
- Enables integration of additional technology.
  - Analog, RF, Sensors/MEMS

Source: Global Semiconductor Alliance (GSA) EDA Interest Group Meeting April 20, 2011

Application Example: 2.5D

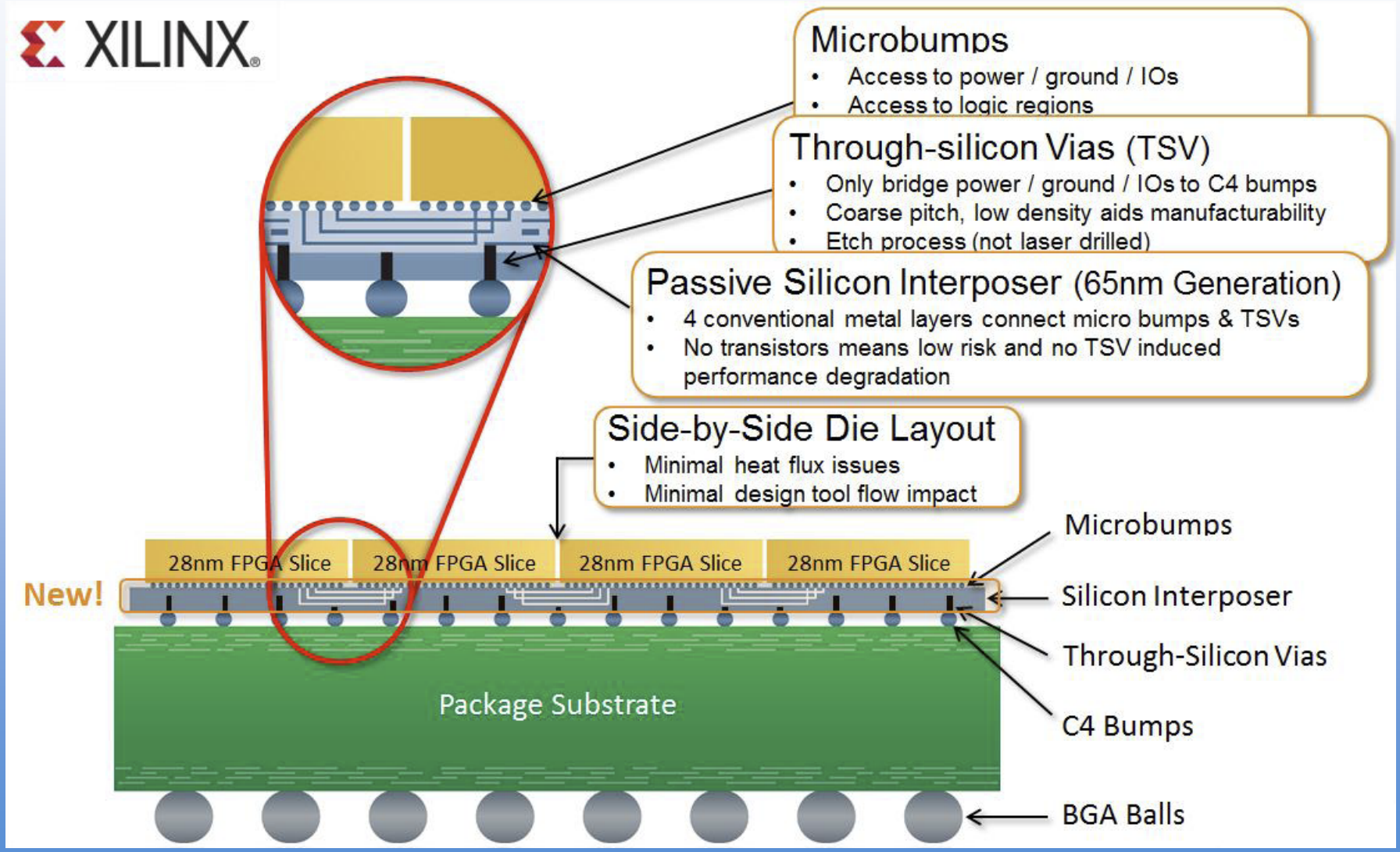
- Vias in passive Si interposer
- Alternative to 3D.
- Supports integration of multiple technologies including passives.
- Potential advantages over 3D (at this time):
  - Low area impact (no keep out areas required).
  - No impact to IC performance.
  - Less disruptive process.
  - Layout techniques similar to PWBs.
- Xilinx Virtex 7
  - Die partitioning improves yield



Source: S. Cheramy, EMPC 2009

45nm technology on 130nm interposer
1056 inter-chip connections
588 TSVs
482 bumps

Xilinx Virtex 7



Rahman, A, "Stacked-Silicon Interconnect Technology" Xilinx, Inc. GSA-EDA Forum, December 8 2010

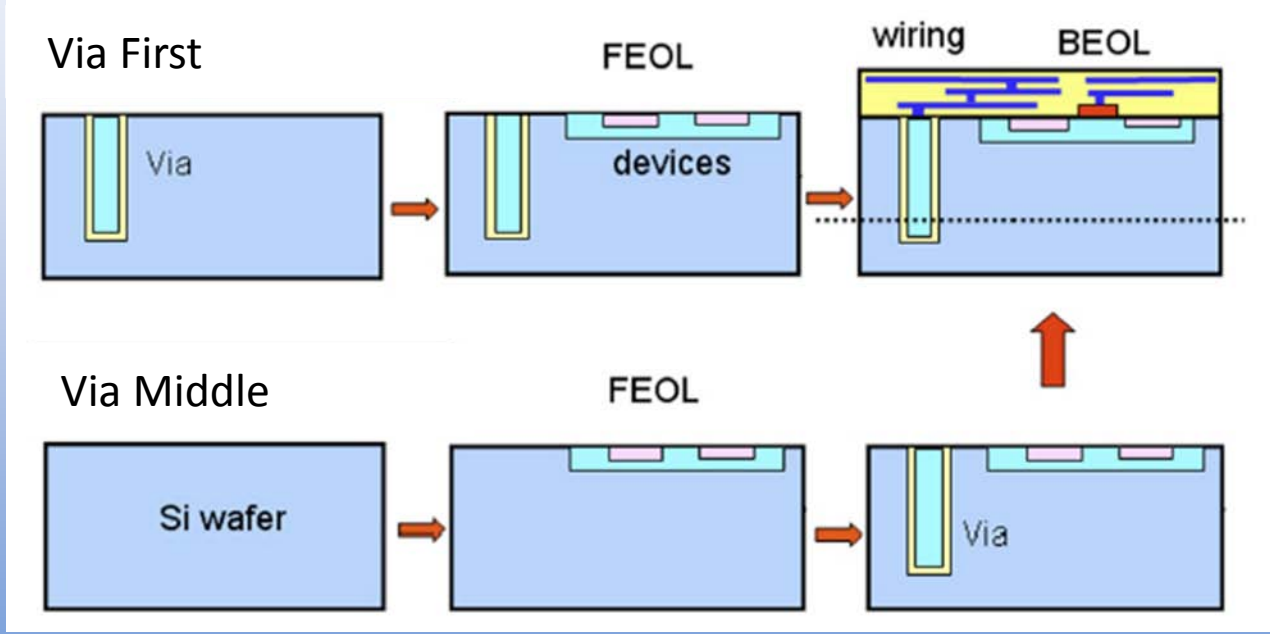
2.5D and 3D TSV Commercialization

Company	Interposers		3D with TSV	
TSMC	2H 2011	[2]	2012-2013	[3]
UMC			2H 2011	[4]
GlobalFoundries			2013	[5]
IBM	2011	[6]		
Samsung			2012	[7]
Elpida			2H 2011	[4]
Micron			2012	[8]
Nanya			2011-2012	[9]
ASE	2012-2013	[10]		
STATSChipPAC			2013	[11]
Amkor	2H 2011	[3]		
SPIL	2011	[12]	2012	[12]
Qualcomm			2013	[12]
Nokia			2012-2013	[12]
Xilinx	2H 2011	[2]		
Dell			2012	[13]

Source: Dr. Phil Garrou, YOLE; http://www.i-micronews.com/lectureArticle.asp?id=6351

TSV Processing: Many Choices

- FEOL: Front end of line
- BEOL: Back end of line
- Via First (polysilicon filled via): TSVs fabricated before transistors.
- **Via Middle (copper filled via): TSV fabricated before copper interconnects.**
- **Via Last (copper liner): TSVs fabricated after bonding the stack.**

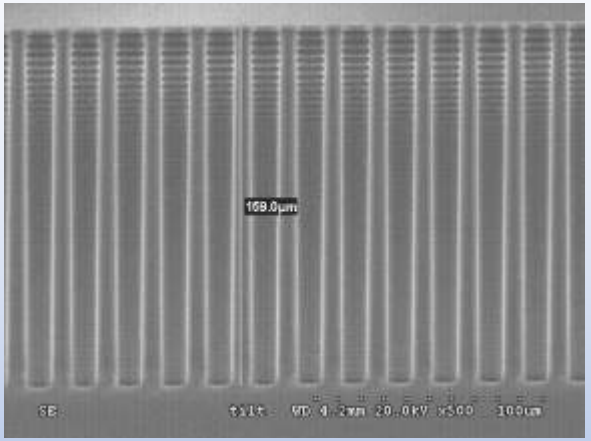


P. Garrou, "Wafer Level 3D Integration," presented at Peaks in Packaging Whitefish Montana, Sept. 5–7, 2007.

Emerging as leading candidates

TSV Processing: More Choices

- Via Processing
  - **Deep reactive-ion etching**
  - Laser
  - Other (e.g. wet chemical etch)
- Via Metallization
  - **Copper electroplating (fill and conformal)**
  - Tungsten
  - Polysilicon
  - Copper paste printing
  - Other (doped silicon, Au plating)
- Interconnects
  - Flip chip ball or stud bump (>100 μm)
  - SnAg and Cu pillars and solder-free μinserts (e.g. Ni) (100-30 μm)
  - μtubes (30-10 μm)
  - Cu-Cu direct bonding (>5 μm)



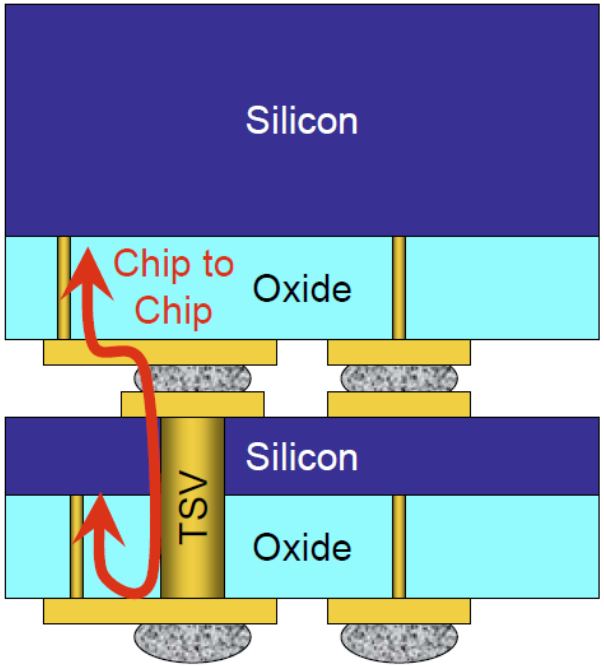
10μm / 160μm deep via
DRIE Etch rate: 9 μm/min

Source: Puech, M. from "DRIE for Through Silicon Via" Alcatel Micro Machining Systems; EMC3D

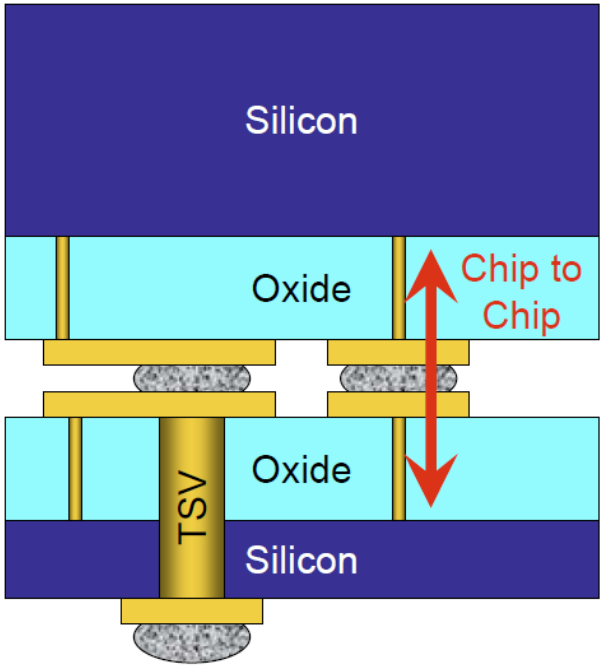
TSV Processing: Still more choices

Multiple Assembly Processes – Wafer to Wafer / Chip to Chip

Face to Back (F2B)
- Easier to Design (No Mirror)
- Chip to Chip requires TSV



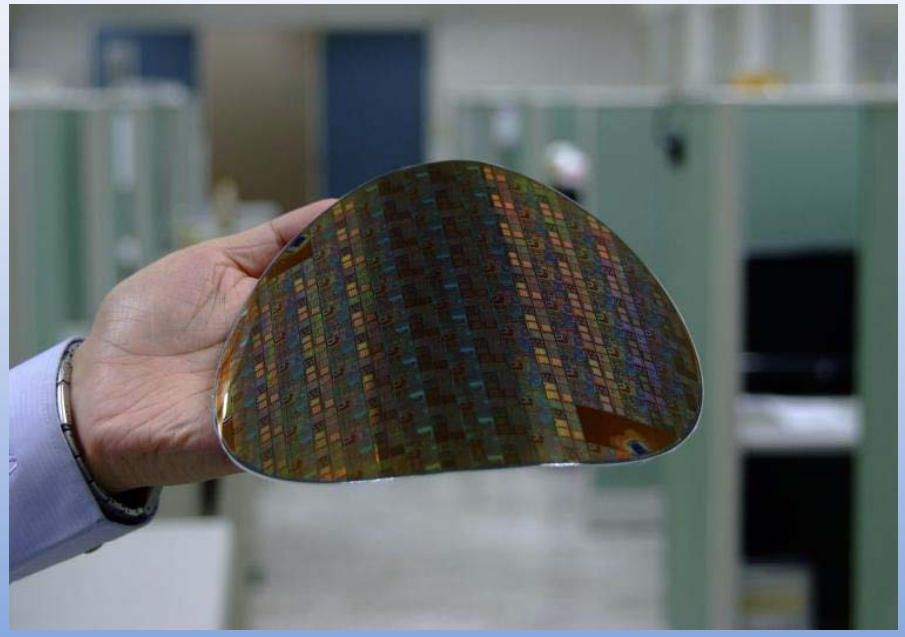
Face to Face (F2F)
- Easier to Process
- Chip to Chip w/o TSV



Source: Barth, J., "3D Design using 2D tools" GSA EDA Interest Group Meeting, February 25, 2011
http://www.gsaglobal.org/eda/docs/3DICDesign-GSAEDAInterest-Barth-20110225-IBMrelease.pdf

Other Enabling Technologies

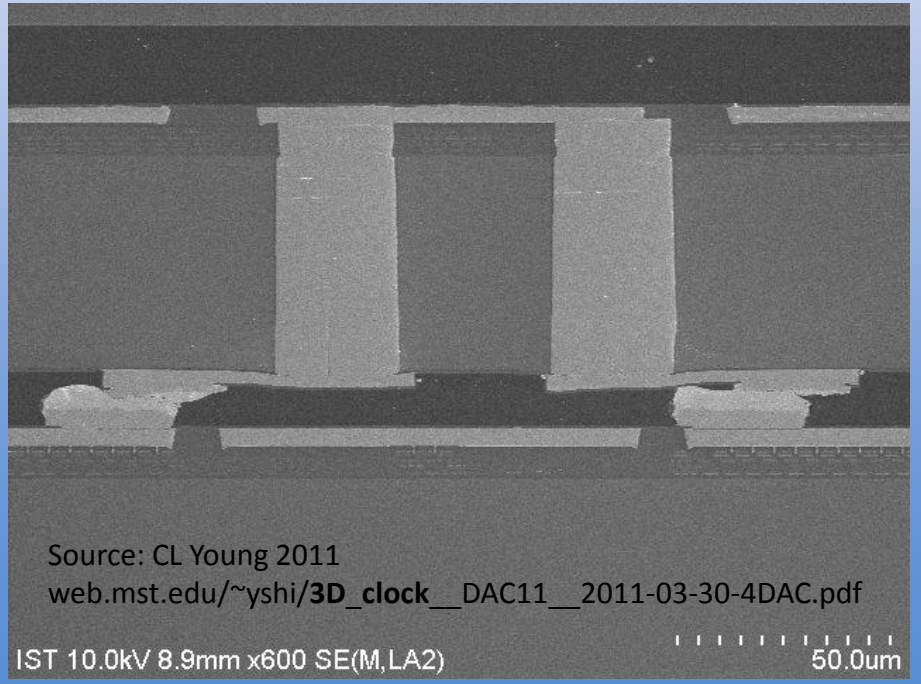
- 3D Electronic Design Automation (EDA) Tools
- Input IC Testing (i.e. known good die)
- Planarization
- Wafer Thinning/Handling
- Alignment
- Bonding
- Testing



Source: CL Young 2011
web.mst.edu/~yshi/**3D_clock**__DAC11__2011-03-30-4DAC.pdf

Potential Reliability Issues

- Design challenges:
  - Present variety of vias and processes muddy the reliability water
  - Stress management
    - Via fabrication may induce tensile stresses in silicon
    - Vias may experience compressive 'hoop' stresses which could lead to via buckling.
    - Quantity and spacing of vias may result in undesirable stress fields
    - Thermally induced stresses due to CTE mismatch may lead to cracking of the silicon wafer.
  - Thermal management: Potentially large and non-uniform heat flow.
  - Redundancy (or the lack of, particularly for space applications)
- Process challenges:
  - Metal voiding during filling
  - Uniform via wall material deposition
  - Active IC surface connectivity
  - Wafer handling
- Performance challenges:
  - Available reliability data is limited
  - Thermal cycling
  - Electromigration
  - Si depletion at/around via
  - Shock/vibration

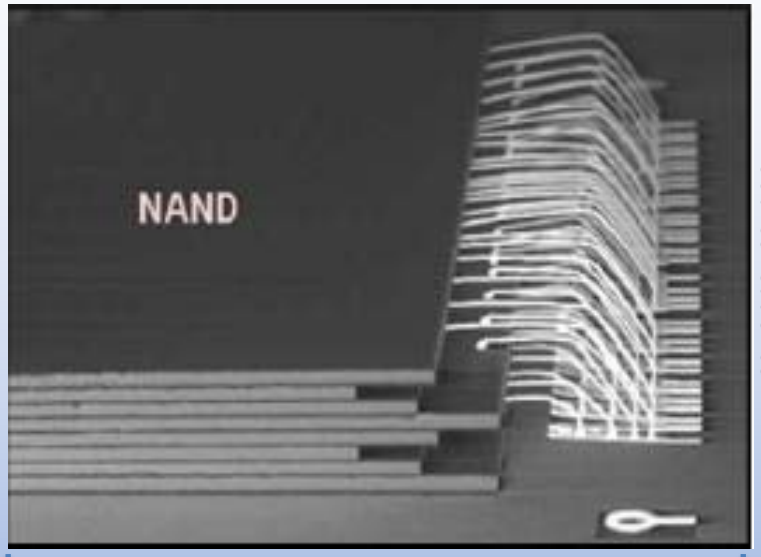


Source: CL Young 2011
web.mst.edu/~yshi/**3D_clock**__DAC11__2011-03-30-4DAC.pdf

Future of Technology

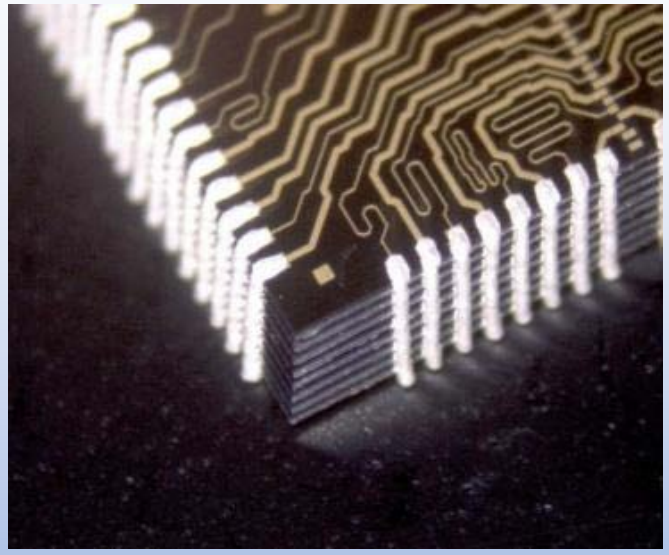
- A variety of 3D IC standards programs underway
  - Sematch and SEMI driving manufacturing standards
  - GSA, 3D SiG, and Si2 driving design standards
  - Also, JEDEC, IEEE, 3D-IC Alliance, and SRC
- 2015 Largest market share will likely be Logic and Memory SiP modules
  - (Source: Yole Development, GSA EDA Interest Group meeting, September 2010)
- Thinning and handling thin (~15 μm) thick die/wafer
- Via densities to 10^5/chip
- New materials for thermal management, via fill, and underfill
- Integrated and/or embedded passives
- Via in glass
- Heterogeneous integration (Sensor, processor, memory, communication SiP)

Coexisting with 3D TSV

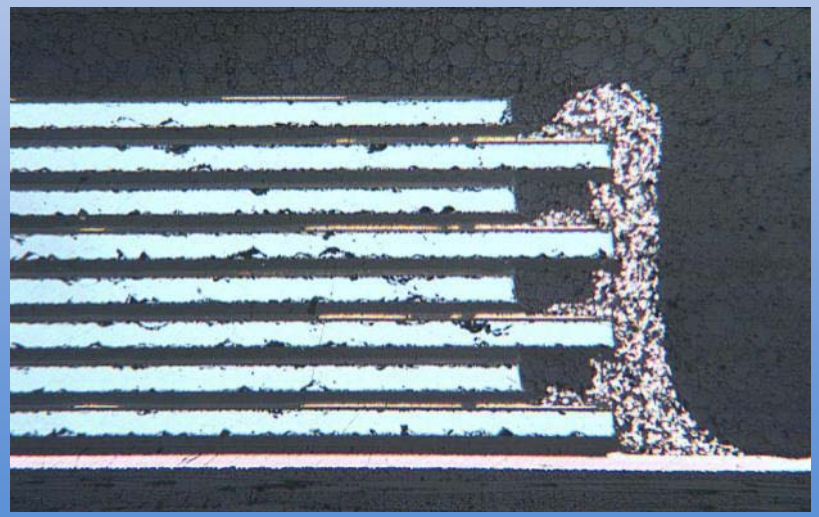


Source: Cadence

Wire bonding is the predominant 3D interconnect technology.



Vertical Circuits, Inc.'s Vertical Interconnect Pillar (VIP) technology interconnecting an 8 die memory stack



Source: Vertical Circuits, Inc.

Conclusions and Future Work

- TSV technology is going mainstream with large die partitioning, logic + memory, and stacked memory hitting the market.
- The applications are really performance driven. TSV just happens to provide the most cost effective solution to satisfy performance requirements.
- NASA engineers will want to use these devices (FPGA) in NASA environments (LEO and beyond) but the existing ground based reliability data is still limited.
- Testing standards are still being developed.
- Attending Semicon West 2012 in July.
- Will continue to drill down on potential reliability concerns, failure mechanisms, and avenues for risk mitigation.

Acknowledgements

- The investigators gratefully acknowledge the funding provided for this work by the NASA Electronic Parts and Packaging program under NASA WBS 724297.40.49.11
- The investigators wish to thank NEPP co-managers Mike Sampson and Ken LaBel for their support.
- The investigators also wish to recognize Drs. Charles “Chuck” Barnes, Doug Sheldon, Reza Ghaffarian, Rajeshuni “Ram” Ramesham, and Jong-ook Suh for their support, guidance, and valuable discussions.