HiREV NEPP Technical Interchange: "CMOS Physics of Failure Lifetime Modeling"

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The Aerospace Corporation

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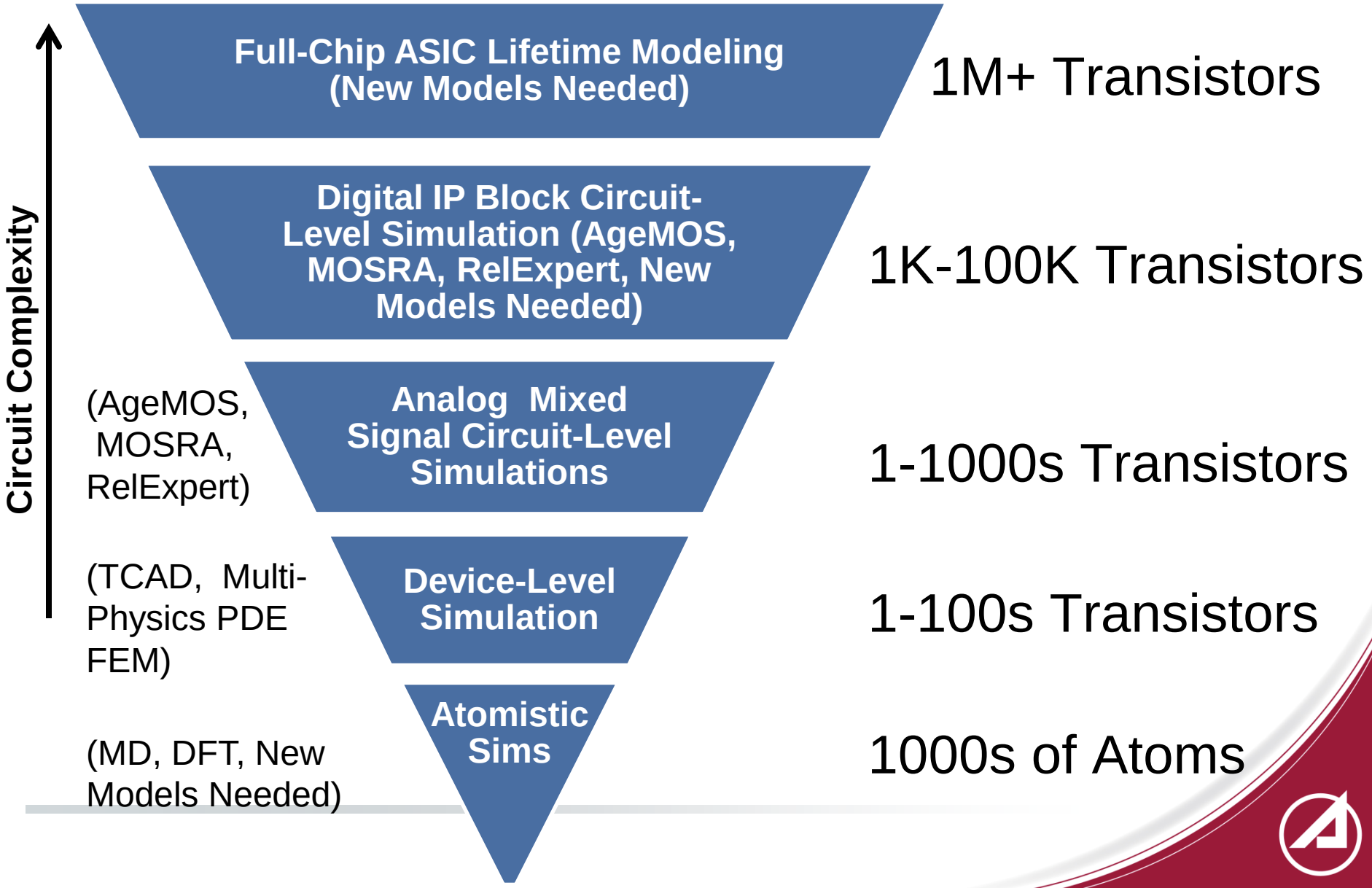
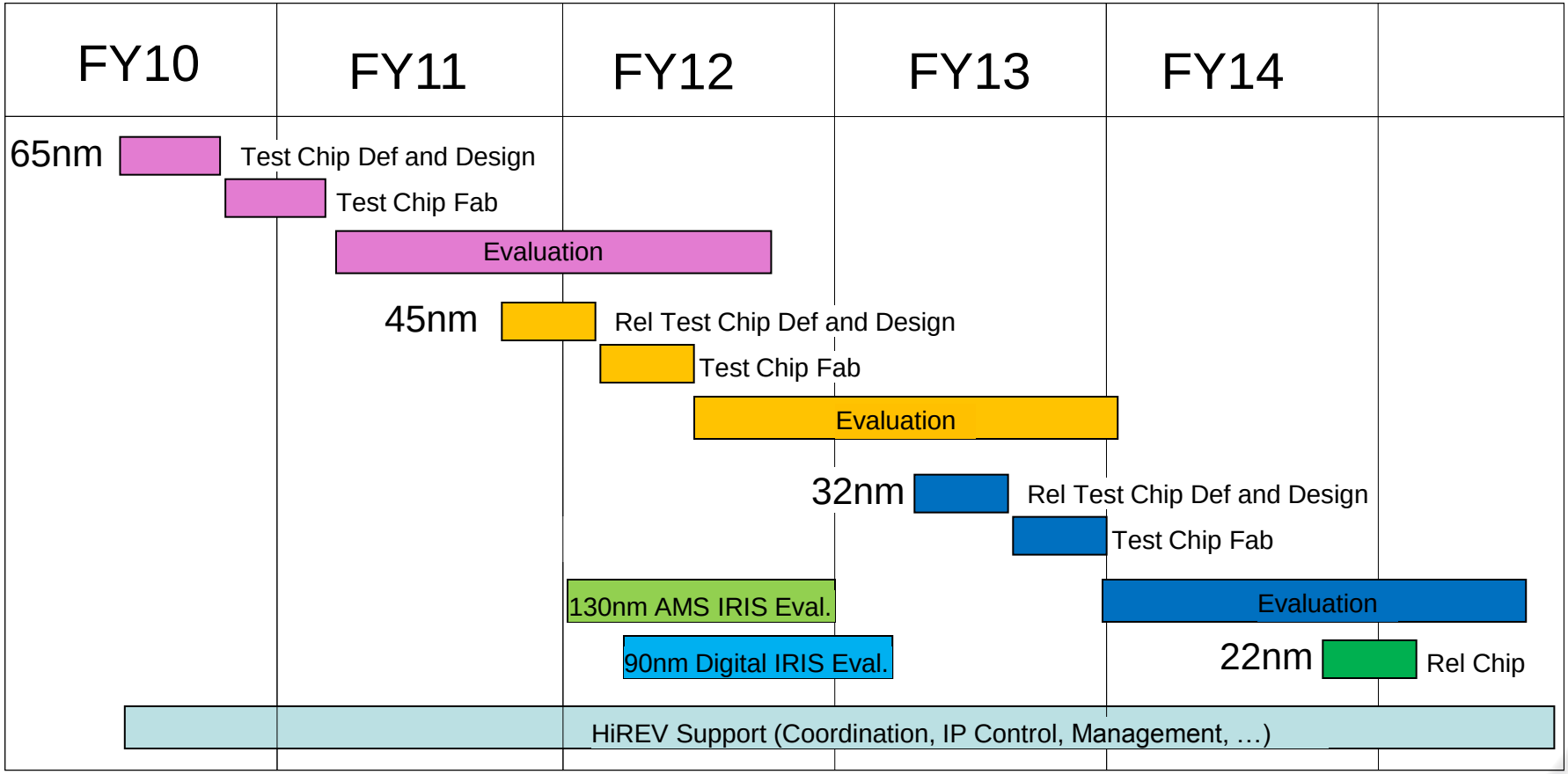
Topics of Discussion

- Multi-Level PoF Modeling & Simulation
- HiREV nano-CMOS Road-Map
- FY12 Lifetime Focus Areas
- CMOS Failure Modes Under Investigation
- Analog Mixed Signal Lifetime Simulation
- 90nm CMOS ASIC Full-Chip Lifetime Model
- Looking Forward

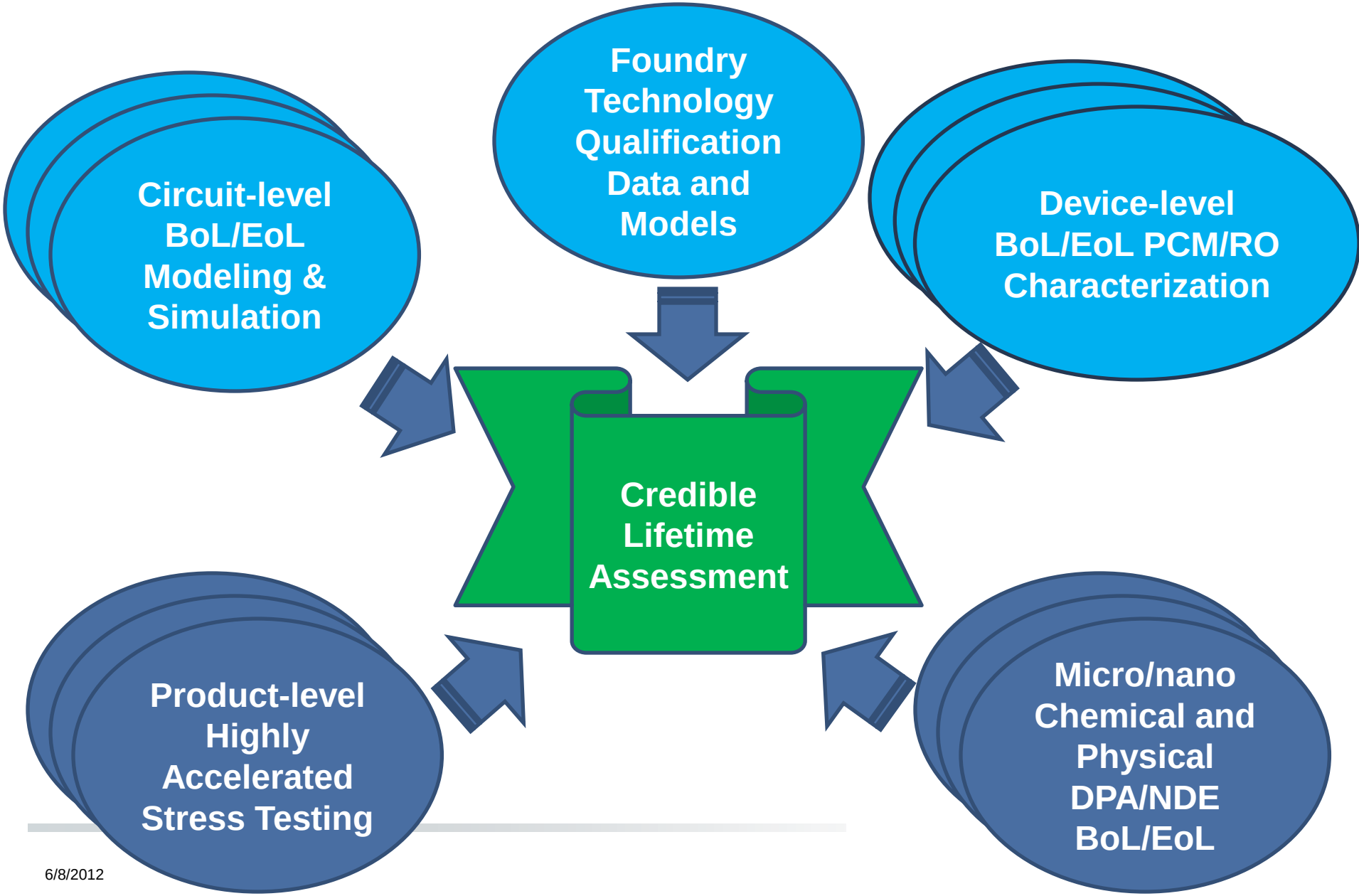
Multi-Level PoF Lifetime Modeling



HiREV FY12 nanoCMOS Roadmap



FY12 HiREV/Aerospace Focus Areas



CMOS Failure Modes Under Investigation

- Front-End-of-Line (FEOL)
  - *Hot Carrier Injection (**HCI**)*
  - *Negative Bias Temperature Instability (**NBTI**)*
  - *Stress Induced Leakage Current (SILC)*
  - *Gate Oxide Time Dependent Dielectric Breakdown (**GO-TDDB**)*
- Radiation Degradation
  - *Total Ionizing Dose (**TID**)*
  - *Rad/Rel **Synergistic Effects***
- Back-End-of-Line (BEOL)
  - *Electromigration (**EM**)*
  - *Stress Voiding (SV)*
  - *Contact & Via Opens*
  - *Inter-level Dielectric TDDB (ILD-TDDB)*
- Advanced Packaging
  - ***Ceramic Strength***
  - ***Interconnect Metallurgy***
  - ***Adhesive Polymers***

Atomistic simulation of HCI degradation in CMOS

FY12 Mid-Year Accomplishment

Goal: Apply atomistic simulation techniques to understand the generation and action of interface and boundary defects resulting from hot carrier injection (HCI) within the channel of CMOS transistors

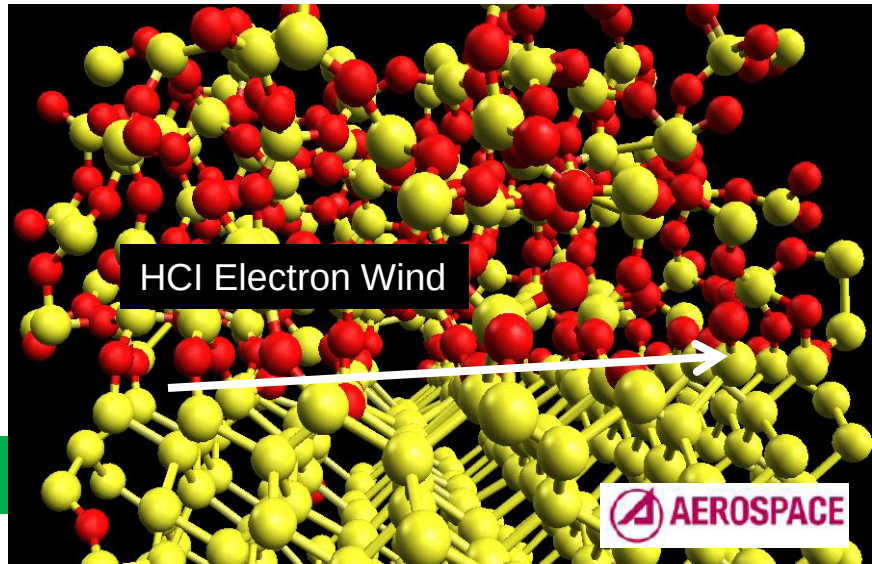
Methodology:

- Molecular dynamics (MD) of initial interface structure
- Density functional theory (DFT) electronic structure calculations for latent defects (e.g. strained bonds, Si-H, etc...)
- Quantum analysis of latent defect hot carrier capture cross section
- DFT-MD simulations of atomic relaxations following carrier capture
- MD simulations of large scale oxide relaxation
- Analysis of defect trapping/charging for end-to-end degradation predictions

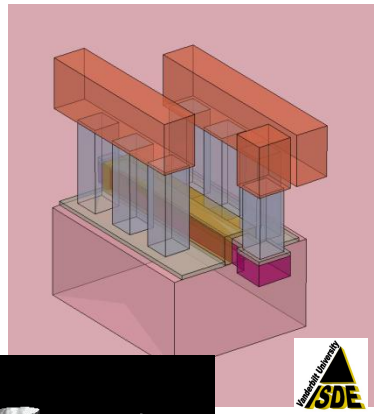
Current Status:

- CMOS, 2 nm thick gate oxide, polySi gate
- Amorphous gate oxide generated using MD
- Plane wave DFT calculations of defects

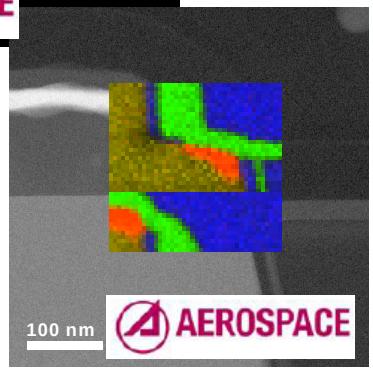
Need MD/DFT Model for Each Failure Mode



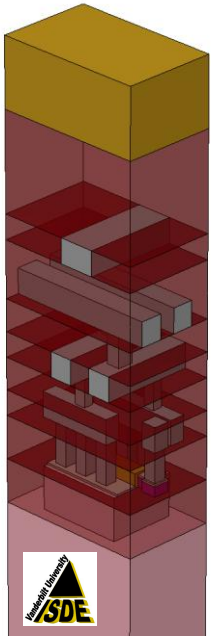
FY11 HiREV Vanderbilt University Collaboration, nano-scale 3D Imaging → TCAD → SEE Response

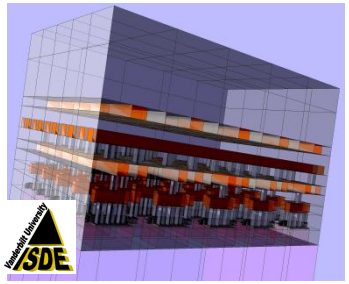


Aerospace 3D Device and Materials Map



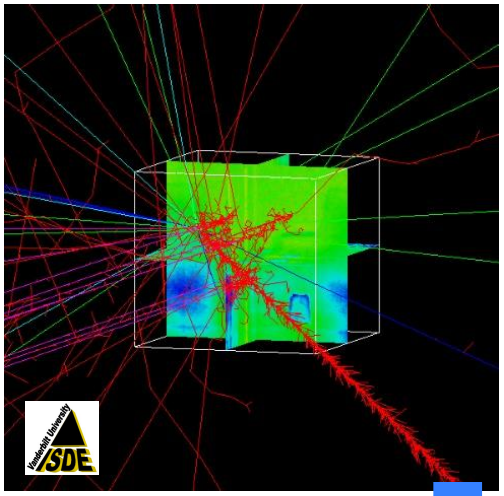
3D TCAD Model Created for MRED

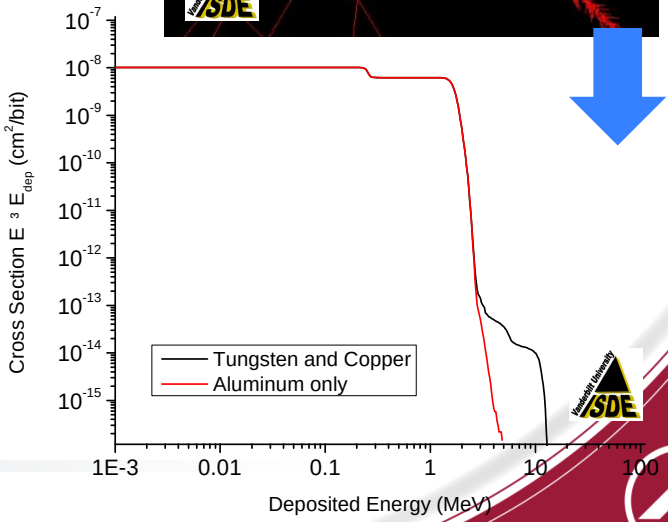




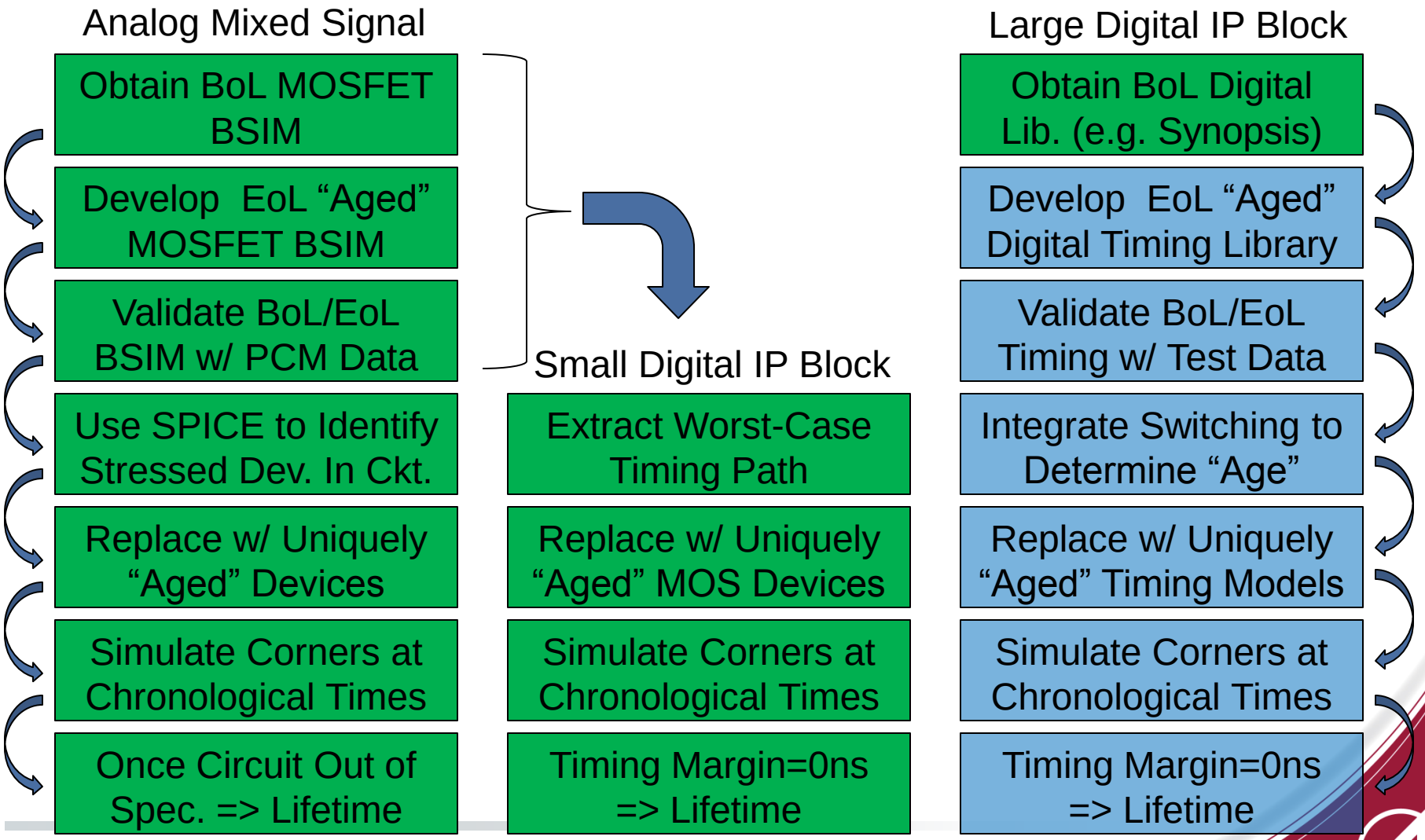
Increase Error Rate for High Qcrit Logic

Simulate Single Event Energy Deposition for Al vs. W





"Bottoms-Up" MOSFET Device, Analog Mixed Signal and Digital Circuit Aging Process



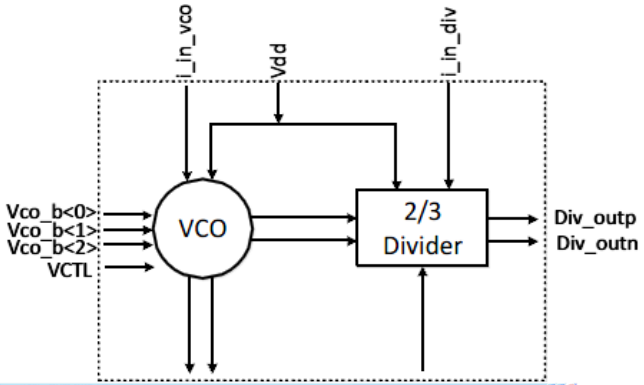
BSIM: Berkeley SPICE IGFET Model

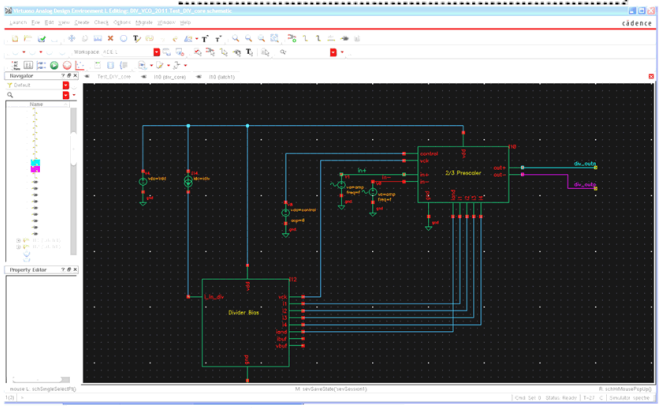
130nm Device Aging Simulation Methodology

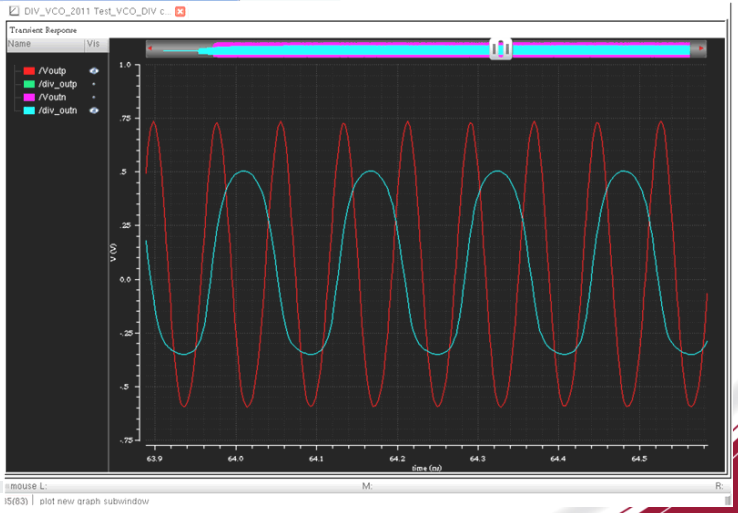
- Develop a device aging calculation for each reliability wear out mechanism based on the physical understanding of the mechanism, data and models available from foundry, literature, and our experimental data
- Review the operating conditions of each transistor in the circuit to identify those that are expected to suffer degradation due to NBTI, HCI, and TDDB
- Project changes in the BSIM (Berkeley Short-channel IGFET Model) models used for these selected transistors at 10, 20 and 40 years to simulate the effects of aging on the circuit
- Compare Beginning of Life (BoL) Simulations with “aged” End Life (EoL) models to simulate degraded circuit performance that illustrates the aging effect

Ex: Analog Mixed Signal Circui VCO / Divider Aging

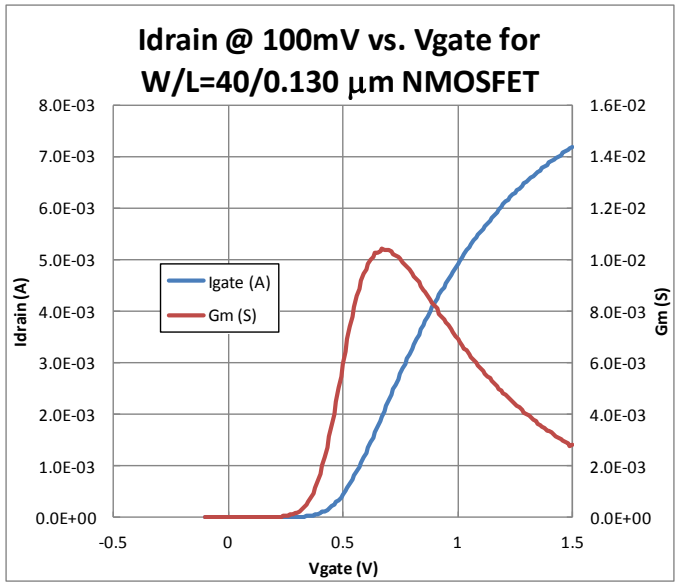
- Inputs
  - *Vdd = 1.5V*
  - *3 Bit Programmable VCO Frequency tuning (8GHz)*
  - *Analog input for Fine Tuning*
  - *Control Bit Selects Divide by 2 or 3*
  - *VCO Current Reference*
  - *Divider Current Reference*
- Output
  - *VCO Differential Output*
  - *Divider Differential Output*



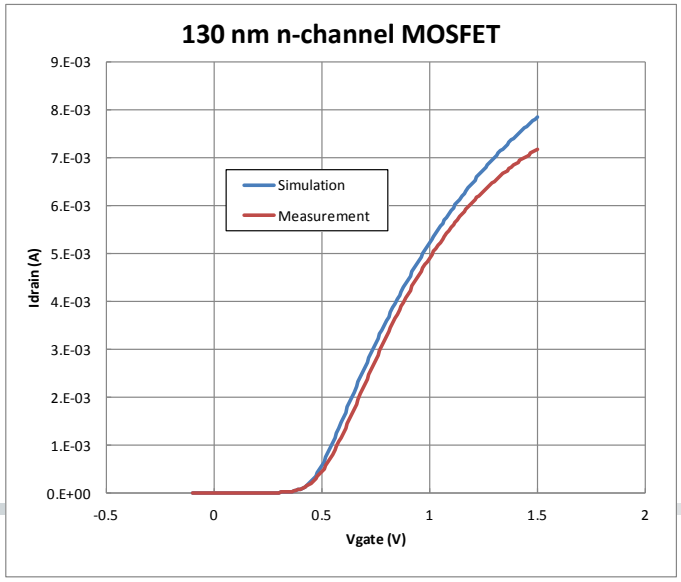


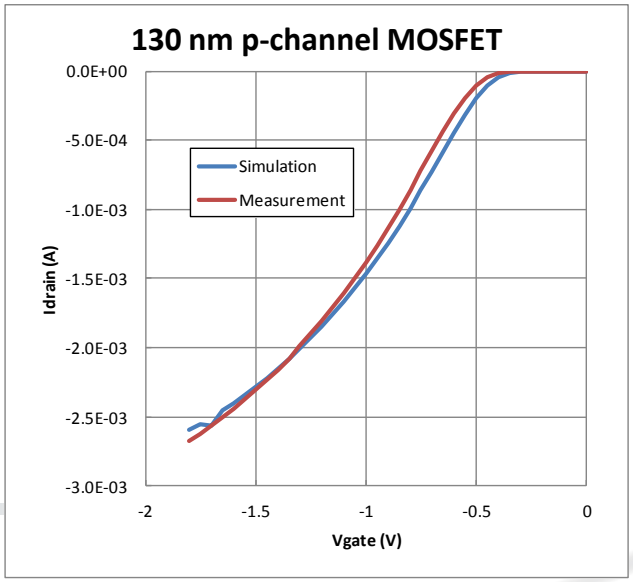


Characterization of 130 nm 8rf Models
Measurement v. Simulation for BoL NMOS and PMOS



- In this example the V_{th} is 0.432 V, G_{mmax} is 10.4 mS
- BSIM 3f5 Level 8 Foundry BoL Model





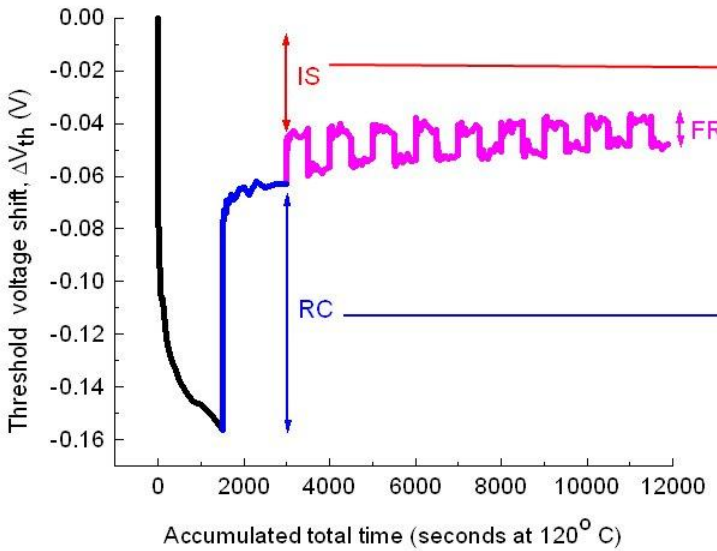
Ex: Operating Point of 130-nm MOSFETs in Circuit

							DC				AC (peak to peak values)				
FET Number	Circuit	Type	W	L	nf	m	Vs	Vg	Vd	Id(mA)	Vs	Vg	Vd	Id(mA)	Freq (GHz)
1	VCO_10GHz Ibias	pfet_rf	20	0.25	5	1	1.5	0.89	0.89	0.35	0	0	0	0	0
2	VCO_10GHz Ibias	pfet_rf	500	0.25	125	1	1.5	0.888	0.7714	8.695	0	0	0	0	0
3	VCO_10GHz Ibias	pfet_rf	38.5	0.25	10	1	1.5	0.89	0.522	0.7185	0	0	0	0	0
4	VCO_10GHz Ibias	pfet_rf	120	0.12	10	1	1.5	1.005	1.005	0.7986	0	0	0	0	0
5	VCO_10GHz Ibias	pfet_rf	120	0.12	10	1	1.5	1.005	1.005	0.7986	0	0	0	0	0
6	VCO_10GHz Ibias	nfet_rf	16	0.4	4	1	0	0.5521	0.522	0.2341	0	0	0	0	0
7	VCO_10GHz Ibias	nfet_rf	16	0.4	4	1	0	0.5521	1.005	0.7986	0	0	0	0	0
8	VCO_10GHz Ibias	nfet_rf	860	0.4	215	1	0	0.5521	0.09374	21.41	0	0	0	0	0
9	VCO_10GHz Ibias	nfet_rf	16	0.4	4	1	0	0.5521	1.005	0.7986	0	0	0	0	0
10	VCO_10GHz Ibias	nfet_rf	540	0.4	135	1	0	0.5521	0.117	15.86	0	0	0	0	0
11	VCO_10GHz_ControlBits	pfet	2	0.12	1	1	1.5	0	1.5	0	0	0	0	0	0
12	VCO_10GHz_ControlBits	pfet	2	0.12	1	1	1.5	1.5	0	0	0	0	0	0	0
13	VCO_10GHz_ControlBits	pfet	2	0.12	1	1	1.5	1.5	0	0	0	0	0	0	0
14	VCO_10GHz_ControlBits	pfet	2	0.12	1	1	1.5	1.5	0	0	0	0	0	0	0
15	VCO_10GHz_ControlBits	pfet	2	0.12	1	1	1.5	1.5	0	0	0	0	0	0	0
16	VCO_10GHz_ControlBits	pfet	2	0.12	1	1	1.5	1.5	0	0	0	0	0	0	0
17	VCO_10GHz_ControlBits	pfet	2	0.12	1	1	1.5	1.5	0	0	0	0	0	0	0
18	VCO_10GHz_ControlBits	nfet_inh	1	0.12	1	1	0	0	1.5	0	0	0	0	0	0
19	VCO_10GHz_ControlBits	nfet_inh	1	0.12	1	1	0	1.5	0	0	0	0	0	0	0
20	VCO_10GHz_ControlBits	nfet_inh	1	0.12	1	1	0	1.5	0	0	0	0	0	0	0
21	VCO_10GHz_ControlBits	nfet_inh	1	0.12	1	1	0	1.5	0	0	0	0	0	0	0
22	VCO_10GHz_ControlBits	nfet_inh	1	0.12	1	1	0	1.5	0	0	0	0	0	0	0
23	VCO_10GHz_ControlBits	nfet_inh	1	0.12	1	1	0	1.5	0	0	0	0	0	0	0
24	VCO_10GHz_ControlBits	nfet_inh	1	0.12	1	1	0	1.5	0	0	0	0	0	0	0
25	VCO_Core	nfet_rf	24	0.12	6	1	0	0.77	0.77	4.347	0	1.5	1.5	12.5	12.75
26	VCO_Core	nfet_rf	24	0.12	6	1	0	0.77	0.77	4.347	0	1.5	1.5	12.5	12.75
27	VCO_MIM_Bank	nfet_rf	8	0.12	2	1	1.5	0	1.5	0	0	0	0	0	0
28	VCO_MIM_Bank	nfet_rf	8	0.12	2	1	1.5	0	1.5	0	0	0	0	0	0
29	VCO_MIM_Bank	nfet_rf	8	0.12	2	1	1.5	0	1.5	0	0	0	0	0	0
30	VCO_MIM_Bank	nfet_rf	8	0.12	2	1	0	1.5	0	0	0	0	0	0	0
31	VCO_MIM_Bank	nfet_rf	8	0.12	2	1	1.5	0	1.5	0	0	0	0	0	0
32	VCO_MIM_Bank	nfet_rf	8	0.12	2	1	1.5	0	1.5	0	0	0	0	0	0
33	VCO_MIM_Bank	nfet_rf	8	0.12	2	1	1.5	0	1.5	0	0	0	0	0	0
34	VCO_Prebuf	nfet_rf	32	0.12	32	1	0.1177	1.005	0.996	7.928	0	1	0.6	18	12.75
35	VCO_Buf	nfet_rf	40	0.12	32	1	0.09374	1.005	0.9438	10.71	1	0.4	1.5	4	12.75
36	DIV_Bias	nfet_rf	40	0.25	10	1	0	0.3396	0.3396	0.2	0	0	0	0	0
37	DIV_Bias	nfet_rf	200	0.25	50	1	0	0.3396	0.473	1.128	0	0	0	0	0
38	DIV_Bias	nfet_rf	400	0.25	100	1	0	0.3396	0.2095	1.905	0	0	0	0	0
39	DIV_Bias	nfet_rf	400	0.25	100	1	0	0.3396	0.2027	1.894	0	0	0	0	0
40	DIV_Bias	nfet_rf	400	0.25	100	1	0	0.3396	0.1973	1.885	0	0	0	0	0
41	DIV_Bias	nfet_rf	400	0.25	100	1	0	0.3396	0.1925	1.877	0	0	0	0	0
42	DIV_Bias	nfet_rf	28	0.25	7	1	0	0.3396	0.698	0.1686	0	0	0	0	0

NBTI Risk

HCI Risks

Current Activity: CMOS-Based Physics of Failure - NBTI



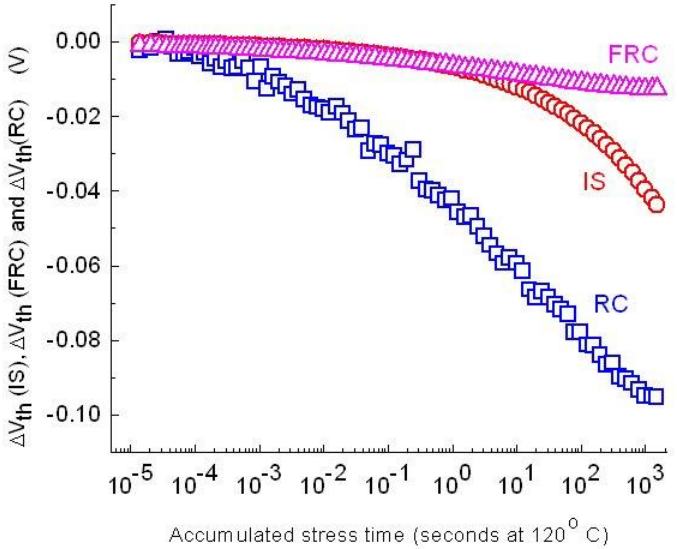
Breaking of Si-H bonds creating positive interface states

Hole traps in the oxide which require positive field to detrap/neutralize.

Hole trapping in the oxide by preexisting defects detrap when field drops to zero

IBM 130 nm bulk technology
Nitrided SiO_2 gate dielectric

V_{gs}=-3.25 volts for 0<t<1500 s
V_{gs}= 0.00 volts for 1500<t<3000 s
V_{gs}= 1.50 for 3000<t<3500 s
V_{gs}=-1.00 for 3500<t<4000 s
Etc



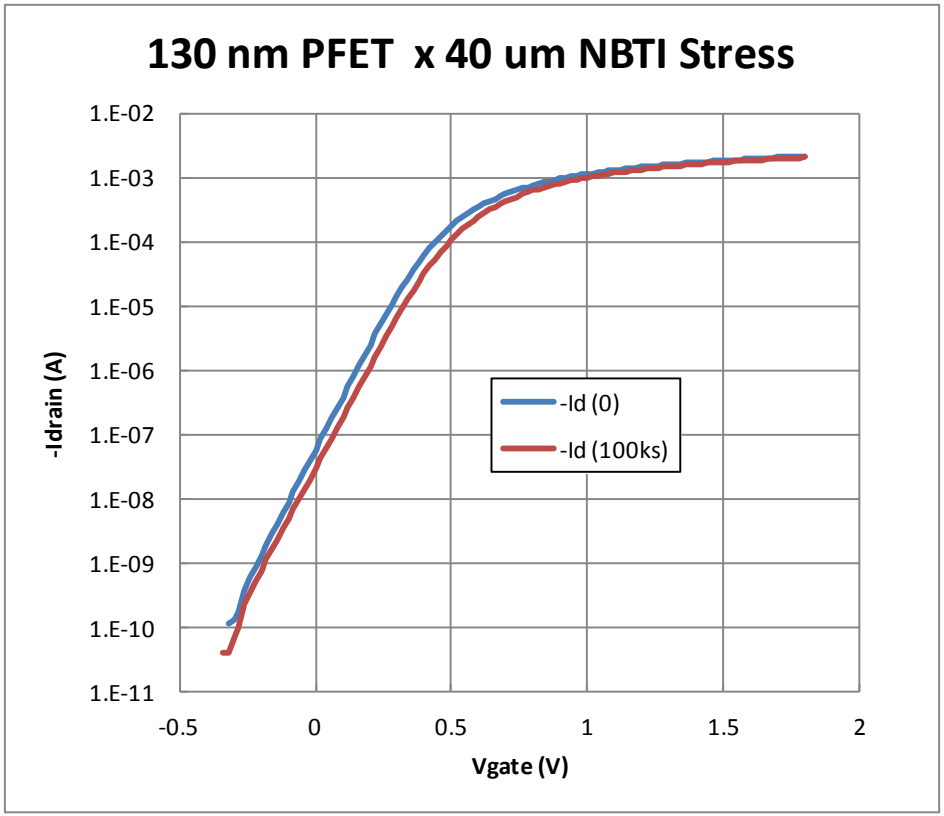
Constant stress V_{gs}= -3.25 volts

Point of Contact: Rod Devine (505)-846-4822
roderick.devine.ctr@Kirtland.af.mil

To appear in the Proceedings of
2012 ICDIM [Physica Status Solidi]

Question: Does this extend beyond 90nm?

130nm NBTI Stress Measurement

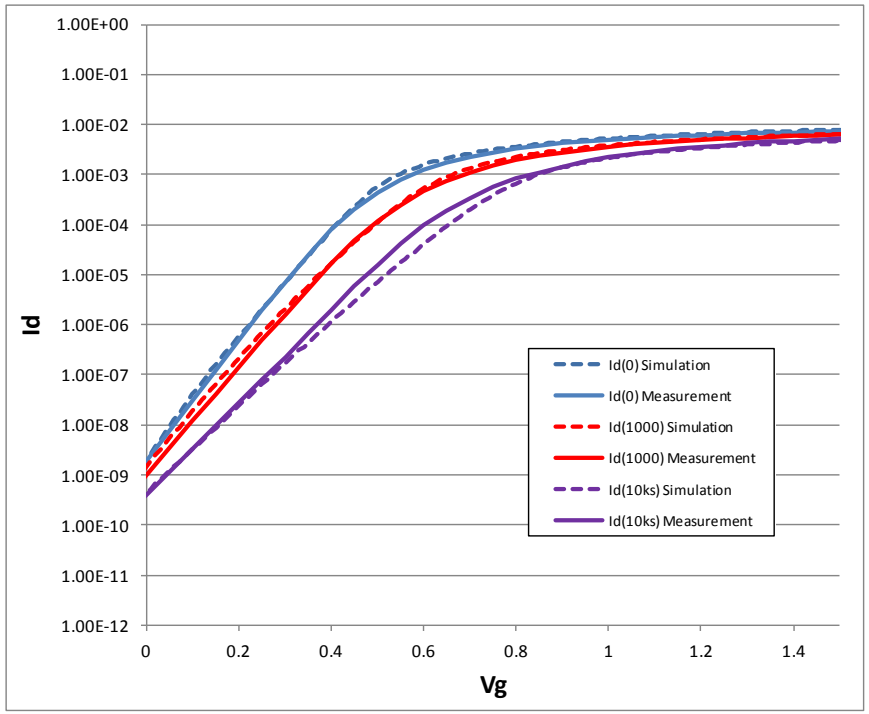


- Device stressed at V_{gate} = -2.3 V at a temperature of 140 C
- Very little degradation observed even at 100 ks
- Initial BSIM model matches the initial measurement as well as it matches the post-stress measurement
- The 130nm 8rf PFET is insensitive to NBTI under these circuit conditions

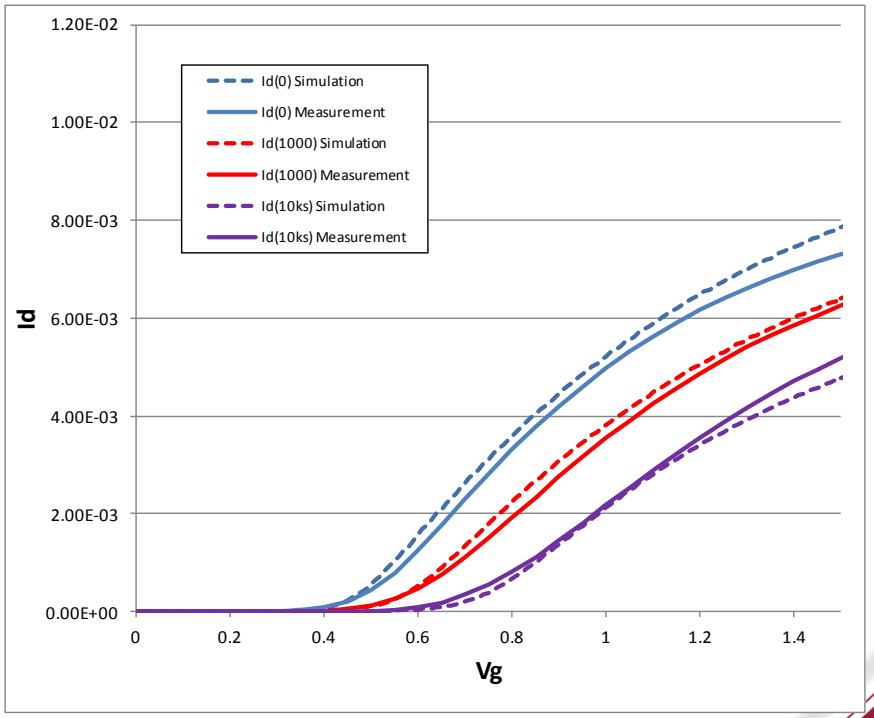
HCI Aged 130nm 8RF NFET Model Validation

- HC Stress data for V_d=2.5 V and V_g=1.25 V
- BSIM4 Models were matched to measured devices by parametric shifts in model parameters CIT, VTH, and Uo
  - *The threshold voltage increases with HCI stress due to charge trapping*
  - *Decreases in transconductance with aging were represented by a decrease in mobility resulting also from an increase in interface traps*
  - *The sub-threshold slope decreases with an increase in interface state density (CIT)*
- Results show good model correlation with this approach

40um x 0.12um NFET Id-Vg (Log plot)



40um x 0.12um NFET Id-Vg (Linear plot)



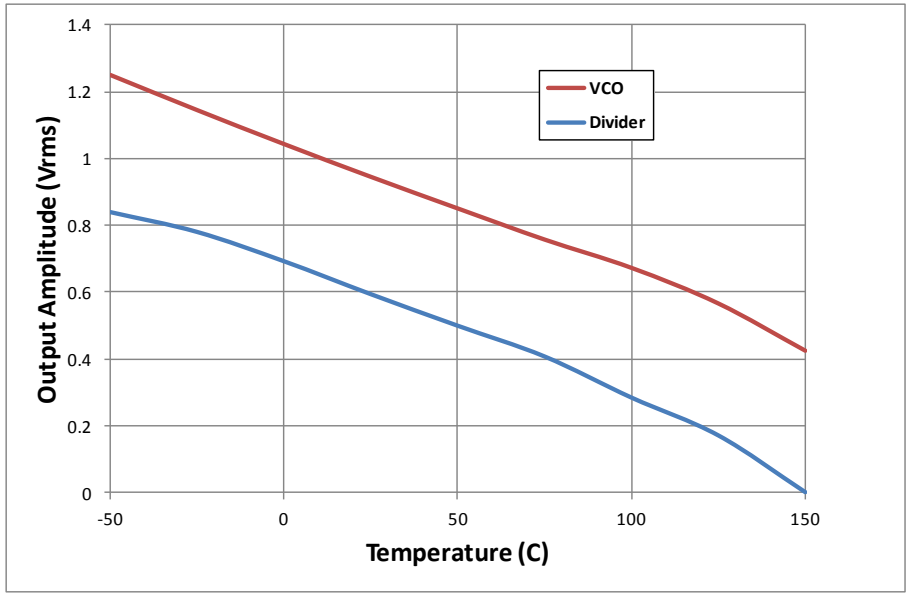
Modeling the lifetime for a particular circuit design, requires knowledge about the devices from that process lot and detailed simulation

HCI/NBTI Aging Simulation Process

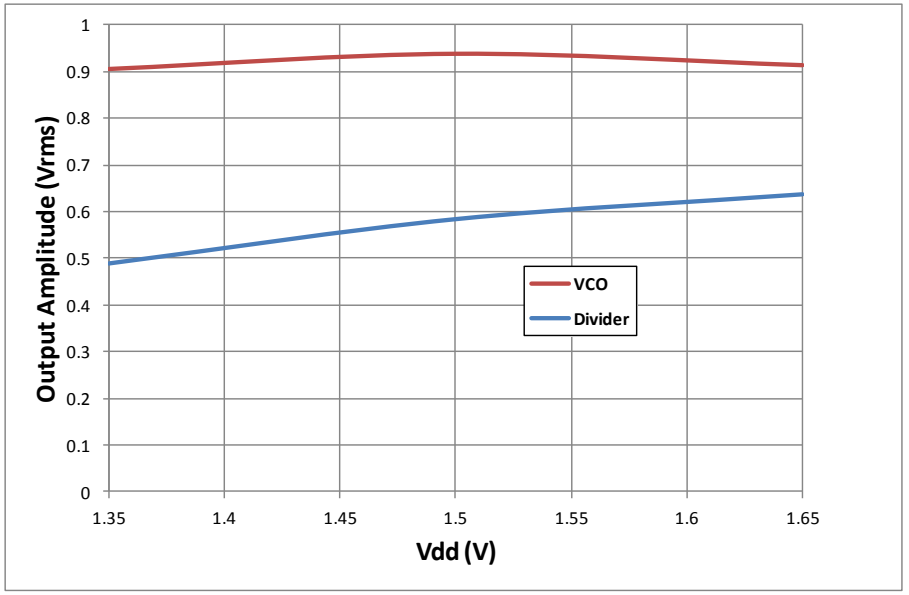
- Establish BoL Circuit Sensitivities to Voltage, Temperature and Process
- Each transistor in the VCO/ Divider Circuit was assigned a separate BSIM4 model instance.
- Variables were added to each BSIM4 model to account for parametric shifts from HCI/ NBTI stress. The variables are contained in a separate “age” file that can be efficiently updated when new calculations are available.
- Parametric Shift variables included in the model are:
  - *Mobility (U0)*
  - *Threshold Voltage(VTH0)*
  - *Interface Trap Capacitance (CIT)*
- The “aged” models were validated by comparing simulated NFET Id-Vg curve traces to measurements taken from actual aged devices.
- AC and DC bias conditions for each transistor in the circuit were tabulated and used to calculate HCI/NBTI stress and parameter shifts at 0, 10, 20 and 40 years .
- Circuit was run with updated parametric shift variables

VCO / Divider Sensitivities

Temperature Sensitivity



Bias Sensitivity

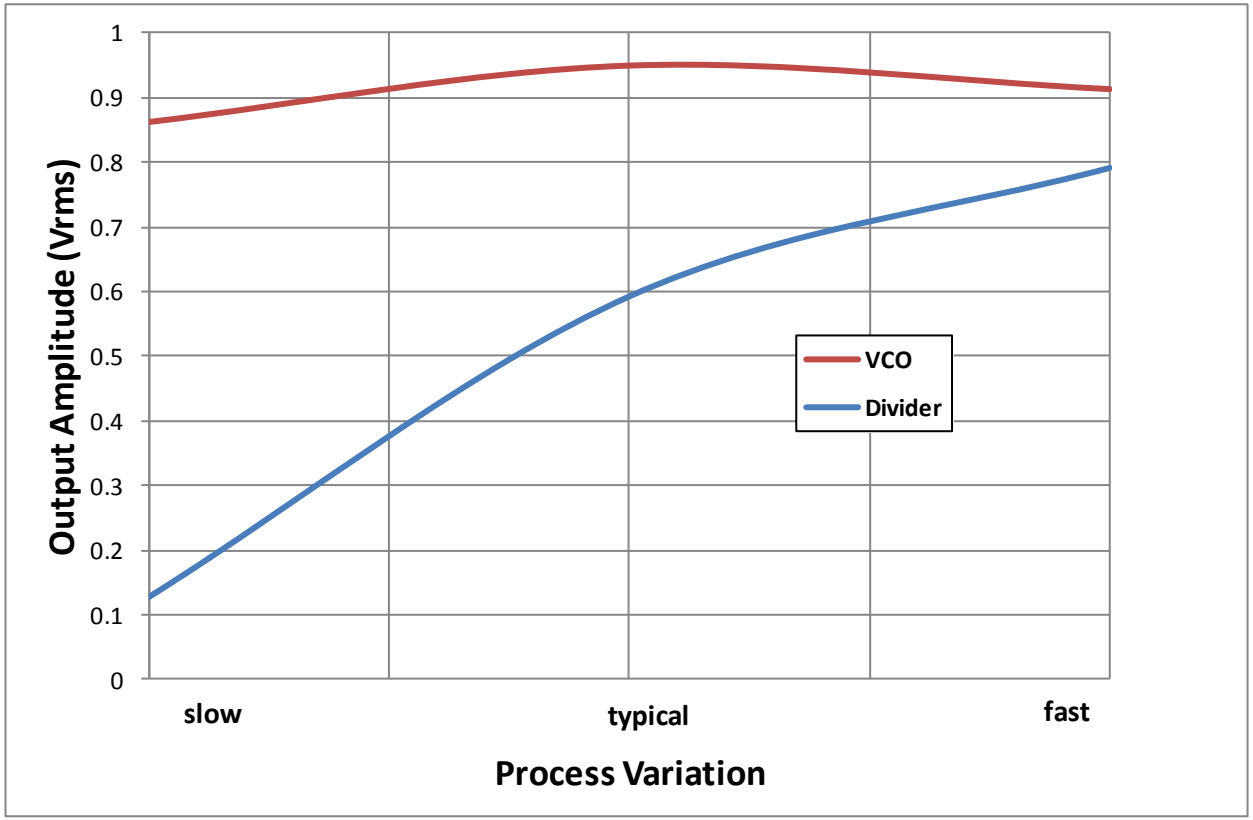


The slope of the curve is 3.7mV/°C. To remain within the min/max data sheet specifications for output amplitude, the VCO/Divider would be restricted to an 8°C temperature range.

The Divider output varies by 0.5mV /1mV Vdd. To remain within the min/max data sheet specifications for output amplitude, Vdd would be restricted to +/- 40mV.

Simulated at BOL, 27C, and nominal process

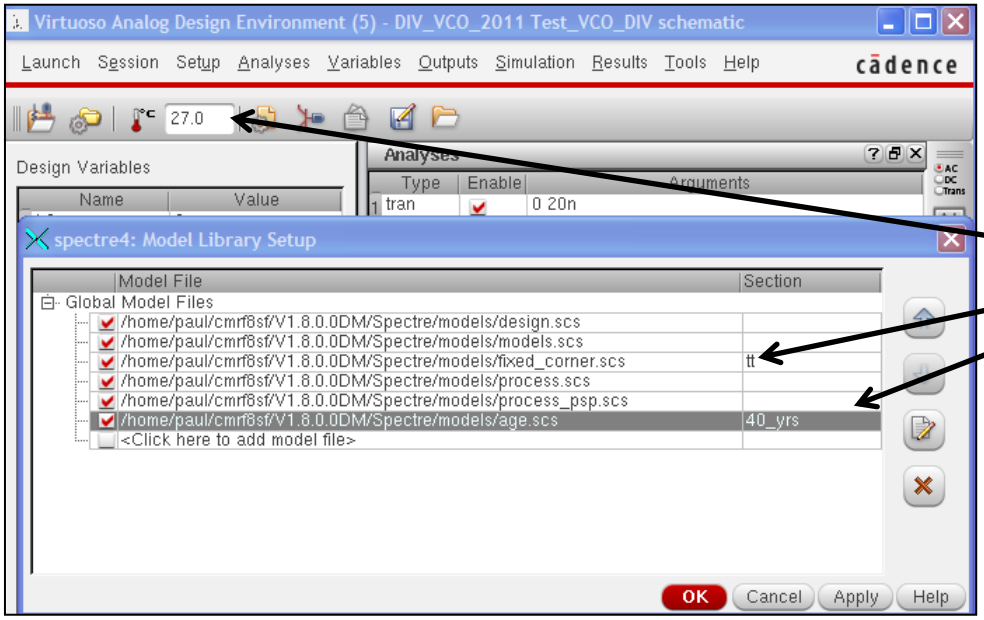
VCO / Divider Process Sensitivity



The Divider output varies by 660mV. To remain within the min/max data sheet specifications for output amplitude, the VCO/Divider would be restricted to within 6% of the process center.

Simulated at BOL, 27C, and nominal bias and process

HCI/NBTI Aging Simulation Automation



Circuit age, temperature and process parameters can be selected from a pulldown menu

```
section 40_yrs
parameters
+ vth_age_25 = 0.4
+ vth_age_26 = 0.4
+ u0_age_25 = -28
+ u0_age_26 = -28
+ int25          = 0.03
+ int26          = 0.03
endsection 40_yrs
```

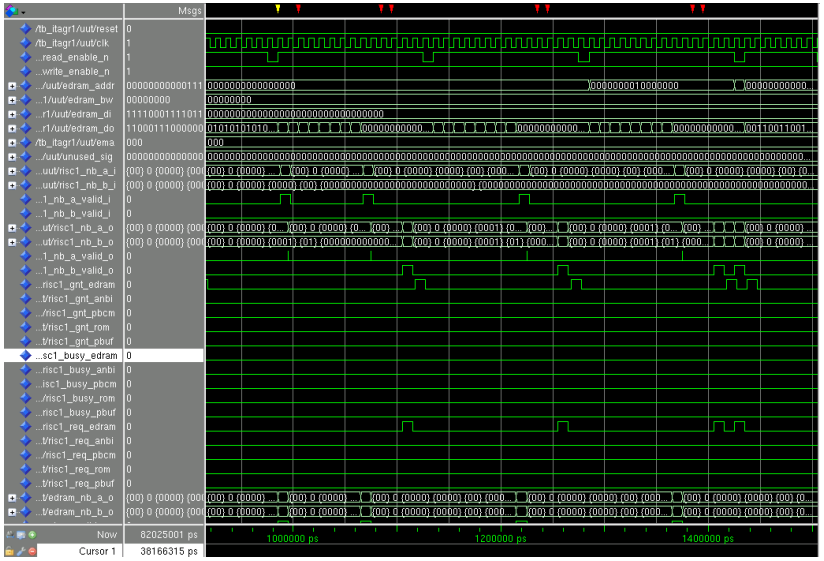
Sample age model file with Vth, U0 and CIT parameter shifts for transistors 25 and 26

130-nm AMS Sims Summary

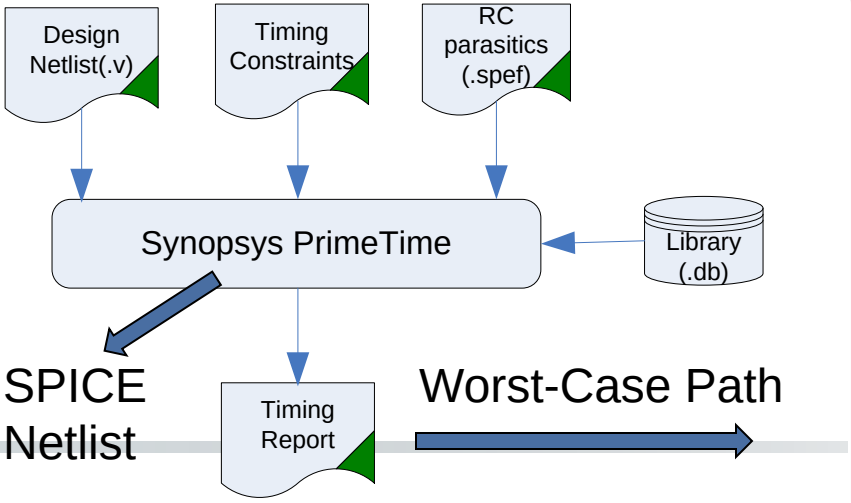
- The output amplitudes of the VCO and Divider are sensitive to shifts in temperature, process and voltage
- The time to failure depends on the use conditions and definition of failure
- The process for simulating the 130nm circuit after aging is operating efficiently and providing good correlation to measured data
  - *Performed simulations for 0, 10, 20, 40 years under worst-case bias/temperature conditions*
- Next Steps Include:
  - *Characterize phase noise as a function of age*
  - *Provide Bias/Temperature Recommendation for Life Testing Activity*
  - *Repeat for 90-nm 9SF AMS and 90/65-nm Digital Only Designs*

90nm Digital ASIC Circuit Aging Status

Functional Logic Simulation



- Received 90nm design database
- Full circuit logic simulation(s) performed
- Primetime Static Timing Analysis Done
- Primetime Si SPICE Netlist extraction of worst-case path(s) complete
- HSPICE Simulation of timing paths begun
- 90nm Aged MOS models under development




```
clock sysclk (rise edge)                                  7.19000    7.19000
clock source latency                                      0.00000    7.19000
PAD_clk (in)                                              0.00000 &  7.19000 r
PAD_clk (net)                                   1
clk_pad/PAD (SS_INBUF)                                    0.00003 &  7.19003 r
clk_pad/O1 (SS_INBUF)                                     0.57724 &  7.76727 r
clk (net)                                       1
clk__L1_I0/in0 (inv_30x)                                  0.01825 &  7.78552 r
clk__L1_I0/y (inv_30x)                                    0.25742 &  8.04294 f
clk__L1_N0 (net)                               13
clk__L2_I2/in0 (inv_30x)                                  0.00822 &  8.05117 f
clk__L2_I2/y (inv_30x)                                    0.23654 &  8.28770 r
clk__L2_N2 (net)                               22
clk__L3_I55/in0 (buf_18x)                                 0.05380 &  8.34150 r
clk__L3_I55/y (buf_18x)                                   0.25680 &  8.59830 r
clk__L3_N55 (net)                              30
core/clk__L3_N55 (itagr1)                                 0.00000 &  8.59830 r
core/clk__L3_N55 (net)
core/nb_risc1_i_24_ram0/CLKA (SRAM_DP_256_69)             0.01017 &  8.60847 r
library setup time                                       -0.74201    7.86646
data required time                                                   7.86646
-------------------------------------------------------------------------------
data required time                                                   7.86646
data arrival time                                                   -7.78522
-------------------------------------------------------------------------------
slack (MET)                                                          0.08124
```

Next Step: Physics of Failure - Based Circuit Modeling

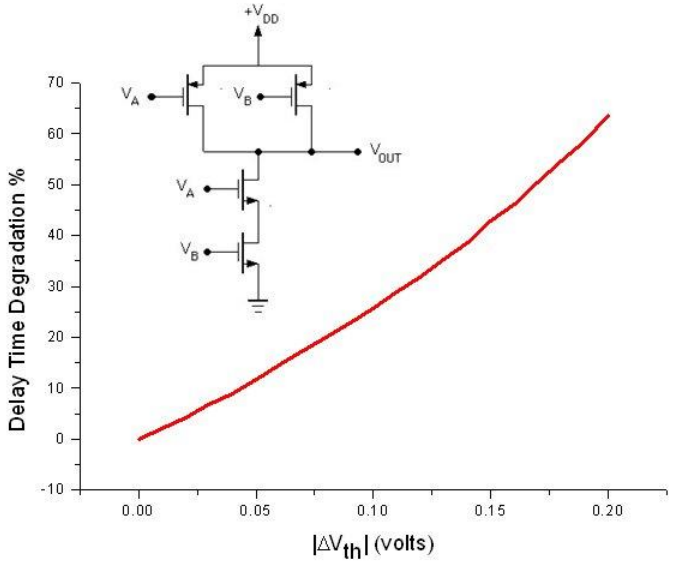
- Done using Xyce™ developed at Sandia National Lab
- Designed for large-scale problems
- Potential access to source code
- Access to local expertise
- Xyce has radiation modeling, which could be obtained in the future.

Future Work

PoF based development of $V_{th}(t)$

- Experimental dependence on bias, T, duty cycle and frequency must be developed and then extrapolated to years.

Single NAND gate with a 1fF load



Multiple NAND gates

Initial Circuit Testing Done on a Ring Oscillator

- 50% duty cycle is ideal
- Common circuit
- 11 NAND gates using the 65 nm PTM models
- Base frequency of 3.5 GHz
- For ΔV_{th}=-0.1 volts the frequency drops by 15%

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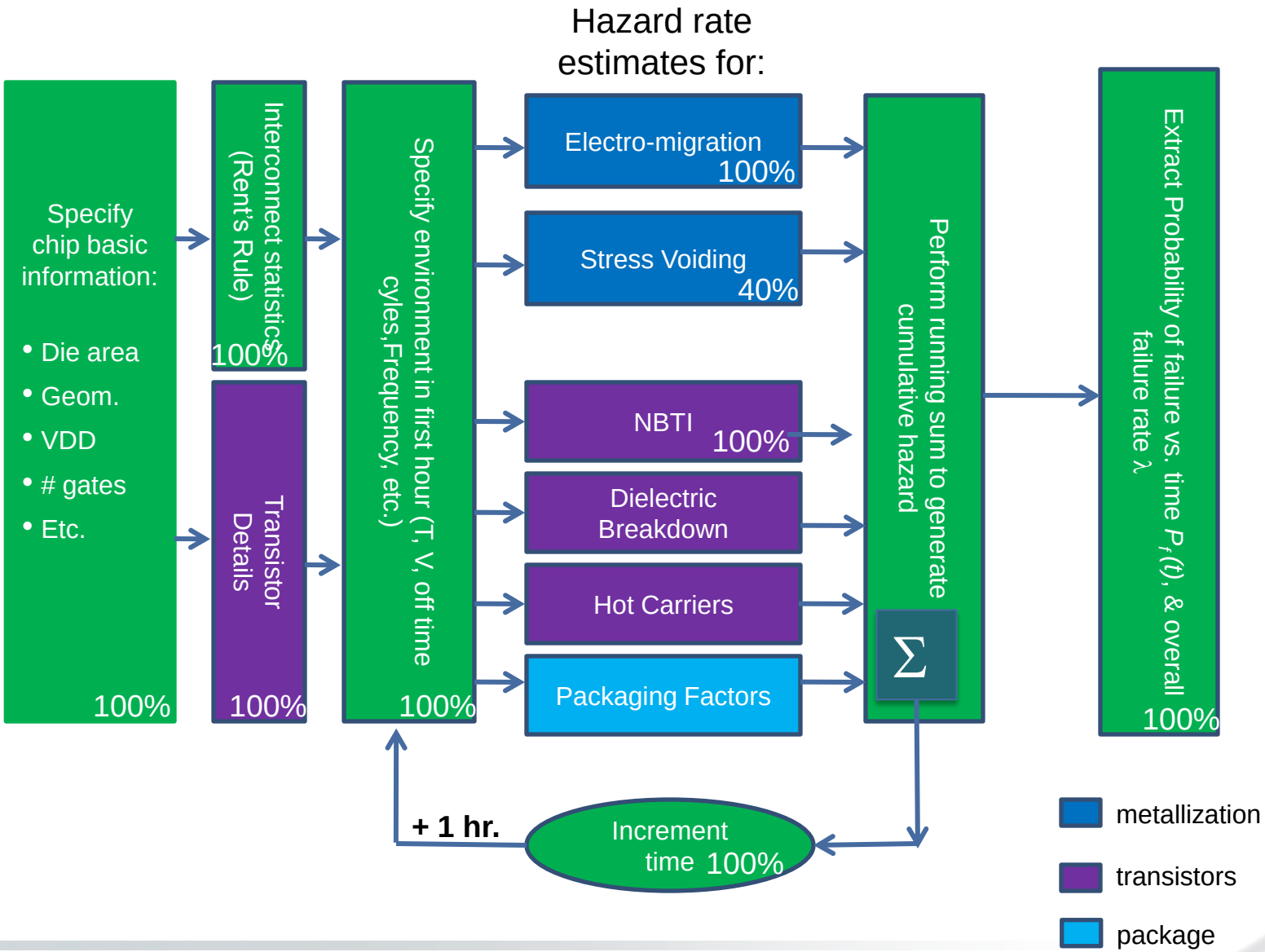
kenneth.kambour.ctr@Kirtland.af.mil

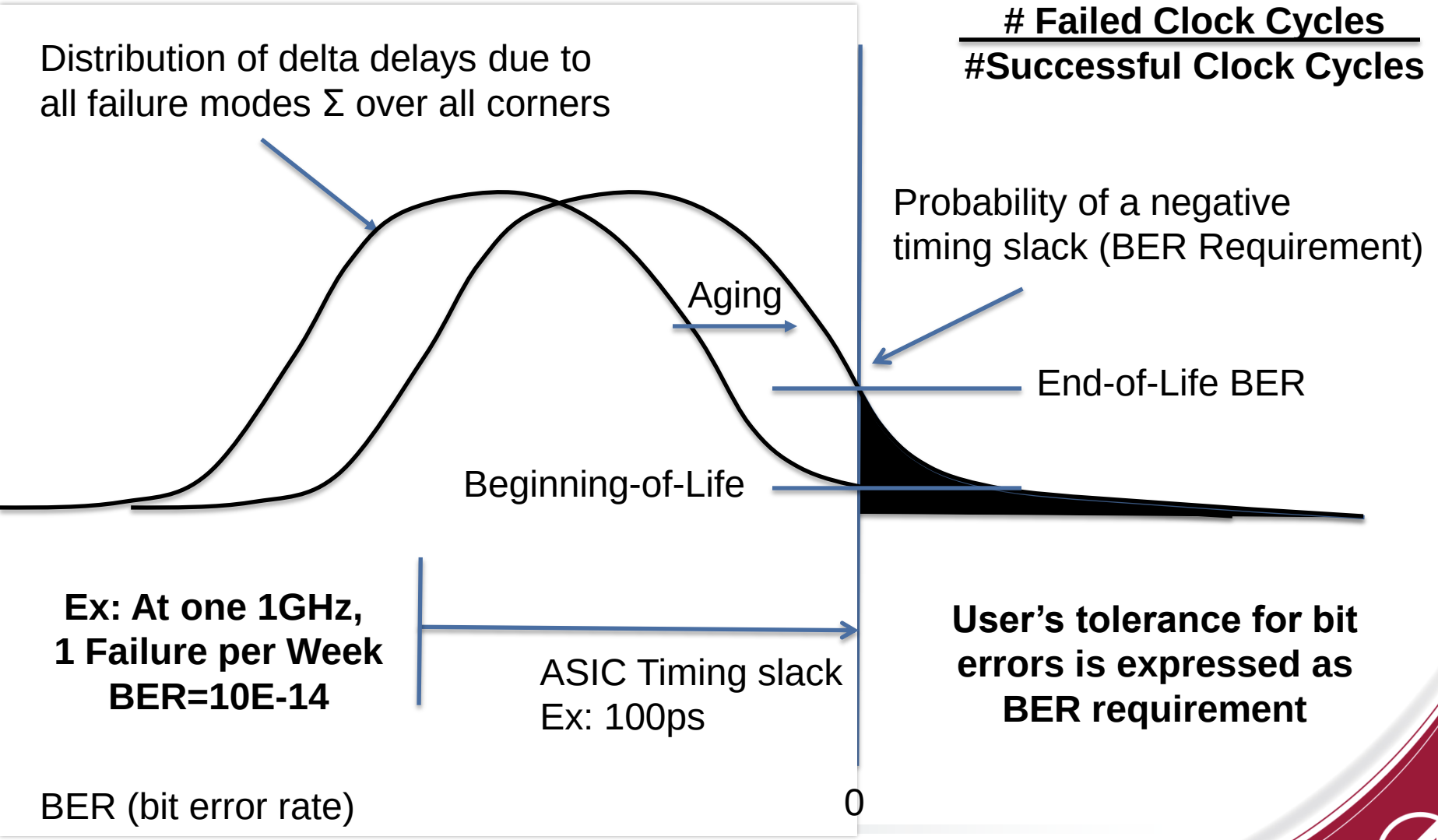
Presented at MRQW Dec. 2011

Full Chip 90nm CMOS ASIC Reliability Modeling Tool



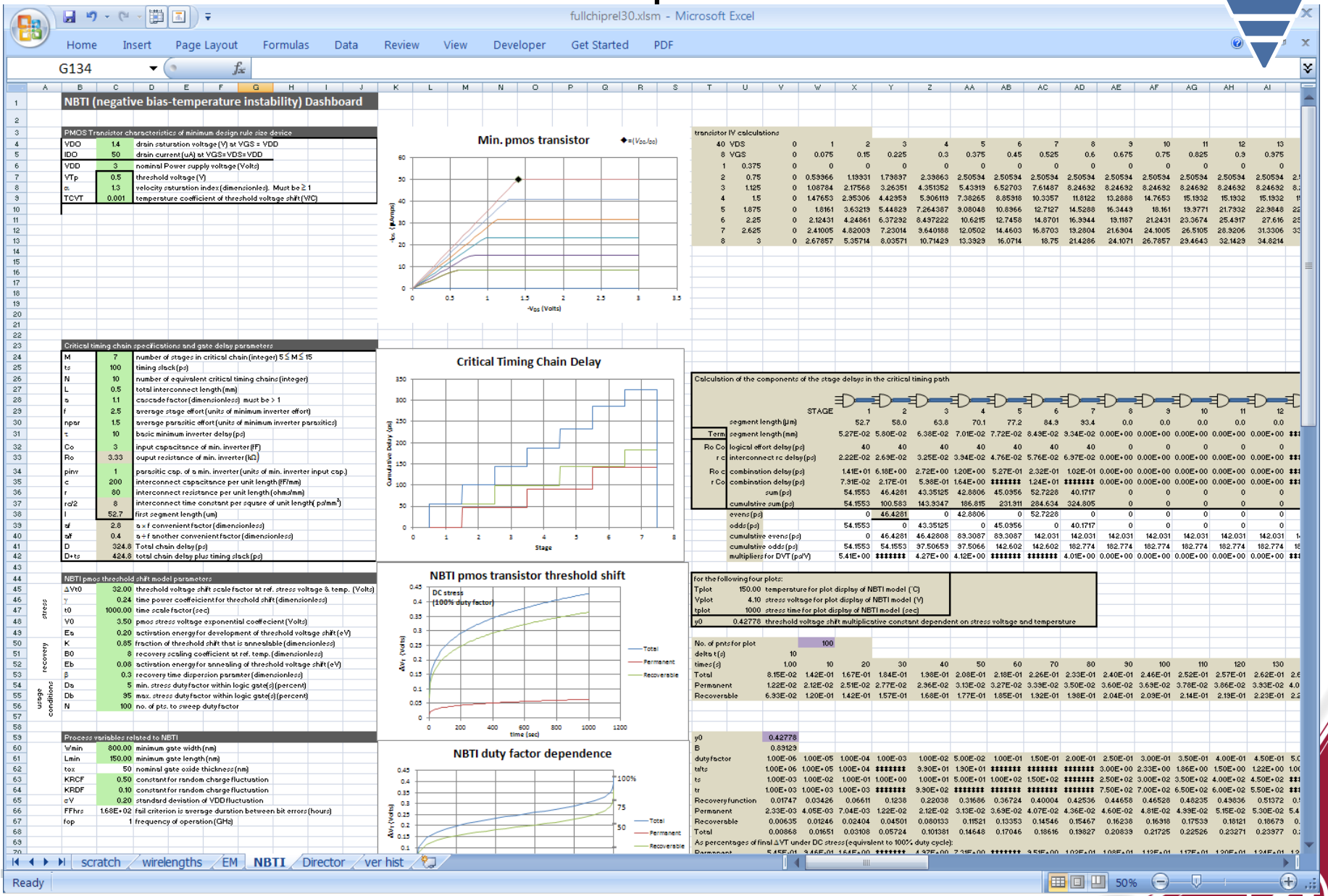
Contact: John Scarpulla or Jon Osborn

Digital ASIC Lifetime Failure Criterion (i.e. 1 failure per week or per year, …etc.)



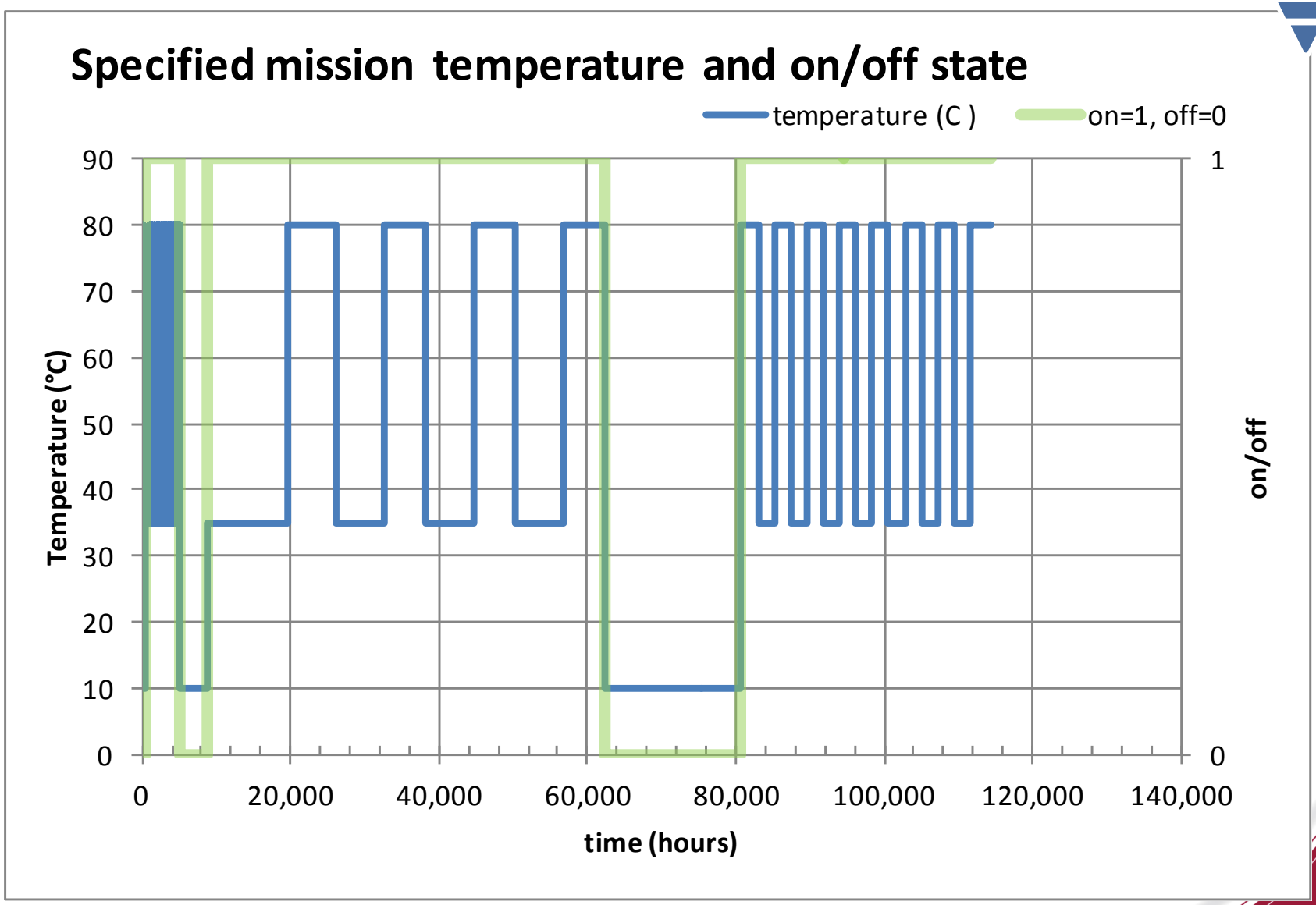
Contact: John Scarpulla or Jon Osborn

Ex: NBTI User Dashboard Inputs



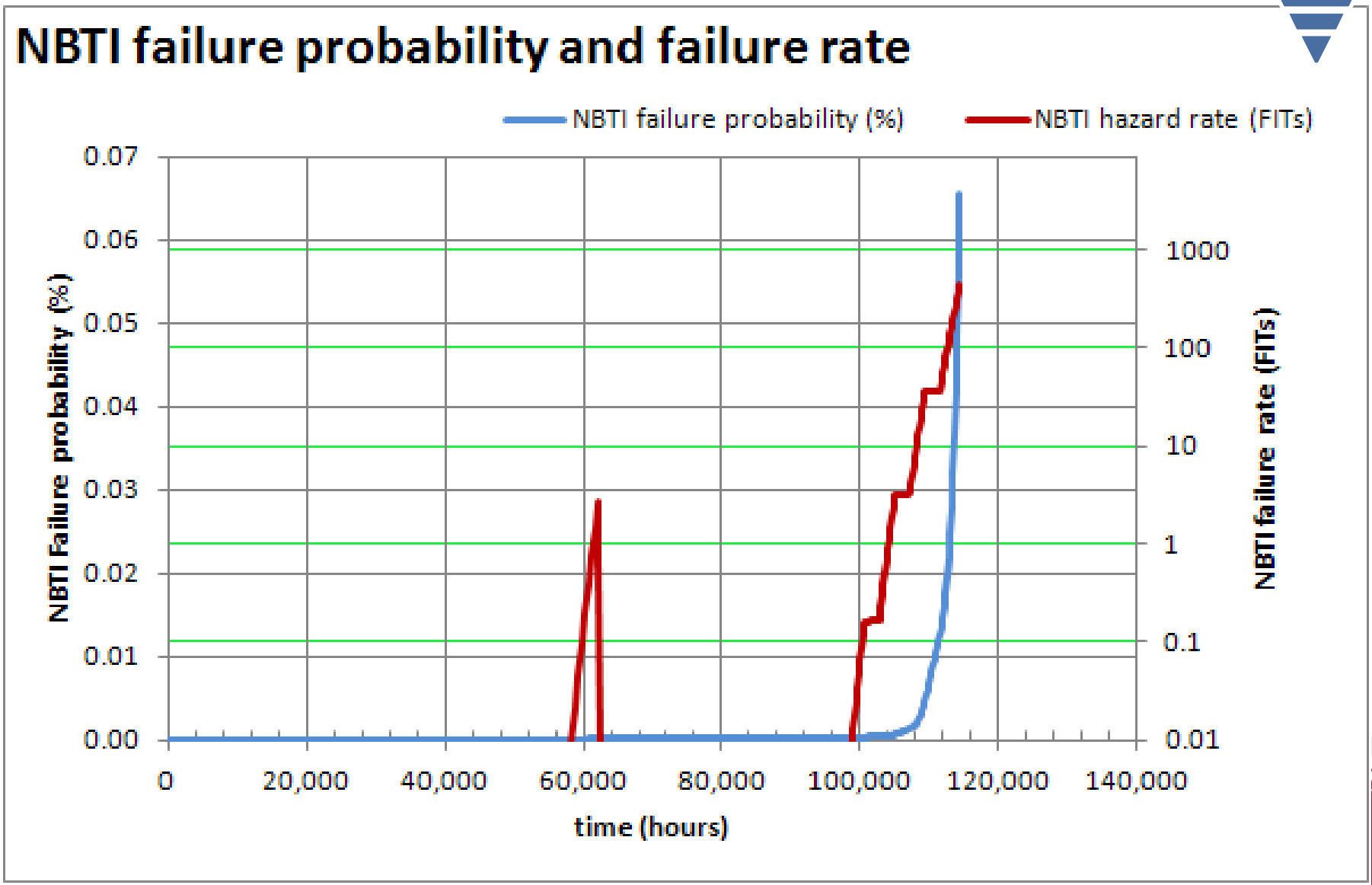
Contact: John Scarpulla or Jon Osborn

Ex: Mission Use Condition



Contact: John Scarpulla or Jon Osborn

Ex: Time evolved FIT rate calculation



Contact: John Scarpulla or Jon Osborn

CMOS ASIC PoF Lifetime Modeling – Looking Forward

- Develop PoF MD/DFT models of each of the major CMOS Failure Modes (Atomistic-Level)
  - *Provides better understanding of PoF and basic mechanisms*
  - *Coupled with nano-scale DPA, may enable **in silico** reliability prediction*
- Develop automated process to extract RelExpert compatible aged MOS models for any process node (Device-Level)
  - *BSIM Pro+ AgeMOS does not do SOI and Foundry Models are proprietary*
  - *Enables process specific End-of-Life Analog Mixed Simulation of circuits*
- Develop process to include BEOL wear-out mechanisms into circuit-level reliability simulator (Circuit-Level)
- Develop automated process to extract time evolved digital cell library timing degradation models (Circuit-Level)
- Complete Full-Chip 90nm CMOS ASIC Simulator (ASIC-Level)
- Develop advanced packaging time evolved failure rate models (ASIC-Level)

Summary

- HiREV nanoCMOS PoF Modeling Progress is Steady
  - *Primarily addressing device/circuit/ASIC lifetime reliability*
  - *Expanding into basic mechanisms and packaging*
- Multiple Technology Nodes Under Investigation
  - *Program Pull at 130/**90**/45nm*
  - *IR&D Interest at 32nm*
- Many opportunities for NEPP and HiREV to collaborate on PoF reliability data collection and model development at device/circuit/ASIC as well as package/board/unit levels of integration

Need more info?
Contact: Jon Osborn, Jon.V.Osborn@aero.org, 310-336-5453

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and

“This work supported by The Aerospace Corporation under the “Reliability By Design Corporate Research Initiative”