

Reliability of State-of-the-Art Digital Electronics

4th Annual NEPP Electronics Technology
Workshop (ETW)

Reliability of State of the Art Digital Electronics

- DfR Solution is developing algorithms for predicting service life of electronics
- Particular focus on part technologies present in next generation digital electronics
- Drivers
 - Part and package modifications are reducing useful lifetimes; not a concern for initial adopters
 - This technology will eventually migrate to longer life platforms in more severe operating environments

IC Reliability (Example) - Microprocessors

- 90nm Microprocessors

- 150-200 FIT over 5 years (0.11% AFR)

Part Number	Description	Node	Field Return Failure Rate (FIT)
MT16LSDF3264HG-10EE4	Micron 2GB SDRAM	130nm	689
M470L6524DU0-CB3	Samsung 512MB SDRAM	130nm	415
HYMD512M646BF8-J	Hynix 1GB DDRAM	130nm	821
MC68HC908SR12CFA	Freescale Microcontroller	90nm	221
RH80536GC0332MSL7EN	Intel 1.8GHz Pentium	90nm	144

- 65nm Microprocessor

- 422 FIT over 5 years (0.37% AFR)

Time in Use →	Operating Reliability Goals		
	0 – 1 Year (8760 hrs)	0 – 3 Years (26280 hrs)	0 – 5 Years (43800 hrs)
Cumulative Percent Fail	0.24%	0.85%	1.85%
Average Failure Rate	274 FIT	323 FIT	422 FIT

3X increase in AFR with decrease in node size

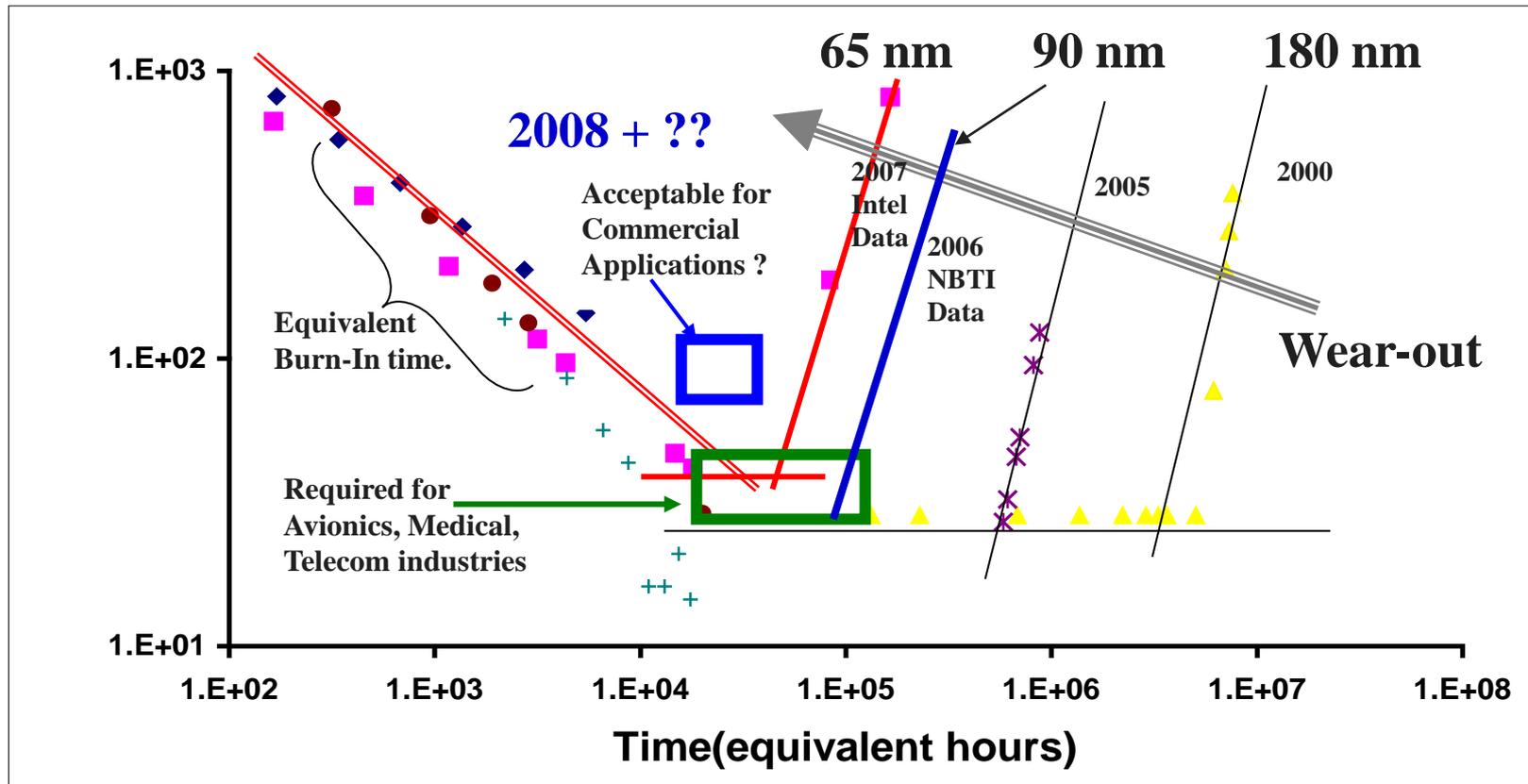
Reliability of Next Generation Microelectronics

- Growing concern in high reliability industries that systems utilizing high performance microelectronics ($\leq 90\text{nm}$ feature size) will not survive their anticipated lifetimes of 10 to 30 years
 - Failure will occur because of the short lifespans of individual transistors caused by intrinsic degradation (aging)
 - “It is a fallacy to say that integrated circuits will not fail because they have no moving parts. The sole reason they work is by the movement of charge carriers (electrons and holes) within them.”

“The notion that a transistor ages is a new concept for circuit designers,” ... aging has traditionally been the bailiwick of engineers who guarantee the transistor will operate for 10 years or so... But as transistors are scaled down further and operated with thinner voltage margins, it’s becoming harder to make those guarantees... transistor aging is emerging as a circuit designer’s problem.

IEEE Spectrum, June 2009

Failure Rates and The Bathtub Curve



- Some field data indicates that each new generation of integrated circuits is beginning to wearout sooner than the last

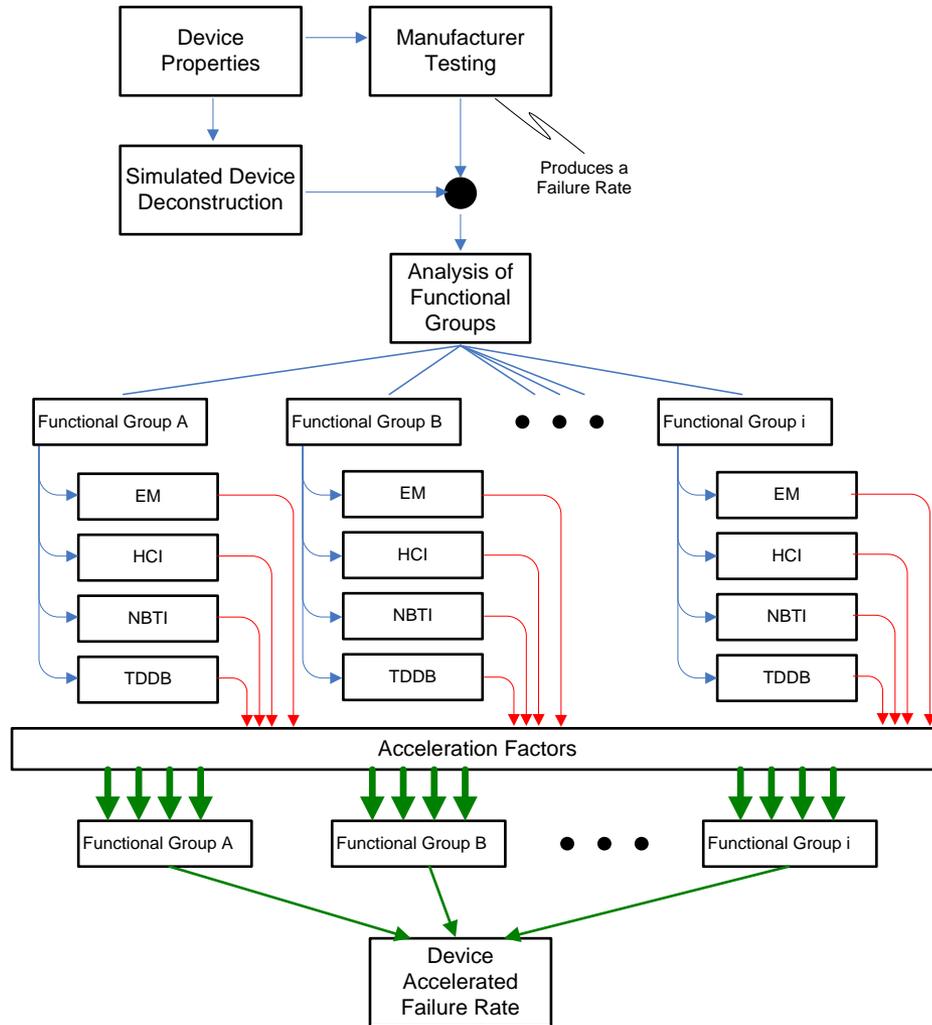
Challenges for IC Reliability Prediction

- Limited degree of mechanism-appropriate testing
 - Only at transition to new technology nodes
 - Mechanism-specific coupons (not real devices)
 - Test data is hidden from end-users (proprietary)
- Visible JEDEC tests are of limited value
 - Limited duration (1 000 hrs) does not necessarily demonstrate wearout behavior
 - Use of simple activation energy (0.7eV) with incorrect assumption that all mechanisms are thermally activated

Multi-Mechanism Approach

- Multi-Mechanism Approach developed in response to industry limitations
- Derives an acceleration factor off of JEDEC test results
 - Different acceleration algorithms for different wearout mechanisms (EM, TDDB, HCI, NBTI)
 - Different Weibull slopes (beta) for different wearout mechanisms
 - Circuit dependent, but only at functional block level (attempt to avoid intellectual property issues)

Multi-Mechanism Approach (cont.)



- Models simultaneous degradation behaviors of multiple failure mechanisms on integrated circuit devices
- Devised from published research literature, technological publications, and accepted degradation models from:
 - NASA\JPL
 - University of Maryland
 - Semiconductor Reliability Community

Key Assumptions

- Use of JEDEC accelerated test data in lieu of device time to failure data
- Default sub-circuit designs to analyze transistor stress states within functional blocks
- Single process node selection for each device
- Basic incorporation of redundancy and/or error correction techniques used in components

Resources that Define an IC

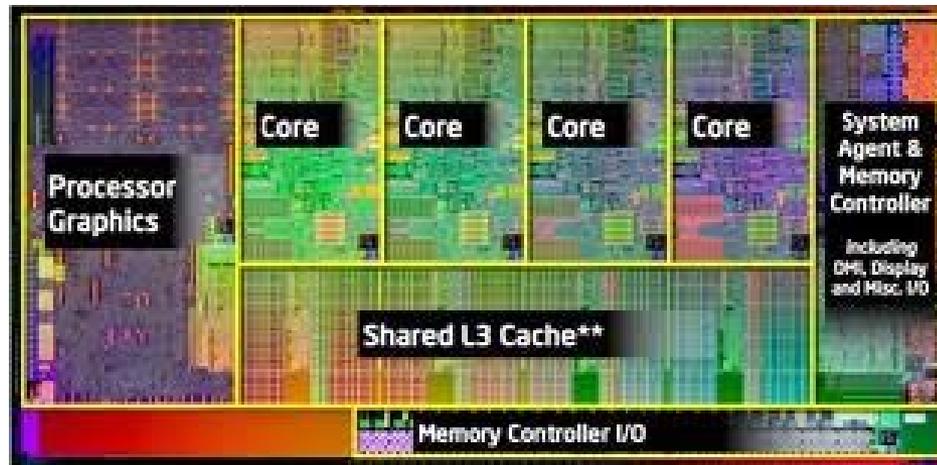
- Limited info available on integrated circuit design and reliability
 - Can we perform a prediction with just system-level design criteria (electrical and thermal data) and component documentation such as its datasheet?
- Knowledge of degradation mechanisms
 - Transistor stress states
 - Functional group susceptibility
 - Electrical and thermal conditions
- Integrated circuit materials and complexity
 - Technology node or feature size (i.e. 90nm)
 - Corresponding material set (e.g. Si, GaAs, SiGe, GaN and SOI)
 - Functional complexity
 - Identified as functional groups within a circuit
 - Operating conditions
 - Voltages, frequencies, currents, and temperature profile



IC Wearout Approach

- Define integrated circuit organization by functional groups
- Apply predefined transistor stress factors from SPICE analysis of “assumed” functional groups
- Characterize electrical and thermal conditions of customer application
- Define test conditions for IC reliability test
- Perform transistor level extrapolation using applicable failure mechanism models

Functional Group Breakdown of an IC

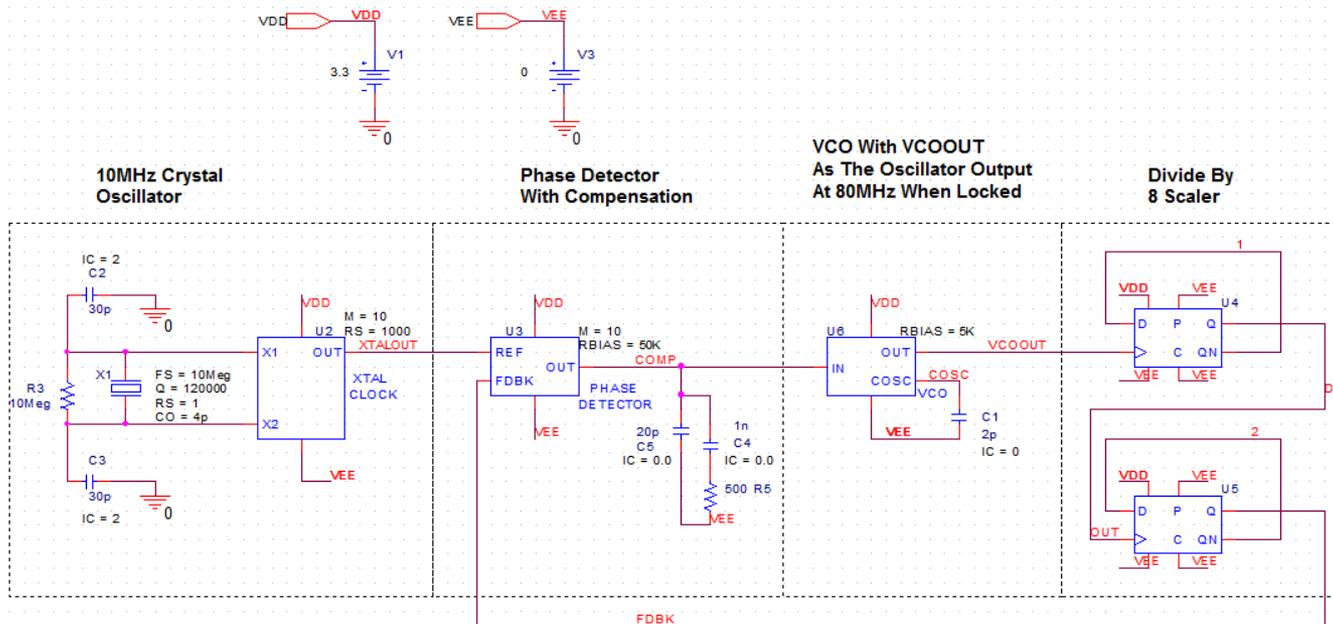


Graphic and overlay of Intel Core i5 Processor

- The complexity of an integrated circuit can be described as a set or multiple sets of smaller sub-circuits called functional groups
 - Each functional group can be comprised of multiple cells which are the basic building blocks of the group, i.e. SRAM bit or processor core
- Each functional group experiences different electrical stresses which can be quantified by analyzing transistor stress states
 - Degradation mechanisms come into play under specific transistor stress states such as drain bias for HCI or gate bias for BTI

Analyzing Transistor Stress States

- Establish relevancy of failure mechanisms, weighting factors, and inputs into Physics-of-Failure algorithms based on
 - Quantity and location of transistors within circuit
 - Probabilistic likelihood of applied operation conditions through background simulation of each functional group
 - Future versions may allow real-time input of component design file to output weighting factors without transfer of proprietary design



Phase-locked loop (PLL)

Circuit designed using CMOS library and components build from transistor models

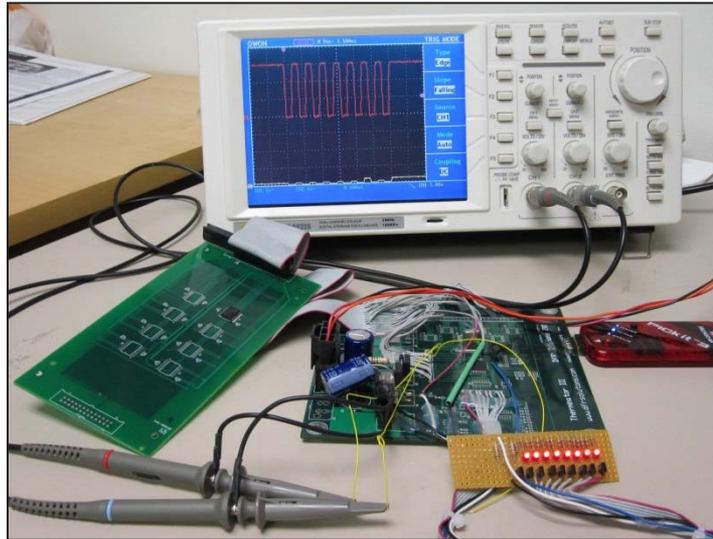
All transistors are analyzed against electrical criteria

Validating Prediction Methodology

- The process flow uses technology node based degradation models which provide the ability to extrapolate from an appropriate accelerated test to anticipated field conditions
 - An appropriate functional test to stress the integrated circuit similar to its application under field conditions, but in an accelerated way
- Utilizing Physics-of-Failure degradation equations, acceleration factors can be applied at the transistor level for clock frequency, voltages, and temperatures.

$$AF_{EM} = \left(\frac{f_1}{f_2}\right)^n \left(\frac{V_{dd1}}{V_{dd2}}\right)^\gamma e^{\left(\frac{E_a * T_1 - T_2}{k T_1 T_2}\right)}$$

$$AF_{NBTI} = \left(\frac{V_{gs1}}{V_{gs2}}\right)^\gamma e^{\left(\frac{E_a * T_1 - T_2}{k T_1 T_2}\right)}$$



$$AF_{HCI} = e^{\left(\frac{\gamma * V_{ds1} - V_{ds2}}{V_{ds1} V_{ds2}}\right)} e^{\left(\frac{E_a * T_1 - T_2}{k T_1 T_2}\right)}$$

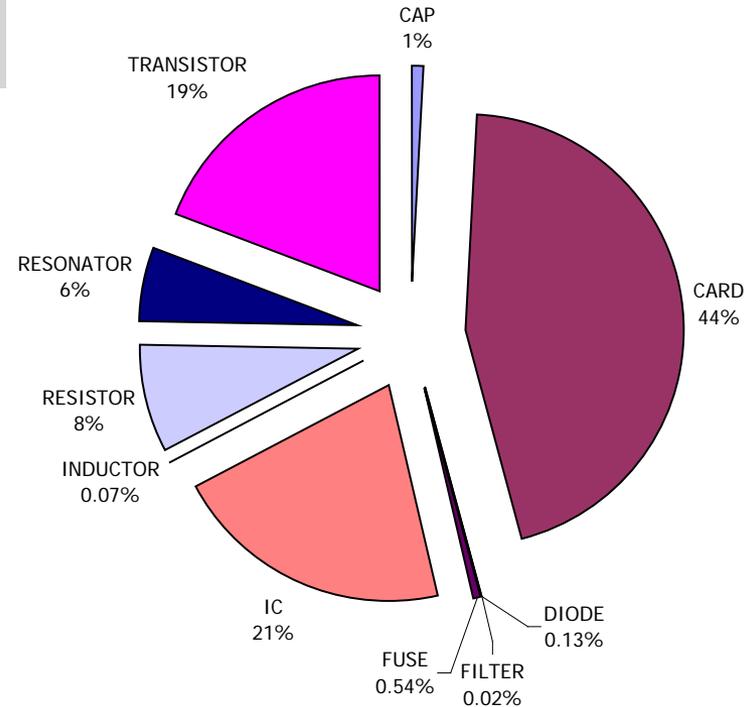
$$AF_{TDDb} = \frac{V_{gs1}^{(a+bT_1)}}{V_{gs2}^{(a+bT_2)}} e^{\left(c * \frac{T_1 - T_2}{T_1 T_2} + d * \frac{T_1^2 - T_2^2}{T_1^2 T_2^2}\right)}$$

Image of a FLASH memory bit-level write/read test to determine bit life without wear leveling

Validation Study (130nm to 90nm)

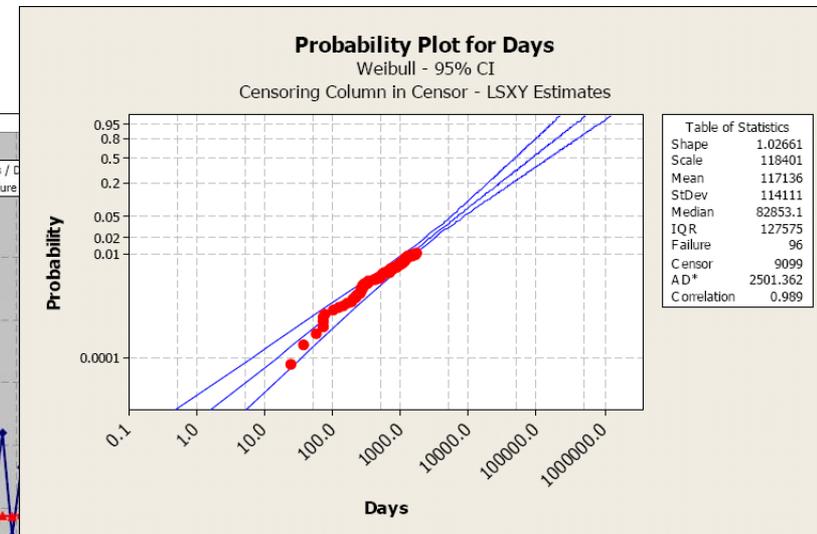
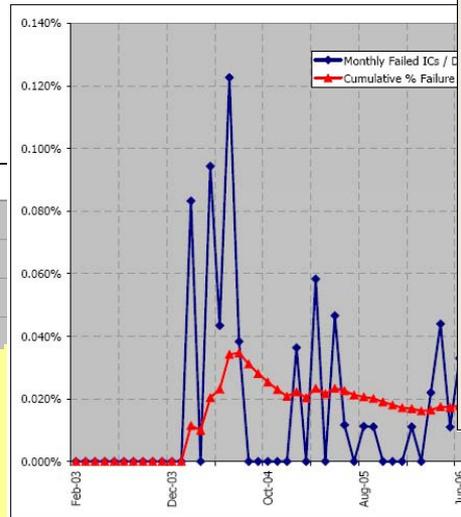
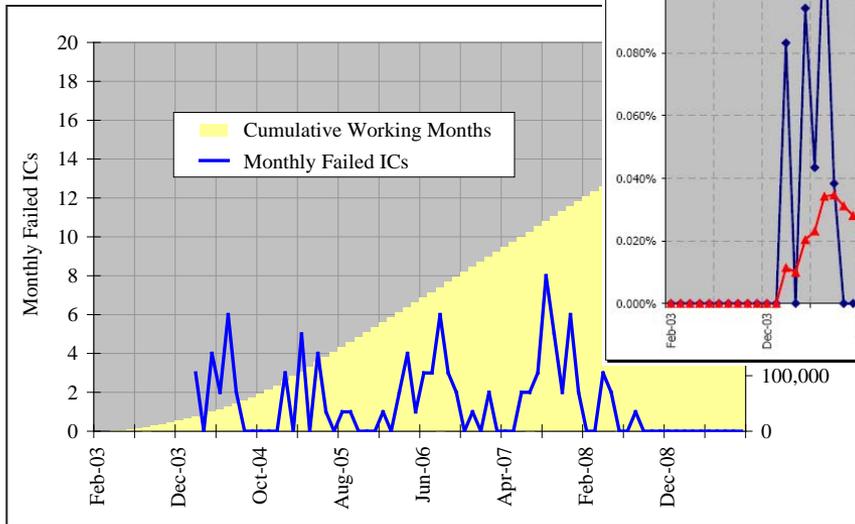
- Field return data was gathered from a family of telecommunication products
 - 56 different ICs comprised 41.5% of the failed part population
- The validation activity was utilized failure data from 5 integrated circuits

<u>Year</u>	<u>Description</u>	<u>Quantity Replaced</u>
2004	1 GB DRAM	190
2001	256MB DRAM	152
2005	512MB DRAM	161
2002	Microcontroller	114
2005	Microprocessor	18



Statistical Analysis on Field Returns

- Failure rate was calculated from raw data
 - Environmental conditions to determine in-field operating temperature
 - Thermal measurements to determine power dissipation
 - Cumulative failure distributions
 - Weibull
 - Exponential



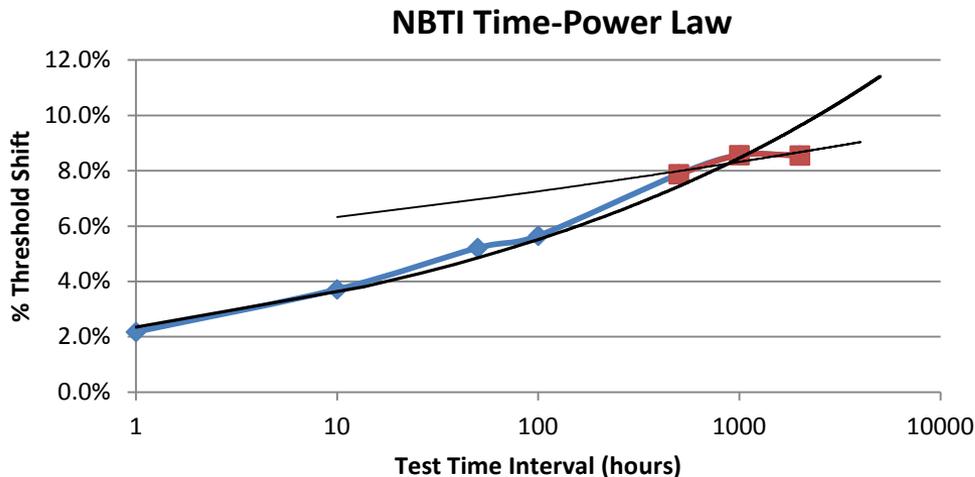
Extracted graphs from statistical analysis of field returns

- Multi-mechanism approach is far more accurate than other existing methodologies and does not require any field data

Description	Failure in Time (FIT) (failures per billion operating hours)				
	Field Data	Sherlock	JEDEC ($E_a = 0.7\text{eV}$)	SR-332	MIL-HDBK-217F
DRAM (256MB)	689	730	51	15	18
DRAM (512MB)	415	418	51	15	18
DRAM (1GB)	821	1012	51	15	18
Microcontroller	220	249	51	27	18
Microprocessor	144	291	51	67	2691

Next Steps: Testing at Functional Block Level

- Functional testing was performed on 45nm Silicon-on-Insulator ASIC PMOS transistor arrays to drive wearout by NBTI
 - The design of the arrays were known, therefore it was not necessary to create an “assumed” circuit for SPICE analysis
 - Transistor stress state analysis → normalized “critical constants”
 - Extrapolation using NBTI Power-Law model using our methodology predicted degradation of threshold voltage by 10% after 6 years of use under field conditions



$$AF_{NBTI} := \left(\frac{V_{gs1}}{V_{gs2}} \right)^{\gamma} e^{\left(\frac{E_a}{k} \cdot \frac{T_1 - T_2}{T_1 T_2} \right)}$$

Acceleration Transform for NBTI

Next Steps: Testing at Component Level

- Testing of Intel Ivy Bridge i7, fabricated at the 22nm technology node
 - Overclocked to ensure operation at maximum achievable clock and bus speeds (4.4 GHz vs. 3.8 GHz)
 - Ten (10) systems
- Several iterations of stress loading to achieve maximum multi-core CPU and RAM stress without bandwidth throttling
 - Floating point and integer mathematics
 - Polynomial arithmetic
 - Markov state models
 - Game, physics and texture (i.e. fur) rendering

Testing at Component Level (cont.)

- Hot (65C) and Cold (-25C) Testing at System-Level
 - Temperature based on thermal diode
- CPU core voltages recorded daily

The image shows a screenshot of a system monitoring application. On the left, there is a 'System Information' window with a 'CPU' tab selected. It displays the following details:

CPU Name	Intel(R) Core(TM) i7-3770S CPU @ 3.10GHz		
CPU Infos	Ivy Bridge, 4 Cores, MMX, x86-64, SSE4.2		
Motherboard	Gigabyte Technology Co., Ltd.: G1.Sniper 3		
	Current	Original	Overclock
CPU	4211.3 MHz	3100.0 MHz	35.8%
Bus	108.0 MHz	100.0 MHz	8.0%

On the right, there is a voltage monitoring table with four columns:

CPU VTT	1.07V	1.07V	1.07V
VCC3	3.32V	3.3V	3.32V
+12V	12.17V	12.17V	12.17V
+VCC	3.36V	3.36V	3.36V
CPU VCORE	1.32V	1.31V	1.32V
DRAM	1.51V	1.51V	1.51V
+3.3V	3.36V	3.36V	3.36V
VBAT	-42949672	-42949672	-42949672

- 80% of cold side systems are unstable after 5 months
 - Operational only at half factory clock speed (1.5 GHz) without stress loading

Next Steps: Developing Reliability 'Packets'

- Suppliers perform in-house EDA of their designs. Each design results in a table row of “critical constants.”
 - Analysis would quantify each of the transistor stress states necessary to degrade the transistors by each applicable mechanism during typical use duty cycles
- The “counts” per failure mechanism type would be normalized for the IC or functional group within the IC (standard libraries)
 - This process would replace the current process of SPICE analysis on “assumed circuits”
- Characterize electrical and thermal conditions of customer application
- Define test conditions for IC reliability test
- Perform transistor level extrapolation using applicable failure mechanism models

Conclusion

- Next generation complex integrated circuits demonstrate issues in regards to reliability performance
 - Additional issues in regards to packaging must also be addressed
- Current solution set is independent from component manufacturers
 - Comprehensive approach requires eliminating reliability performance as intellectual property

Who is DfR Solutions?

Best Design

Verification Tool

- Printed Circuit Design

*The Industry Leader in
Quality-Reliability-
Durability
of Electronics*

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- Inc Magazine

**2012 Global
Technology
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Key Facts

- Founded in 2005
- 30+ Employees, Multiple worldwide locations
- Software, Consulting, Research, Lab Services

Over 600 Customers

**Most Major Avionic
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