CLASS Y DEMONSTRATORS
(Infusion of New Technology into DoD Standards)

NASA Electronic Parts & Packaging Program (NEPP)
Electronics Technology Workshop (ETW)

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S. Agarwal
NASA - Jet Propulsion Laboratory, California Institute of Technology
Pasadena, California, USA
Shri.g.agarwal@jpl.nasa.gov

The Curiosity rover examines a rock on Mars with a set of tools at the end of the rover's arm, which extends about 7 feet (2 meters).
Image credit: NASA/JPL-Caltech

Agenda

- Introduction
- The “Class Y” Initiative, Bringing new technology into QML
  - What is it?
- Class Y Demonstrators
  - PIDTP
    - Definition
    - Non-hermetic Packages; Flip-chip Assemblies; Solder Terminations
  - Supplier Data
    - Aeroflex; Xilinx; Honeywell; BAE; e2v
- Getting to Class Y Qualification
  - Release of Spec 38535K (which contains Class Y requirements)
  - Class Y Suppliers Audits
    - Certification, Qualification
- Concluding Remarks

What is the “Class Y” Initiative?

- Advances in packaging and device technology are happening rapidly.
- How do we enable space flight projects to benefit from the newly developed devices?
- NASA is leading a G12 initiative, called Class Y, for infusing this new type of complex devices into military/space standards. Class Y is envisioned as a new category of ceramic-based non-hermetic microcircuits, such as the Virtex-4 and Virtex-5 field programmable gate arrays (FPGAs) offered by Xilinx Corporation.
- Creation of a new class of microcircuits (such as Class Y) requires considerable effort. It must be coordinated with manufacturers, government agencies, prime contractors, and other interested entities (e.g., academia). Also, we need to ensure that all aspects of packaging configuration are adequately covered by the military documents, such as MIL-PRF-38535 and MIL-STD-883. These packaging aspects include flip-chips, underfills, adhesives, column attaches, and others
- New test methods must be created and the existing standards updated as necessary.

Infusion of New Technology into Mil Standards Adding Class Y to Microcircuits Specification

- **Microcircuits specification, MIL-PRF-38535**
  - Next revision (K) is in preparation
  - Includes Class Y requirements
  - Second draft available now
  - Comments due by June 24, 2013

- **Acknowledgements**
  - Special thanks to DLA-VA
  - Thanks to everyone including task group (TG) members and advisors

- **Class Y Status**
  - See the next sheet

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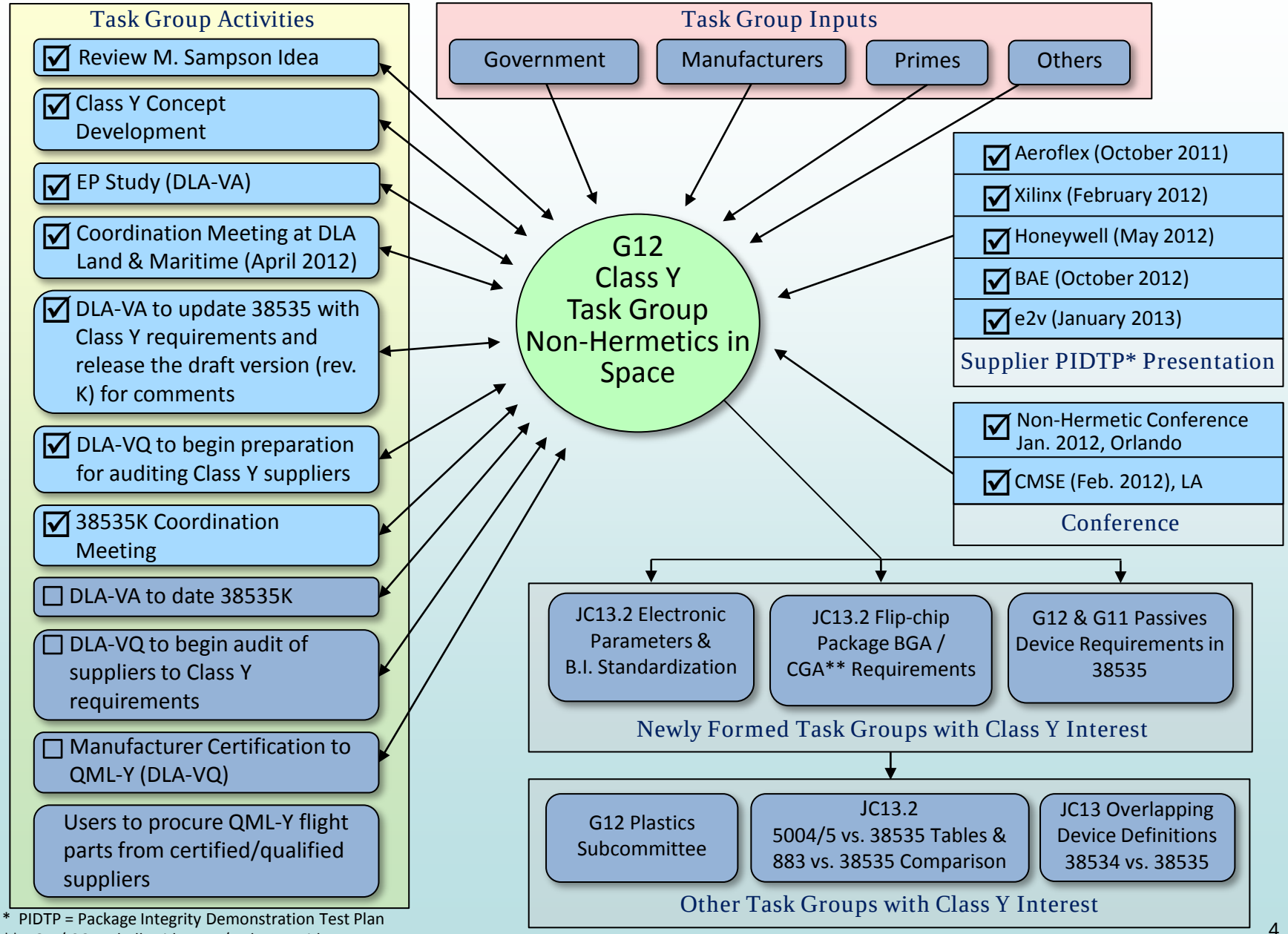
Infusion of New Technology into QML System
G12 Class Y Effort at a Glance



* PIDTP = Package Integrity Demonstration Test Plan
** BGA / CGA = ball-grid array / column-grid array

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Infusion of New Technology into Mil Standards, Class Y
Qualifying New Packaging Technology

- **Issue**
  - How to address the manufacturability, test, quality and reliability issues unique to specific non-traditional assembly/package technologies intended for space applications?

- **Solution Proposed**
  - Each manufacturer to develop a Package Integrity Demonstration Test Plan (PIDTP).
  - Addresses issues unique to non-hermetic construction and materials, such as potential materials degradation, interconnect reliability, thermal management, resistance to processing stresses, thermo-mechanical stresses, & shelf life.
  - The PIDTP shall be approved by QA after consultation with the space community. Ref: 38535K, Para B.3.11

Infusion of New Technology into Mil Standards, Class Y Applicability of the PIDTP

- **The PIDTP Requirement would apply to:**
  - Non-hermetic packages (e.g., Class Y)
  - Flip-chip assembly
  - Solder terminations

- **Microcircuits employing more than one of above technologies shall include elements for each in the PIDTP** (See 38535K, Para H.3.4.4.1).

Infusion of New Technology into Mil Standards, Class Y PIDTP – Non-hermetic Packages

- **Non-hermetic Packages (Class Y)**

  For class Y microcircuits, the PIDTP must address issues unique to non-hermetic construction and materials, such as potential materials degradation, moisture absorption, and resistance of active devices, passive devices and interconnects to environmental effects and processing stresses. Moisture sensitivity level characterization (ref: IPC/JEDEC J-STD-020D) should be performed for exposed flip-chip underfill or thermal grease/epoxy. Ref: 38535K, Para H.3.4.4.1.

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Infusion of New Technology into Mil Standards, Class Y PIDTP – Flip-chip Assembly

- **Flip-chip Assembly (Class V or Class Y)**

For space microcircuits employing flip-chip assembly technologies either class V or class Y (class level S), the PIDTP must address the materials and processes unique to solder bump interconnect attach, underfill and lid-to-die attach. The plan shall, at a minimum, demonstrate how the following are evaluated and monitored including a corresponding package level reliability demonstration. Ref: 38535K, Para H.3.4.4.1.2.

  - Substrate materials
  - Bump geometry
  - Solder bump deposition process and materials
  - Flux materials
  - Underfill materials
  - Lid (or heat spreader) attach/adhesive materials

Infusion of New Technology into Mil Standards, Class Y PIDTP – Solder Terminations

- **Solder Terminations (Class V or Class Y)**

  For space microcircuits employing solder terminations (class V or class Y), the PIDTP shall must address the materials and processes unique to solder terminations, such as ball/column integrity, attachment integrity, damage due to test, protection for shipment and shelf life. Manufacturer's shall perform post column attachment electrical characterization over temperature and compare data with pre-column attachment process to assess any damage due to column attachment process. Ref: 38535K, Para H.3.4.4.1.3.

Supplier Interest in Class Y

- **The front runners (See the G12 website for complete presentations)**
  - Aeroflex :
    - Presented their data on underfills and temperature cycling
  - Xilinx:
    - Presented data on V-4 FPGA. Also on BME capacitors.
  - BAE:
    - As part of their presentation, they showed the results of over temp electricals taken before and after column attachment
  - Honeywell:
    - Presented on material properties
  - E2v (Grenoble, France):
    - Presented on-board level test results
- **Others**
  - Texas Instruments
  - Microsemi Actel
  - Intersil
  - Cypress
  - 3D

Class Y
Package Integrity Demonstration Plan, PIDTP
Preliminary Data Sharing with the Space Community

- Presentations by Major Suppliers (see G12 website for complete presentations):
  - ☑ Aeroflex (Presented at the Class Y TG meeting in October 2011)
  - ☑ Xilinx (Presented at the TG meeting in February 2012)
  - ☑ Honeywell (Presented at the TG meeting in May 2012)
  - ☑ BAE (Presented at the TG meeting in October 2012)
  - ☑ e2v (Presented at the TG meeting in January 2013)
  - ☐ TBD

Sample Preliminary PIDTP
(Ref: Aeroflex presentation at Oct. 2011 Class Y meeting)

- **Test Vehicles**
  - 1x1 die size, 2x2, and 3x3
- **Wafer Level Acceptance**
  - Bump and Die Yield
    - Computed average bump yield
    - Calculated die yield based on die size
  - Bump Height
    - Estimated average bump height
  - Bump Shear
    - Measured bump shear force
- **Underfill Material Selection**
  - Initial Screening
    - Five underfills selected based on vendor recommendations
  - Material Property Screening
    - IGA analysis per MIL-STD-883, TM1018
    - Outgassing per ASTM-E-595
    - Ionic Impurity per MIL-STD-883, TM5011
  - Final Selection for PIDTP
    - Selected three underfills for PIDTP evaluation.

Sample Preliminary PIDTP, (Contd.)
(Ref: Aeroflex presentation at Oct. 2011 Class Y meeting)

- **X-Ray Assembly Monitor**
  - Interconnects
    - Aligned vs. misaligned
- **CSAM Assembly Monitor**
  - Underfills
    - All three underfills evaluated for voids
- **Temperature Cycling Testing**
  - Conditions B (-55/125C) and C (-65/150C)
    - Weibull life predictions made (in cycles)
- **High Temperature Storage**
  - 1500 hr at150C, and 2000 hr at 125C
    - Die shear tests
- **Multiple Reflow Testing**
  - 20 reflows per JESD22-A113-B
    - Die shear tests

Preliminary PIDTP Summary
(Ref: Aeroflex presentation at Oct. 2011 Class Y meeting)

Test Type	Test Method and Conditions	Notes	Pass/Fail
Wafer Level Acceptance	Bump yield. Bump height. Bump shear.	Wafer bumping monitors.	**Pass**
Underfill Material Selection	TM 5011, ASTM-E-595.	Outgassing.	**Pass (Note 1)**
X-Ray Assembly Monitor	TM 2012.	Joint reflow.	**Pass**
CSAM Assembly Monitor	IAW Aeroflex procedures.	Underfill voids.	**Pass**
Temperature Cycle Testing	TM 1010. Condition C. Condition B.	Continuity resistance measurements.	**Pass**
High Temperature Storage	JESD22-A103C. 1500 hours at 150C. 2000 hours at 125C. Eutectic test die on ceramic. SAC test die on build-up.	Die shear per TM 2011, Condition F.	**Pass 1500 hrs at 150C.** **Pass 2000 hrs at 125C.**
Multiple Reflow	JESD22-A113-B. 20 reflows using separate eutectic and SAC reflow profiles. Eutectic test die on ceramic. SAC test die on build-up.	Die shear per TM 2011, Condition F.	**Pass 20x reflows based on shear load.**

Note 1: Underfill I now listed on NASA outgassing web page.

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Summary of Xilinx Presentation at Feb. 2012 Class Y Meeting—Qualification Summary

- Xilinx qualifies QV CF packages (with 0805 & 603 chip capacitors attached to the package) at die/package component level.
- Xilinx is satisfied that this qualification guarantees the reliability of the product, including the chip capacitors
- 10 years worth of life test, temperature cycling, & HAST Qualification & reliability monitor data on commercial flip chip packages (with same 0805 & 0603 capacitors) with no package or chip capacitor failures.
- See the G12 website for complete presentation

Comments/Differences from Proposed Class Y

Ref. Honeywell Presentation at May 2012 Class Y Meeting

- Underfills are not qualified to TM 5011
  - 5011 underfills not available from our supplier
  - TM 5011 Table I does not address underfills; must be revised
  - Underfills all pass NASA outgassing per ASTM E595
- CSAM preferred over X-ray as inspection method
  - CSAM detects underfill defects which affect reliability
  - X-ray only detects shorts or badly deformed bumps—observable by electric test
- Internal visual (TM 2010) must be done before assembly
- Constant acceleration is not a meaningful screen for flip-chip die without lids
  - Constant acceleration is only needed for lid or cap attach
- Die shear for Group B testing is not meaningful
  - All die shear testing at Honeywell has exceeded equipment limits
- Salt atmosphere testing is not meaningful for Group D
  - No Kovar or corrodible metal in the package
- Temp/humidity test (unbiased HAST) is recommended for QCI Group D
  - More important than mechanical Group D4

Honeywell QCI Plan

Ref. Honeywell Presentation at May 2012 Class Y Meeting

- Group B QCI to be performed on each build of flip chip product or quarterly, whichever is less frequent
  - Based on proposed QML Class Y (not yet released)

- Group D QCI to be performed on each build of flip chip product or every 6 months, whichever is less frequent
  - Class Y proposal doesn't give guidance for Group D
  - Manufacturers must propose their own Package Integrity Demonstration Test Plan

Honeywell Summary

Ref. Honeywell Presentation at May 2012 Class Y Meeting

- Honeywell has been developing non-hermetic flip chip packaging for more than 10 years
  - Extensive reliability characterization
- Qualification plans have been reviewed frequently with customers and qualifying agencies
- Honeywell's screening flow and qualification plan follows the proposed Class Y, with some minor differences
- Honeywell fully supports establishment of Class Y for non-hermetic space products
  - Lack of a QML standard has been an impediment for customer acceptance of non-hermetic flip chip packaging in space applications

Ref: BAE Presentation at Oct. 2012 Class Y meeting

BAE SYSTEMS

Electrical Test With or Without Columns

BAE Systems performs burn-in and 3-temp testing without columns

- **Post-column attach: BAE Systems performs room temp testing only**

CGA Module Test Experiment (requested by Aerospace/NASA)

- 3 RAD750 devices were 3-temp tested without columns (Land Grid Array)
- Columns were attached
- Devices were then re-tested with columns (Column Grid Array)
- All 3 parts passed full Group A test both pre- and post-column
- Test results were compared pre- and post-column

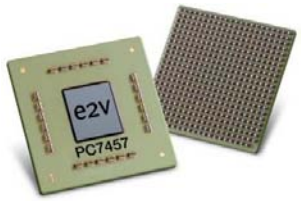
- Comparison of Input-Output Test Parameters shows < 8% deltas between pre- and post- column electrical test:

Parameter	Temp	s/n 2605	s/n 2788	s/n 2829
Input leakage (high voltage) (IIH)	+25C	< 0.5%	< 1%	< 0.5%
	-55C	< 6%	< 1.5%	< 1.5%
	+125C	< 7%	< 7%	< 8%
Input leakage (low voltage) (IIL)	+25C	< 1%	< 1.5%	< 1%
	-55C	< 3%	< 3.5%	< 3.5%
	+125C	< 1.5%	< 2%	< 2%
Voltage Output High (VOH)	+25C	< 0.5%	< 0.5%	< 0.5%
	-55C	< 1%	< 0.5%	< 0.5%
	+125C	< 0.5%	< 0.5%	< 0.5%
Voltage Output Low (VOL)	+25C	< 3.5%	< 7%	< 3.5%
	-55C	< 6% *	< 7%	< 5%
	+125C	< 4%	< 4%	< 3.5%
Dynamic I/O Idd	+25C	< 3%	< 3%	< 3%
	-55C	< 3%	< 3%	< 2.5%
	+125C	< 3%	< 3.2%	< 3%

* except 1 pin at 12%

Ref: e2v Presentation at Jan. 2013 Class Y meeting

ON THE WAY TO QML-Y
From “QML-Y like” products to “QML-Y” qualified products



C7457

PC8548

Space Program Development

QML-Y Qualified Products

Upgraded Flip Chip Assembly Line

+

QML-Y Screening

Screening Requirements in Draft 38535K
Class V vs. Class Y

- **Screening**
  - Same for both V and Y except the differences related to hermeticity vs. non-hermeticity.

- **Column Attached Parts (as offered by Manufacturers)**
  - 100% DC electricals post column attachment (same for V and Y)
  - Visual inspection (same for V and Y)
  - No additional screening requirement for V or Y

QCI Requirements in Draft 38535K
Class V vs. Class Y

- **QCI (Land Grid Array)**
  - Group A :
    - Same for both V and Y
  - Group B:
    - Same, except hermeticity vs. non-hermeticity differences
  - Group C:
    - Same
  - Group D:
    - Same except hermeticity vs. non-hermeticity differences
    - Added PIDTP.
      - PIDTP (Flip-chip) and PIDTP (Solder terminations): Same for V and Y
      - PIDTP (Non-hermetic packages): Class Y only
  - Group E:
    - Same for both V and Y

- **Column Attached Parts (as offered by Manufacturers)**
  - Columns shear test
  - Group A, Subgroup 1 only:
    - Same for V and Y

Infusion of New Technology into the QML System Roadmap to QML-Y Flight Parts Procurement

- Major Milestones:
  - ☑ G12 approval of TG charter
  - ☑ G-12 Class Y Task Group to develop requirements
  - ☑ G12 approval for DLA-VA to commence EP study
  - ☑ DLA-VA to conduct EP study
  - ☑ DLA-VA to release “final” report
  - ☑ Coordination meeting at DLA Land and Maritime (April 2012)
  - ☑ DLA-VA to update 38535 with Class Y requirements and release the draft version (rev. K) for comments
  - ☑ DLA-VQ to begin preparation for auditing Class Y suppliers
  - ☑ 38535, rev. K Coordination meeting

  - ☐ DLA-VA to date 38535, rev. K
  - ☐ DLA-VQ to commence audit of suppliers to Class Y requirements

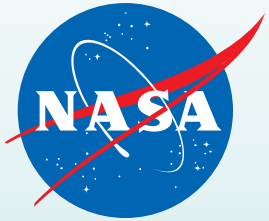
- After milestones completed,
  Users to procure QML-Y flight parts from certified/qualified suppliers

Closing Remarks

- The Class Y experiment has shown that it takes a considerable amount of time and effort to infuse new technology into the QML system.
- Needed to develop a new concept, PIDTP, to address the complexities of advanced packaging technologies.
- A lot of work remains to be done.

- NASA Electronic Parts Assurance Group (NEPAG)

http://nepp.nasa.gov



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