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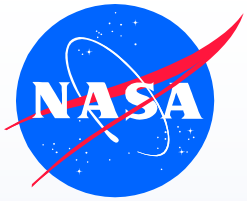

NEPP Electronic Technology Workshop
June 17-19, 2014

Cubesat Processor Radiation Efforts

Steven M. Guertin

Jet Propulsion Laboratory / California Institute of Technology

Pasadena, CA

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Under contract with the National Aeronautics and Space Administration (NASA)
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Outline

- Motivation
- Microcontrollers – Current Cubesat Devices
  - Selection Efforts
  - MSP430 SEE and TID
  - PIC SEE and TID
- Microprocessors – Expected Use Soon
  - Selection
  - Snapdragon Efforts
  - Atom
- Future Work

Key Issues

- Common paradigm of Cubesat processing
  - Small
  - Low Power
  - Microcontroller-like
  - A couple common processors/microcontrollers
- Looking forward
  - We expect that processing desire will increase
  - Instruments may become more computation intensive
  - Primary processors may migrate for more computation
- Approach for improving mission assurance
  - Determine mission assurance issues for current-generation microcontrollers/microprocessors– focus on SEL/gross SEE, and TID (Primarily LEO and GEO/GCR environments)
  - Build repository of knowledge for devices for future use

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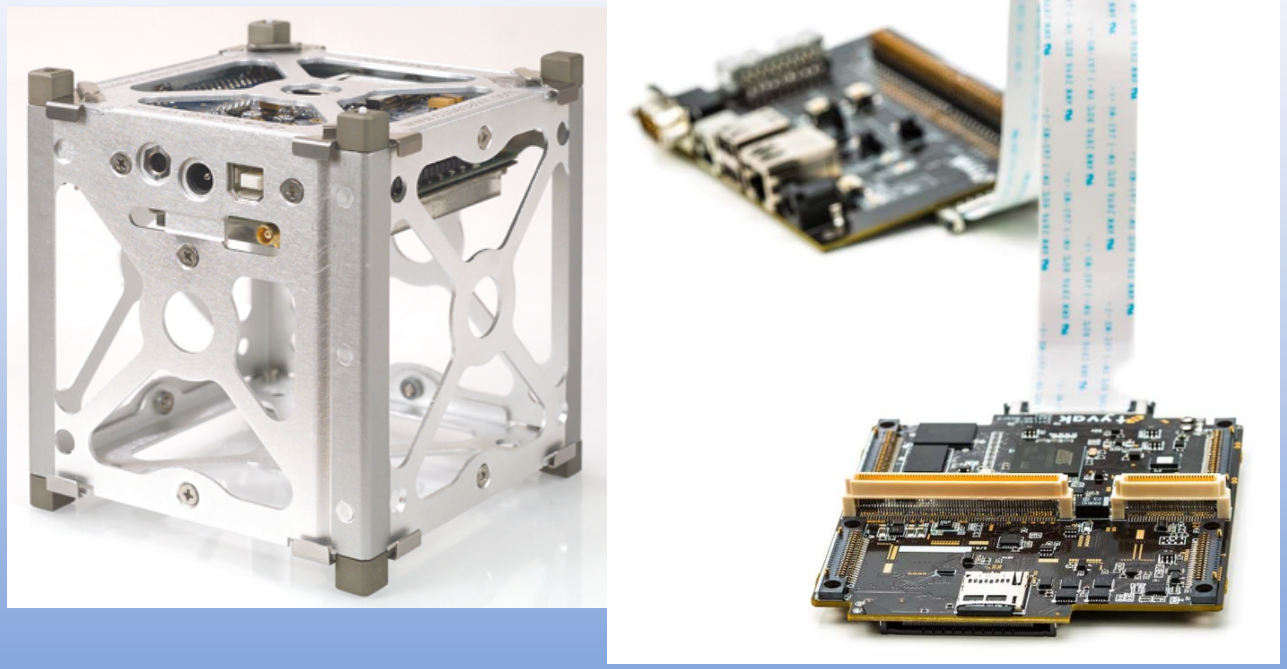

CUBESAT MICROCONTROLLERS

To be presented by Steven M. Guertin at the 5th NASA Electronic Parts and Packaging (NEPP) Program Electronic Technology Workshop June 17-19, 2014, NASA GSFC, Greenbelt, MD.

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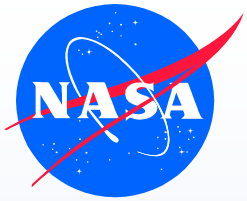
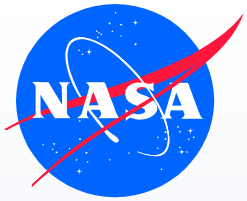
Cubesat Controller Survey



- Reviewed many Cubesat system architectures
  - Verified device ordering approach with Pumpkin – they indicate orders are simple “no special procedures” quote and buy from places like Digikey

CubeSat Provider	Processor	Availability	Development Board
Pumpkin	TI MSP430F1612	Yes	Yes
	TI MSP430F1611	Yes	Yes
	TI MSP430F1618	No	No
	Silicon Labs C8051F120	Yes	Yes
	Microchip PIC24FJ256GA110	Yes	Yes
	Microchip dsPIC33FJ256GP710	Yes	Yes
Tyvak (Intrepid)	AT91SAM9G20 (ATMEL, ARM9 Based)	Yes	Yes

CubeSat Provider	Processor	Availability	Development Board
GOMspace (NanoMind)	AT91SAM7 series (ATMEL, ARM7 Based)	Unknown	Unknown
	ATMEL ATMEGA1281	Yes	Unknown
Gaussteam (ABACUS)	TI MSP430 series	Yes	Yes
ESL/ISIS (Cube Computer)	ARM Cortex-M3 MCU	Unknown	Unknown
ISIS (OBC)	AT91SAM9G20 (ATMEL, ARM9 Based)	Yes	Yes
Clyde Space	Use Pumpkin CubeSat OBC	Yes	Yes

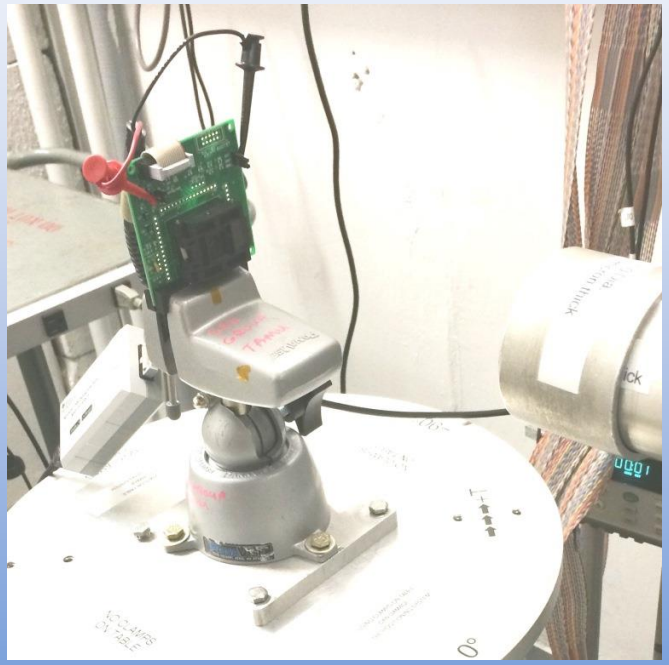


Microcontroller Selection

- Initial efforts
  - Currently focusing on the PIC and MSP devices
    - Database shows many missions use these
    - Believed they may show some significant problems
    - Relatively easy inside our flow for development
  - Pushing to the AT91SAM9G20
    - No data yet, but moving forward with test design and plan
    - ARM-based – in-line with Xilinx Zynq, and higher-end processors
- Follow-up
  - Most likely the AT91SAM9G20 will be studied more in the future (i.e. no likely to finish this FY)
  - Si Labs C8051
  - At present, focus is on SEL and TID. SEE effort may increase

SEE Testing – MSP430

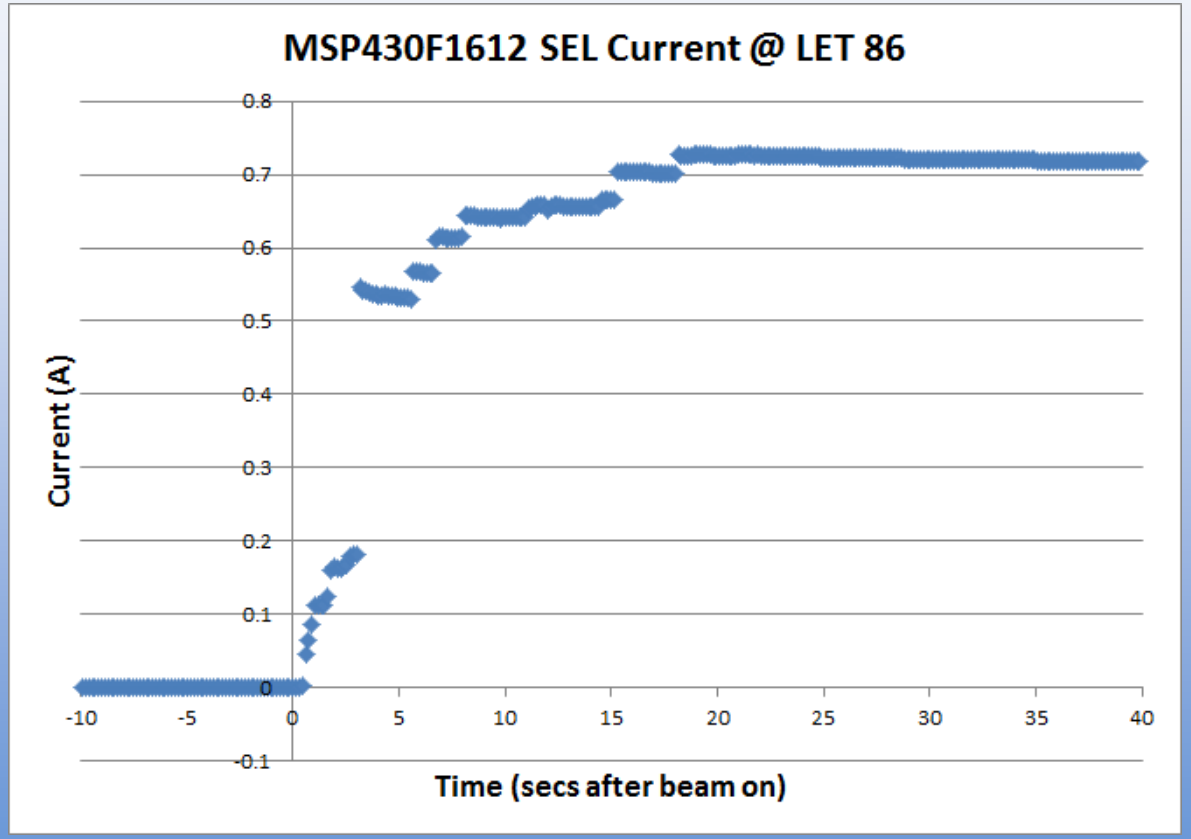
- Utilized MSP development kit
  - Prepared by acid-etching and using a socket with the plastic over the DUT drilled out
- Primary test effort
  - Performed SEL and limited SEE testing of MSP430F1612
  - Cursory comparison to MSPF4301611 shows similar behavior
- Socket on the board limited angular study
  - But SEL and SEU already observed so error in rates is in conservatism



MSP430F1612 positioned in the beam line at TAMU

SEL Results – MSP430

- MSP Devices Experienced increased current almost immediately after the beam was turned on.
- Nominal operating current is less than 1 mA
- Current “steps” observed, making signature messy
- Max current appears limited, but 100x or more of nominal…
- Device un-programmable and not running after 1e6 – but run at right is 3e4/cm^2 w/no failure

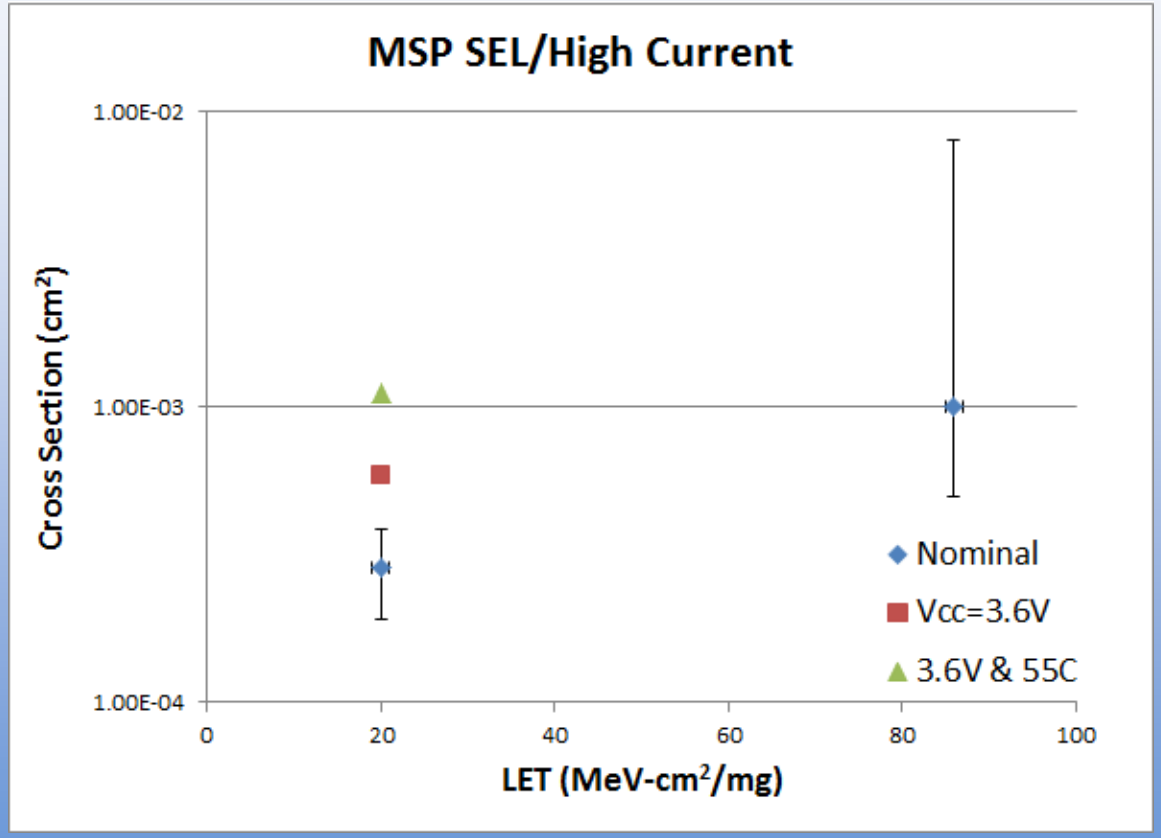


Flux = ~2e3/cm^2-sec

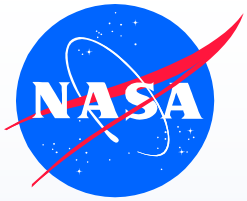
SEL Cross Section – MSP 430

- SEL behavior is common at tested LETs (20 and 86 MeV-cm^2/mg)
  - 0.05 A threshold
- Not recovered by reset
- Cannot measure other event types
- Expect to have cross section ~1e-6cm^2 at LET 10

- ISS event rate estimated between 2e-5 and 4e-4/day
  - ~10x higher for GCR



Error bars (nominal only) ~2σ, and include beam uncertainty



SEE Results – MSP430

- Tested MSP430F1612 for SRAM upsets
- Test program loads 2048 bytes with 0s or 1s (depending on pass number)
- Runs for general SEE observation used SEL protection, only LET 20 MeV-cm^2/mg was tested

LET (MeV-cm^2/mg)	Condition	SBUs	σ (cm^2/bit)
20	Nominal	66	4.2e-8
20	3.6V	21	3.0e-8
20	3.6V/55C	7	2.0e-8

- Reduced cross section with Vcc expected; final row probably reflects low statistics as temperature should have no impact

TID Testing of MSP 1611 & 1612

- Performed biased and unbiased testing
- Used JPL's high dose rate Co-60 room irradiator
- Between irradiation, tested with characterization programs:
  - LED blinker
  - Flash memory test program (provided in MSP development kit)
  - Whetstone test program
- Test steps: 1, 2, 5, 10, and 20 krad(Si)
- Unbiased devices showed no degradation at 20 krad
- Some biased 1611 devices became unstable at 10 krad
  - some devices failed to be reprogrammable at 20k, but instead seemed to be running the TID test program (LED blinking)

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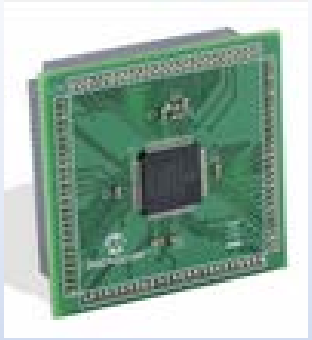
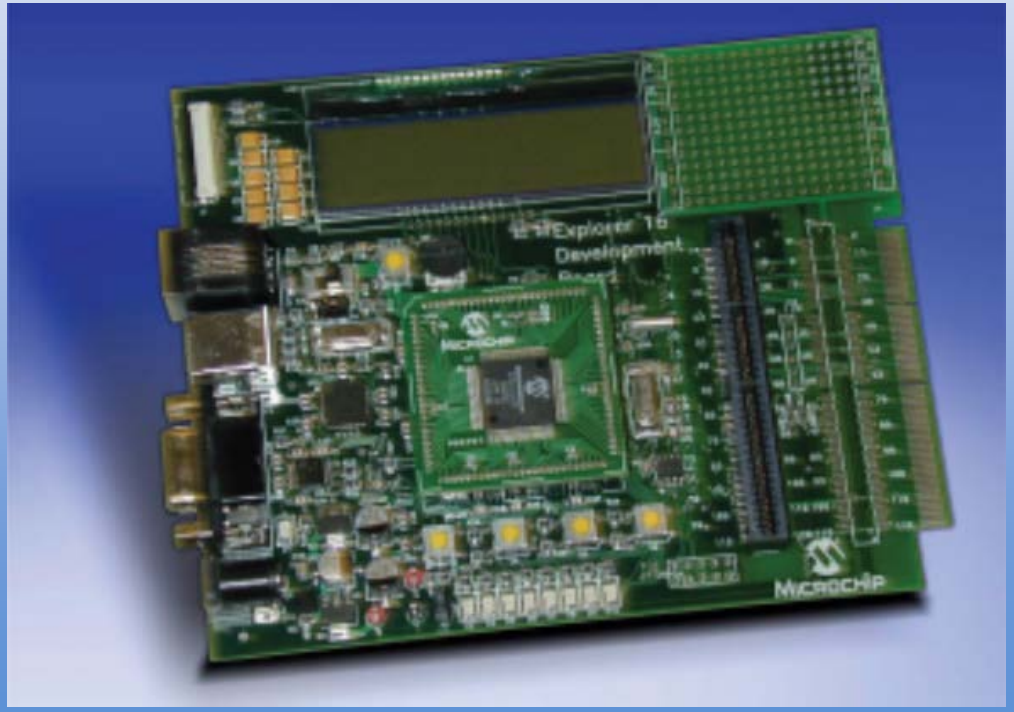
SEE Testing - PIC

- Used Explorer 16 board from Microchip
- Test Devices:
  - PIC24FJ256GA110
  - dsPIC33FJ256GP710
- Using on-board regulators
- Two test programs
  - RAM write/read
  - Flash read/dwell

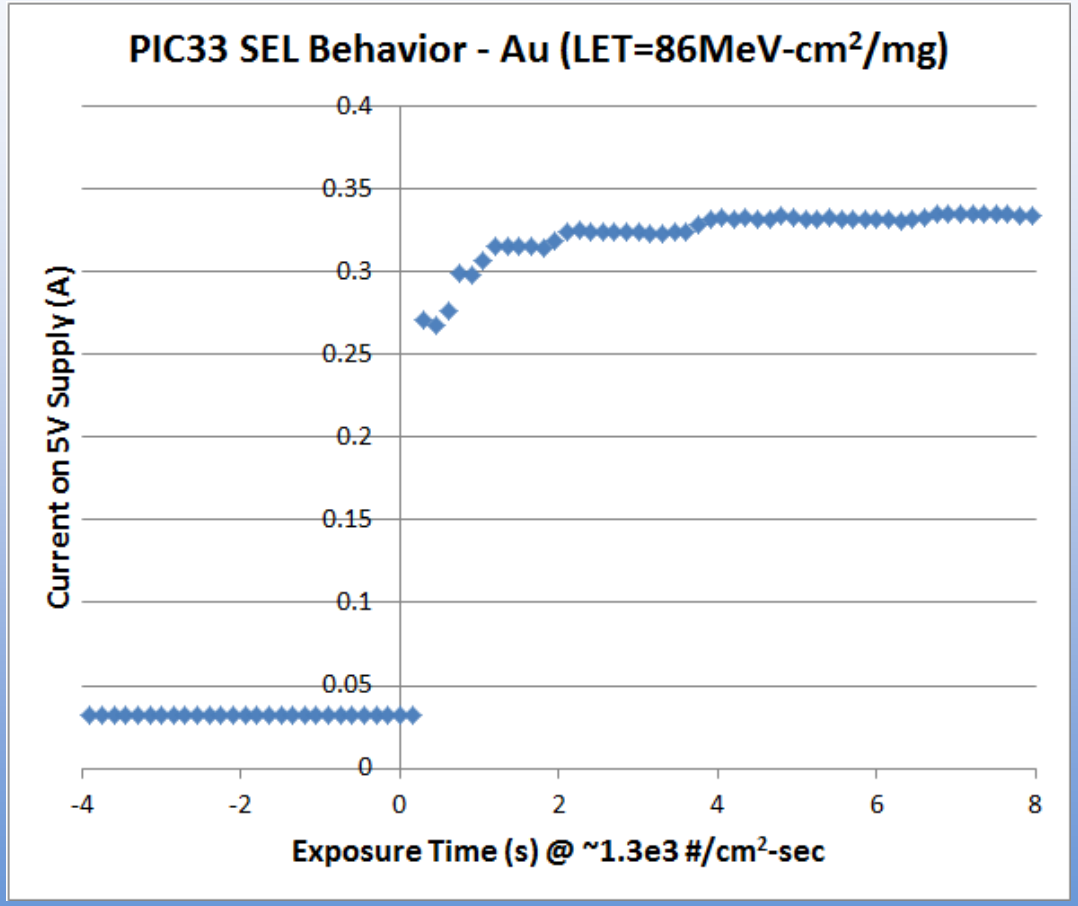


Plug-In-Module
- PIC24
- dsPIC33



SEL Results – PIC33 Current

- 5V supply line increases current very quickly after beam on
- Not recovered by reset
- Similar "current-step" behavior to MSP
- Maximum current appears to be small compared to SEL
  - But still 10x increase

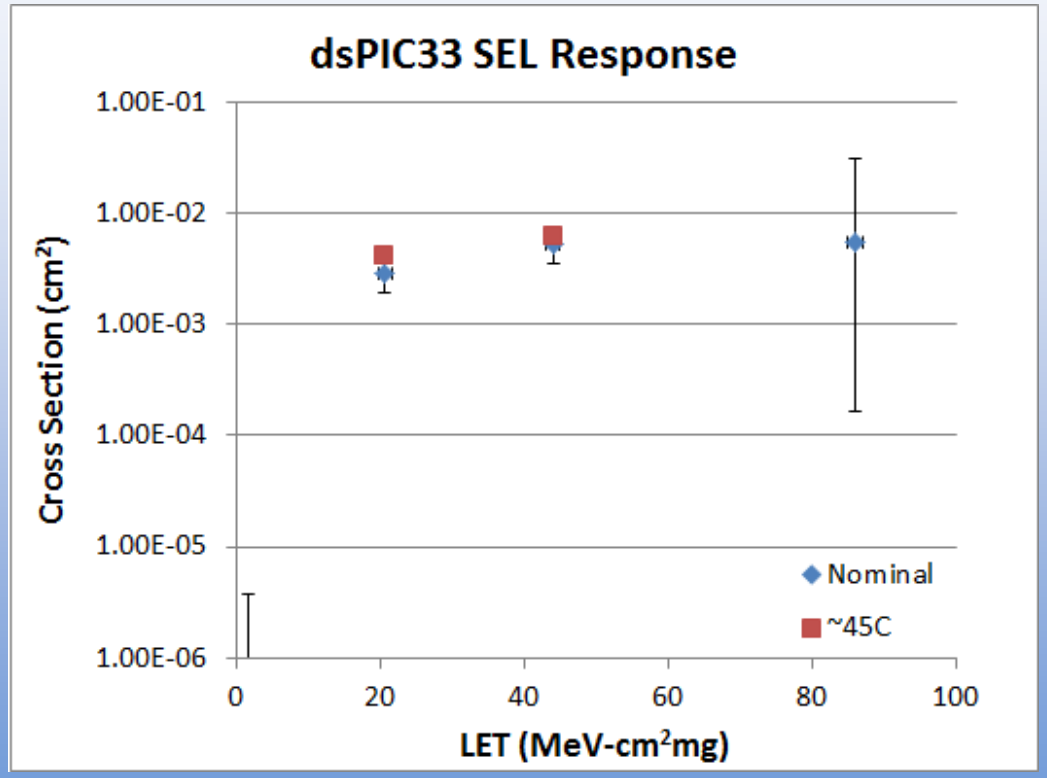


No evidence of damage after exposure to 1e7 #/cm²

SEL Cross Section

- Used 0.25 A as threshold for SEL
- When heated, the SEL current trips protection on the on-board regulation
- Both points (slightly) higher σ for high T

- ISS event rate estimated between 2e-4 and 4e-3/day
  - ~10x higher for GCR



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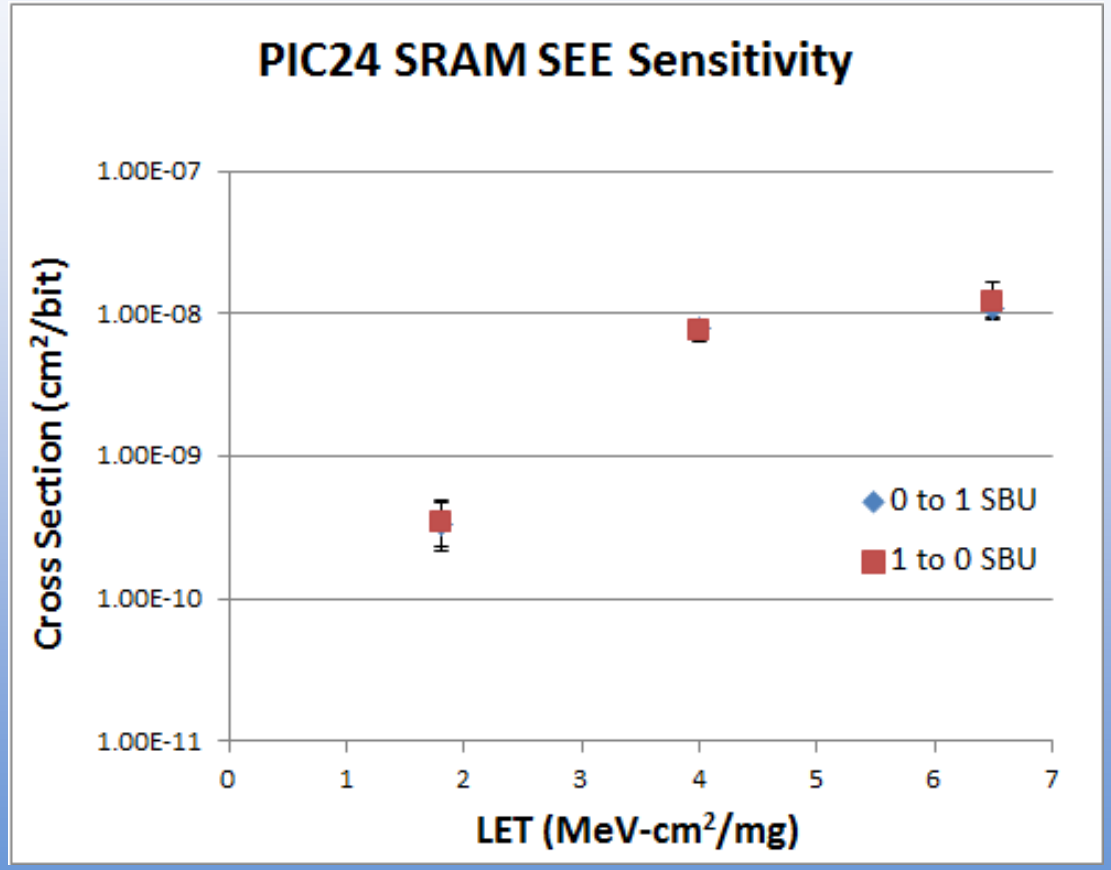
PIC SEE Results



- Low priority compared to SEL efforts
- Flash Results
  - No upsets observed with 6e5 #/cm^2 ions at LET = 86
  - Limiting per-bit cross section of ~6e-12 cm^2/bit
- SRAM Results
  - SEL behavior interfered at higher LETs

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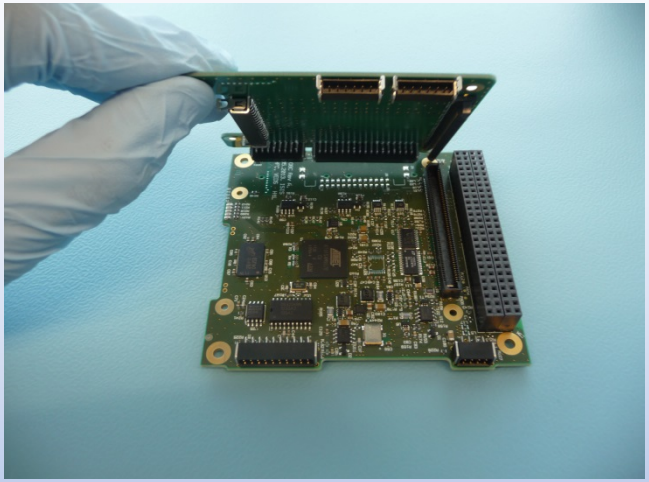
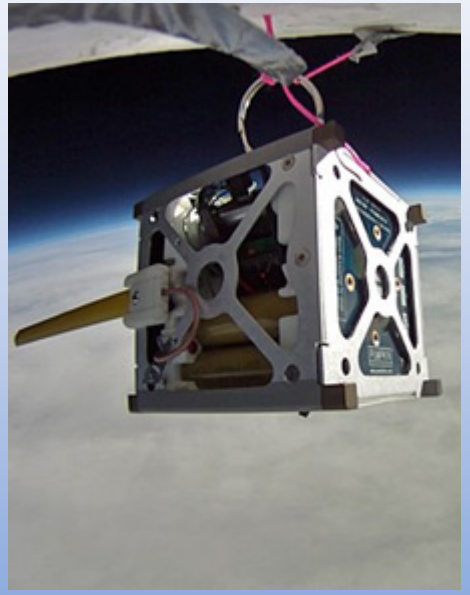


ARM9-based ISIS board

NASA AMES Phonesat



CUBESAT MICROPROCESSORS

To be presented by Steven M. Guertin at the 5th NASA Electronic Parts and Packaging (NEPP) Program Electronic Technology Workshop June 17-19, 2014, NASA GSFC, Greenbelt, MD.

Motivation

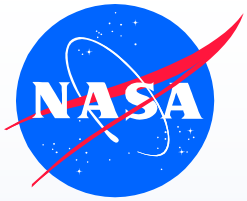
- Various Cubesats have flown with more capable processing
  - Usually C&DH is 8 or 16-bit MCUs, the “ARMs” are actually reduced capability Thumb™ processors
  - AAUSat-3, CANX-2 used a 32-bit ARM processor
  - Phonesat … flew … phones (and newer iterations are flying more)
- Expect that as Cubesat programs continue, need for more processing will be important
- Key drivers – same as for Cubesats in general
  - Small, low power, cheap
  - Generally accessible to low-budget environments (schools, R&D, etc.)

Snapdragon/Atom Effort

- We focused on cell phone processors – primary player is ARM, with Intel trying to get Atom into play
- Avoid issues with closed architecture – i.e. not using Apple A6/A7/etc.
- Most common phone processor in high-end devices is Snapdragon, with Krait CPU (similar to ARM Cortex A15)
  - We are currently looking at Snapdragon 600 and Snapdragon 800 (both TSMC 28 nm – low power)
  - Prototyping equipment readily available
  - Being used in the hobby space

Looking Forward

- SEL of MSP and PIC devices
  - Threshold is not known well enough
  - Given observed sensitivity, threshold region important
- TID of PIC devices
- Testing of AT91SAM9G20
  - May have to wait for next year due to above work
- Testing of Snapdragon 600
  - SEL test at LETs up to 37 (may obtain data at 75, but not considered important to most Cubesats)
  - Limited SEE detection being developed
  - TID Testing (may require well-controlled dose delivery to avoid damage to boards)
- Testing of Atom devices
  - Development effort underway



BACKUP

SEFI in MSP430

- Observed 1 event where test program continued to operate but repeated error pattern observed.
- During runs without power-cycle (no SEL protection)
  - Note observed asymmetry (~4:1) in 1 to 0 vs. 0 to 1 SBUs
- Passes writing all ‘1’s resulted in:
  - 0xfe observed in first 64 even addresses
  - Went away after first few cycles
- SEFI turned into errors in all ‘0’s passes:
  - 0x01 observed in first 64 even addresses
  - Continued through beam-induced reset
- Cross section for this event is about 1e-4cm^2 @ LET 20
- Also observed 1 reset event – same cross section

A Packaging Example

- We are finding some significant problems with some test boards, in terms of preparation for test…

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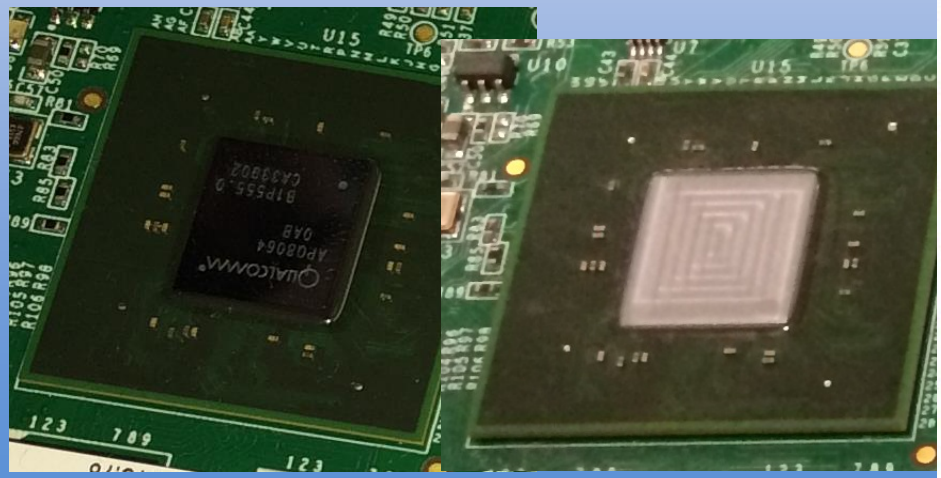
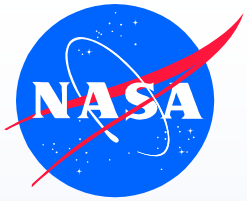
A Packaging Example

- We are finding some significant problems with some test boards, in terms of preparation for test…

Alternate Snapdragon Board

- Another board design – IFC6410 is much easier to work with
- We have established method to thin devices to enable testing with 25 MeV/amu cocktail at TAMU (~100 μm)





SEE Testing of Snapdragon

- Exposed IFC6410 board to Ar @ LET = 7 MeV-cm^2/mg
- Test software was to monitor Android boot
  - Observed through UART error output
  - Provides information about boot behavior for first ~90 seconds
  - Takes ~5 seconds after power up to be activated
  - Provides interrupt/exception reporting
- Total exposure was 3e6 #/cm^2
  - No damage observed
  - No evidence of high current modes (but LET was low)
  - But system had a hard time, and crashed often

- Capture of errors during boot
- LET=6.3, flux ~5e3 #/cm^2
- Using Android boot

- Requires ~10-15 secs of boot to get reports

- Usually fails to reach reportable status

L2 Error

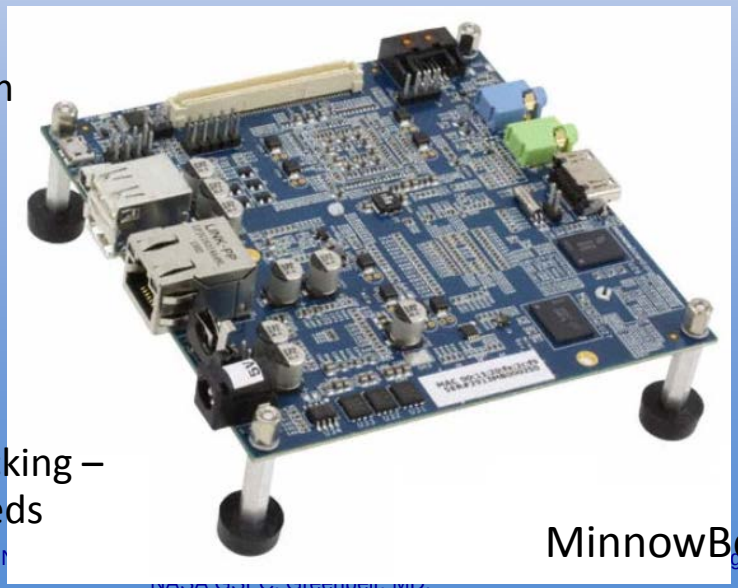
Unspecified Exception

Unspecified Exception

```
[    42.074530] Bluetooth: Tx timer expired
[    42.074530]
[    43.814375] L2 Error detected!
[    43.816419]  L2ESR     = 0x00010010
[    43.819807]  L2ESYNR0  = 0x6200080a
[    43.823195]  L2ESYNR1  = 0x04a4977a
[    43.826583]  L2EAR0    = 0x0002c160
[    43.829971]  L2EAR1    = 0x00000000
[    43.833358]  CPU bitmap = 0x1
[    43.836319] L2 data soft error, single-bit
[    43.840378] Kernel panic - not syncing: L2 single-bit error detected
[    43.846787] [<c0014918>] (unwind_backtrace+0x0/0x11c) from [<c07ba978>] (pani
c+0x84/0x1d4)
[    43.855028] [<c07ba978>] (panic+0x84/0x1d4) from [<c007d7f4>] (msm_l2_erp_irq
+0x1fc/0x260)
[    43.863268] [<c007d7f4>] (msm_l2_erp_irq+0x1fc/0x260) from [<c00d2844>] (hand
le_irq_event_percpu+0xb0/0x290)
[    43.873065] [<c00d2844>] (handle_irq_event_percpu+0xb0/0x290) from [<c00d2a60
>] (handle_irq_event+0x3c/0x5c)
[    43.882862] [<c00d2a60>] (handle_irq_event+0x3c/0x5c) from [<c00d554c>] (hand
le_fasteoi_irq+0xdc/0x148)
[    43.892232] [<c00d554c>] (handle_fasteoi_irq+0xdc/0x148) from [<c00d20a8>] (g
eneric_handle_irq+0x30/0x44)
[    43.901785] [<c00d20a8>] (generic_handle_irq+0x30/0x44) from [<c000ee40>] (ha
ndle_IRQ+0x7c/0xc0)
[    43.910544] [<c000ee40>] (handle_IRQ+0x7c/0xc0) from [<c0008620>] (gic_handle
_irq+0x94/0x110)
[    43.919059] [<c0008620>] (gic_handle_irq+0x94/0x110) from [<c07c8cc0>] (__irq
_svc+0x40/0x70)
[    43.927453] Exception stack(0xc0d05e70 to 0xc0d05eb8)
[    43.932488] 5e60:                                     00000000 c0f3cd00 00000
000 00000000
[    43.940668] 5e80: c0d04000 00000000 00000202 c0d05f28 00000012 fa00300c c0d43
75c 0000000a
[    43.948817] 5ea0: c0d4f080 c0d05eb8 c0087d3c c0087710 20000113 ffffffff
[    43.955440] [<c07c8cc0>] (__irq_svc+0x40/0x70) from [<c0087710>] (__do_softir
q+0x4c/0x248)
[    43.963680] [<c0087710>] (__do_softirq+0x4c/0x248) from [<c0087d3c>] (irq_exi
t+0x48/0xa0)
[    43.971860] [<c0087d3c>] (irq_exit+0x48/0xa0) from [<c000ee44>] (handle_IRQ+0
x80/0xc0)
[    43.979734] [<c000ee44>] (handle_IRQ+0x80/0xc0) from [<c0008620>] (gic_handle
_irq+0x94/0x110)
[    43.988249] [<c0008620>] (gic_handle_irq+0x94/0x110) from [<c07c8cc0>] (__irq
_svc+0x40/0x70)
[    43.996642] Exception stack(0xc0d05f28 to 0xc0d05f70)
[    44.001678] 5f20:                     00000000 00000000 00000001 00000003 00000
003 00000003
[    44.009858] 5f40: c0d65924 00000003 00000000 c0d65924 00000000 00000000 00000
002 c0d05f70
[    44.018007] 5f60: c07c873c c005bf7c 60000013 ffffffff
[    44.023073] [<c07c8cc0>] (__irq_svc+0x40/0x70) from [<c005bf7c>] (msm_cpuidle
_enter+0x70/0x78)
[    44.031680] [<c005bf7c>] (msm_cpuidle_enter+0x70/0x78) from [<c056911c>] (cpu
idle_enter+0x14/0x18)
[    44.040592] [<c056911c>] (cpuidle_enter+0x14/0x18) from [<c0569690>] (cpuidle
_idle_call+0x1e0/0x3c0)
```

Atom Test Devices

- Two types of boards:
  - MinnowBoard
  - Conga board
- Conga boards
  - Use E620 embedded Atom processors
  - 45nm parts
- MinnowBoards
  - Use E640 embedded Atom processors
  - 45nm parts
- Hobbyist Boards
  - Strong community for hacking – will be helpful for test needs



MinnowBoard

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Limitations of Mobile/Cellphone Processor SEE Testing

- Test boards
  - Packaging – can be significant problem with preparation for heavy ions and TID
  - Access to power generation and monitoring of current may be extremely limited
- Software/Operations
  - These are complex SOCs
  - We are targeting SOC test methods, but they may be too complex to evaluate without significant effort