

NASA Electronic Parts and Packaging (NEPP) Program 2017 Electronics Technology Workshop

NEPP Program Task 17-294 Government Working Group

Prepared by MSFC ES43/Patrick McManus
ES43-ESSSA/Kathy Laird
Presented by GSFC 370/Michael Sampson

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I. Acronyms

II. Purpose, Objective, & Scope

III. Major Accomplishments

IV. Current Topics

AD	Analog Devices
AMRDEC	Aviation and Missile Research, Development, and Engineering Center
Au/Sn	Gold/Tin
BeO	Beryllium Oxide
C	Celsius
DLA	Defense Logistics Agency Land and Maritime
DPA	Destructive Physical Analysis
DWV	Dielectric Withstanding Voltage
EP	Engineering Practice
GSFC	Goddard Space Flight Center
GWG	Government Working Group
IGA	Internal Gas Analysis
IR	Infineon International Rectifier
JEDEC	Joint Electronic Device Council
JPL	Jet Propulsion Laboratory
JSC	Johnson Space Center
LaRC	Langley Research Center
MIL-PRF	Military Performance Specification
MIL-STD	Military Standard
MSFC	Marshall Space Flight Center
NEPAG	NASA Electronic Parts Assurance Group
NEPP	NASA Electronics Parts and Packaging
NSWC	Naval Surface Warfare Center
PR	Periodic Requalification
QML	Qualified Manufacturers Listing
R&R	Read and Record
SAE	Society of Automotive Engineers
SEM	Scanning Electron Microscopy
SMC	Space and Missile Center
G11	Component Parts Committee
SMD	Surface Mounted Device or Standard Microcircuit Drawing
SSTC-G12	Solid State Technical Committee
TM	Test Method
Vrms	Volts Root Mean Square
WCCA	Worst Case Circuit Analysis

GWG was established in January 2017

- **Purpose:** To discuss in detail government topics from NEPAG which require additional in-depth technical solutions
- **Objective:** To establish a one-government stance applicable to both terrestrial and space programs
- **Scope:** Attendees represent 5 government agencies and DLA
 - Air Force SMC/The Aerospace Corporation
 - Air Force – Wright-Patterson
 - Army AMRDEC
 - NASA Centers
 - Navy NSWC Crane Division

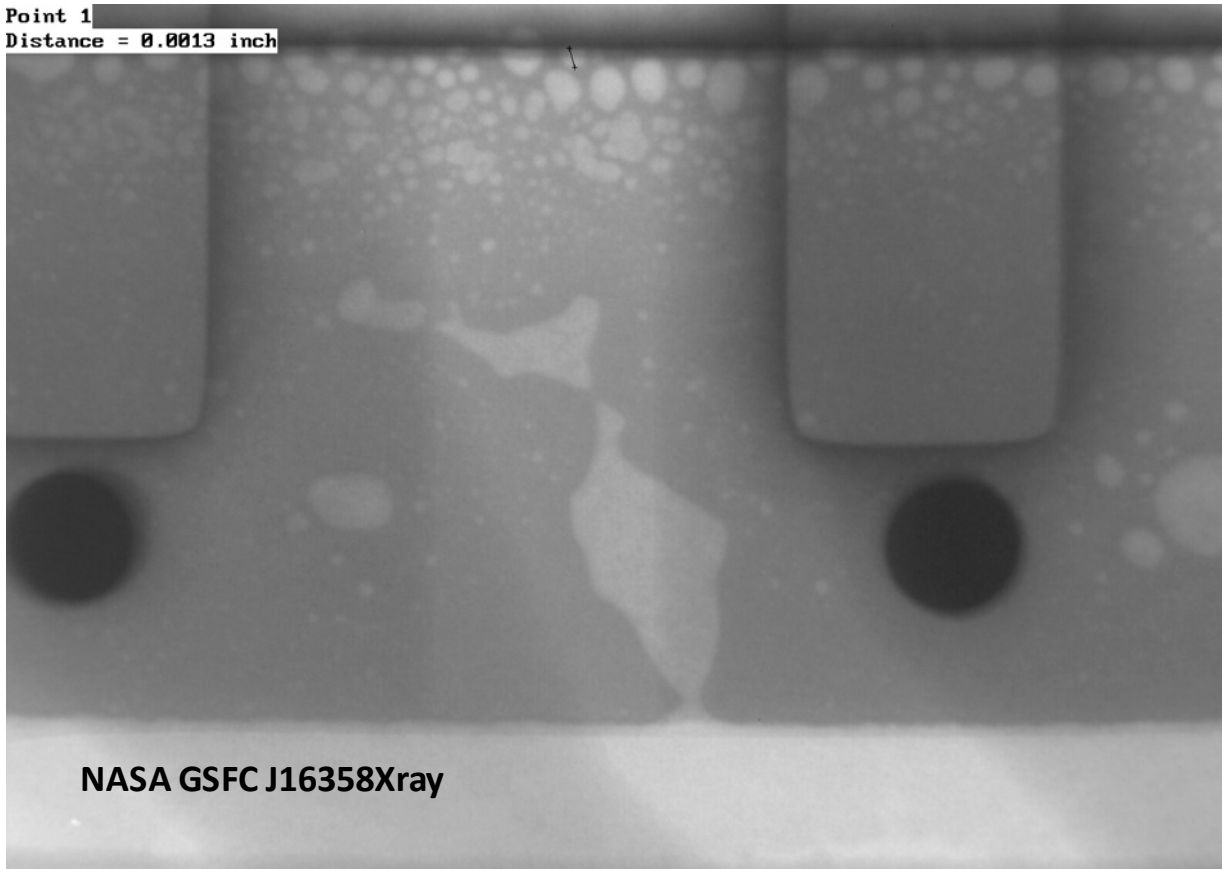
1. Radiography Inspection Criteria

- **Developed a unified government position to address Analog Devices (AD)/Infineon International Rectifier (IR) proposal to reduce the MIL-STD-883 TM2012 X-ray design seal width.**
 - Proposed maximum 75% void criteria be reduced to 5% during October 2016 and January 2017 SSTC-G12/JEDEC task group meetings
 - Change based on X-ray rejects of only 4 part types with Au/Sn solder sealed lids subjected to and passing temp cycling or temp cycling and thermal shock testing
 - AD – Tested four 52-lead ceramic quad flat pack devices
 - 1000 -65/+150C temp cycles followed by leak testing
 - IR – Tested 28 SMD 0.2, 98 SMD 0.5, and 448 UB devices
 - 100 -55/+150C temp cycles, leak testing, 400 -55/150C temp cycles, leak testing, 20 cycles thermal shock, leak seal

Radiography Inspection Criteria (cont.)

X-ray highlighting voids in lid seal solder

Point 1
Distance = 0.0013 inch



NASA GSFC J16358Xray

Radiography Inspection Criteria (cont.)

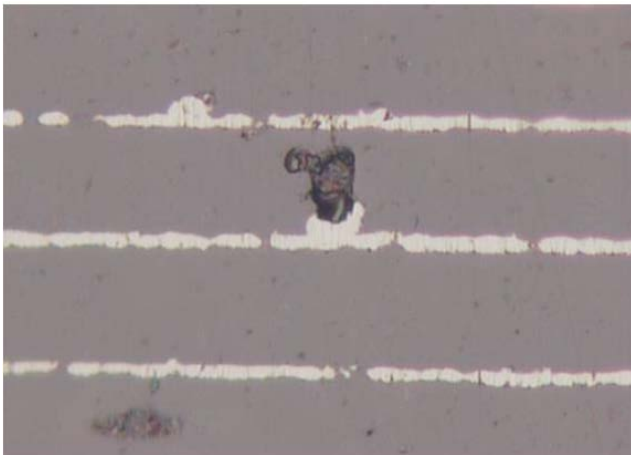
- **Letter signed by all five government agencies, rejecting change, sent to DLA Document Standardization Division and to JEDEC/SSTC-G12 chairs.**
 - Relaxing the criteria from 75% to 95% voiding does not provide confidence in long term reliability
 - Need to maintain process control and to have a robust package seal
 - 95% voiding will reduce manufacturers' continuous improvement efforts to optimize the seal process and could ultimately result in an inferior product
 - AD and IR both admitted operators could not discern 95% voiding
 - 75% voiding criteria has been in both MIL-STD-750 and 883 radiography inspection methods for over 30 years
- Letter equally applies to MIL-STD-750 TM2076.

2. Hybrid Microcircuit Requalification

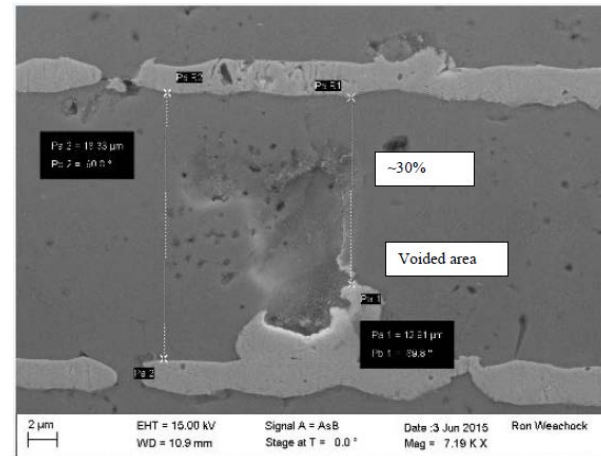
- **JEDEC JC13.5 task group was formed to discuss periodic requalification (PR) requirements for Class H and Class K hybrid microcircuits.**
 - JEDEC task group prepared list of 9 PR requirements
 - GWG agreed to 7 of 9 requirements, including to allow Class H periodic inspection requirements to remain currently as stated in MIL-PRF-38535. Two requirements require further discussion and will be resolved at September 2017 SSTC-G12/JEDEC.
 - GWG recommended a 2-year PR; JEDEC suggested a 5-year PR
 - GWG recommended manufactures qualify the largest and smallest die/substrates and then apply the existing 50% rule to cover die/substrates having dimensions between these two extremes; JEDEC suggested keeping the requirement as currently stated, i.e. the 50% rule without the smallest/largest die/substrates requirement

3. DPA Dielectric Inspection Criteria

- **Draft of MIL-PRF-32535A does not require inspection of voiding or nonuniformities in dielectric layers $< 7\mu\text{m}$.**
- The following change was proposed and accepted
 - A dielectric evaluation method for layers $< 7\mu\text{m}$ was added, which includes using SEM to determine if 50% voiding is a result of manufacturing defects or DPA artifacts.



Optical Microscopy Image of Void in Ceramic Dielectric
Source: NASA GSFC J15135DPA



Scanning Electron Microscope (SEM) Image of Same Void
Source: NASA GSFC J15135DPA

4. MIL-PRF-38534 Rev K Draft Review

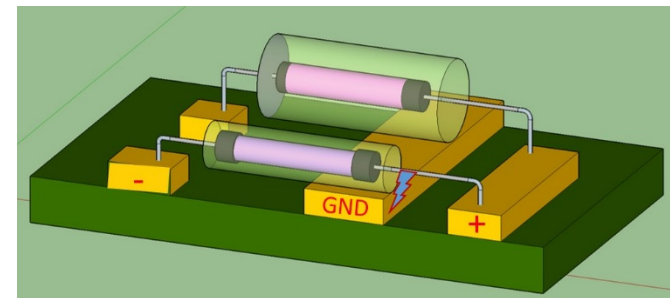
- **Compiled 26 comments and submitted to DLA for review.**
 - 24 comments were resolved and will be incorporated in an updated Rev K draft
 - 2 comments are unresolved and will require further discussion with SSTC-G12, JEDEC, and DLA
 - Current wording allows Group C lot qualification electrical failures to be used for subsequent IGA testing. However, if there are electrical failures, the lot fails and a new qualification lot must be selected.
 - Rev K deletes the requirement for WCCA. Due to hybrid complexity, WCCA is essential to ensure no element is driven beyond its design limit.

NASA GSFC J13016DPA



5. RNR75 Resistor EP Study

- Comments were requested to a DLA EP study proposing a revision of the MIL-PRF-55182 reduced barometric pressure DWV test.
 - Vishay is the sole source manufacturer of RNR75 resistors and experienced barometric pressure DWV corona discharge failures while testing at the required 450 Vrms. Vishay requested to reduce the test voltage to 300 Vrms or to allow the addition of water vapor during the test as means to mitigate test failures.
 - GWG agreed with the recommended option of reducing the test voltage to 300Vrms.
 - GSFC submitted the response to DLA.



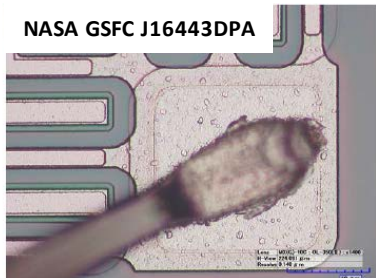
Work in Progress

- **DLA EP Study for MIL-STD-981: Survey on lot control, paragraph 5.6.1.1.1.2 Class S**
 - Should Class S rework allow materials from different LDCs?
- **MIL-STD-883K TM2017: Definition of “Crack:”**
 - A newly added paragraph reads, “Crack is a separation in the mounting material that is measurable in length, width and depth. It is not pullback of the fillet or shrinkage due to the curing process.”
 - Pullback should also be defined
 - The term “crack” is used elsewhere in the TM to describe instances of different failure criteria, i.e. crack in bond wire, crack emanating from mounting holes, and crack in solder joint. The new definition does not apply in these cases.

Work in Progress (cont.)

- **MIL-PRF-19500 Major Change Definitions and Required Notification**
 - During a DLA M19500 manufacturer audit, an auditor noted a major change was made to the bond wire process step. DLA was not notified.
 - M19500 adequately defines major changes and required requalification testing. A bond wire process change is listed as a major change but M19500 does not specifically state manufacturer is to notify DLA of major changes.
 - In this case, manufacturer had performed all required requalification, but did not notify or provide data to DLA.

NASA GSFC J16443DPA



(Continued on next page)

Work in Progress (cont.)

- **MIL-PRF-19500 Major Change Definitions and Required Notification (cont.)**
- **MIL-PRF-38534 and MIL-PRF-38535 were reviewed to determine if there were similar issues**
 - Major change specifications in M38534 are acceptable as written
 - Major change specifications in M38535 need to be revised
 - “Class 1 changes” are defined in A.3.4.2 but specific details not given in a table. Unclear if Class 1 changes are major changes, which are well defined in Table A-I along with required requalification testing.
 - Notification of Class 1 changes are to the acquiring activity, not the qualifying activity
 - Notification of major changes is not specified, but qualifying activity should be specified both in A.3.4.2 and as a note to Table A-I

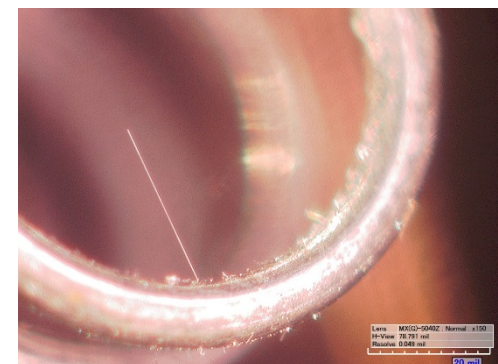
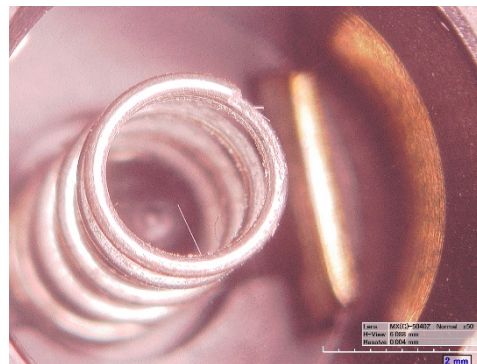
Work in Progress (cont.)

- **Lack of BeO Marking Requirements in Attenuator Specifications (e.g. 3933)**
 - Packages of parts containing BeO must be marked as such due to safety hazards
- **Read and Record Data for QML Microcircuits**
 - MIL-STD-38535 states R&R data is required on delta parameters when specified in the SMD
 - Unclear whether R&R data is only required for space level parts
 - SMDs vary widely in number of deltas measured
 - Recommend M38535 use JEP-163 to call out minimum required parameters
 - Data retention is specified as 5 years, which is not sufficient for many space programs; recommend extending to 15 years
 - JEDEC has open action to address this issue

Work in Progress (cont.)

- **Concerns with Use of Lead Free Solder in Military Standards**
 - Since the 1990s, majority of MIL EEE parts specs have contained some form of prohibition on tin-based surface finishes unless they contain a minimum of 3% lead (Pb) by weight.
 - To address 'heritage' use of Pb-free materials in military specifications prior to 1990, such as MIL-PRF-23419 (fuse cartridge), DLA permitted the use of Pb-free solder "with the approval of the qualifying activity" where factors such as 'heritage design' and history of reliable performance could be used.
 - DLA has been periodically amending MIL specs to add the "with qualifying activity approval" language whenever it is learned that a heritage design has been affected by Pb-free prohibitions
 - GWG wants to understand what factors the qualifying activity has considered with this type of allowance and whether or not the information is available to the user community.

**Tin Whiskers on Tin-Plated Iron Alloy Springs
Used in Pushbutton Switches
Courtesy NASA GSFC Code 562**



Work in Progress (cont.)

- **Chip Capacitor Wall Thickness**

- MIL-PRF-55365 for tantalum chip capacitors specifies a minimum wall thickness of 1 mil for T level capacitors
- GWG has concerns that known failures may be the result of a thin wall thickness. GWG members are researching failures to determine if thin walls are a contributing factor.

CWR29 capacitor case cracked due to thermal overstress during rework to remove/replace adjacent component.
Case Wall Minimum Thickness ~ 3 to 4 mils

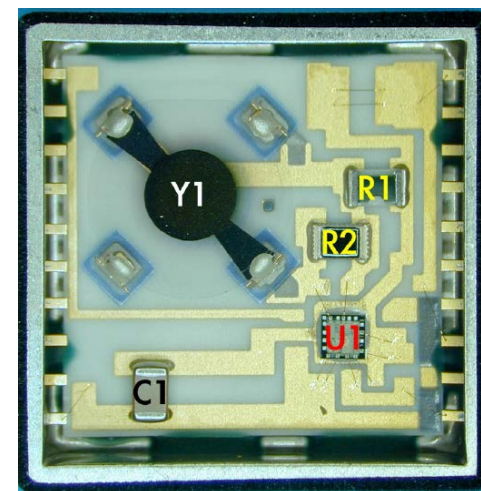


Images Courtesy of NASA GSFC Code 562

Work in Progress (cont.)

• MIL-PRF-55310 QPL Oscillator Specification

- Slash sheets for TCXO, OCXO, and OCVCXO type oscillators are inactive and there have never been slash sheets for VCXO, TCVCXO, MCXO, and RbXO type oscillators.
- DLA plans to conduct an EP Study to determine from the QPL suppliers:
 - What products they are providing to military and space customers for which there are no active slash sheets and
 - What screening/qualification test flows they are using?
- GWG will ask G11 to form a new task group to update M55310.



Questions?

Contact Information:

- Patrick.D.McManus@nasa.gov
- Jeffrey.H.Sokol@aero.org

