

Trigger & Data Flow Preliminary Design Review August 16, 2001

Mission Assurance

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<u>General</u>

- The Trigger & Data Flow (T&DF) S&MA program will be conducted in accordance with LAT PAIP, LAT-MD-00039-1.
- Quality is achieved through empowering employees, emphasizing teamwork, continuous improvement (relentless) and through sound scientific approaches to characterizing the flight hardware.
- Lessons learned from other programs will be utilized.
- The implementation relies on the controlled application of procedures, instructions and integrated product teams
- Success of the program is dependent on:
 - Highly skilled design team, QA, EEE, Electronic packaging engineer with knowledge in a wide variety of areas.
 - Commands respect for technical knowledge/experience.
 - Be multifaceted (knows materials, metallurgy, manufacturing, mechanics, etc.)
 - Design T&DF specifications the first time.
 - Build test and validate hardware to specification the first time.

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Quality Assurance Control Flow Diagram





EEE Parts Program

- EEE Part Program Control Plan LAT-MD-00099-02 implemented.
- T&DF design engineers are using Quality Level 2 parts per GSFC-311-INST-001 which governs the selection, screening, and qualification processes.
- Parts selection process will utilize the NASA Parts Selection List (NPSL), MIL-STD-975, GSFC PPL-21, and DESC QML P/N.
- All EEE parts will be derated in accordance with PPL-21 and stress analysis will be performed to compare against the nominal stress derating criteria.
- PCB will verify that all parts meet requirements of radiation, parts heritage, quality level, specifications, upscreens, DPA, other tests, and source inspections.
- Component / Subsystem / System Engineers will generate parts list and submit to PCB for approval. Separate list for parts, materials and processes will be prepared.
- At present, focusing on the long lead active non-QML parts, including ASIC, 3.3V DAC, 3.3V ADC, Qualification and Screening plan
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Material, EEE Packaging and Processes Program

- Implemented a materials and processes program as per LAT-SS-00107-1, LAT Mechanical Parts Plan.
- Materials planned to be used will conform to 1.0% Total Mass Loss (TML) and 0.1% Vacuum Condensed Material (VCM) per NASA Specification.
- Manufacturing, Assembly, and Quality Control of Electronic System will be in compliance to NASA-STD-8739.1, NASA-STD-8739.2, NASA-STD-8739.3, NASA-STD-8739.4, NASA-STD-8739.7
- PWBs will be manufactured and tested as per IPC-2221, IPC-6012 & IPC-6012, IPC-2223 Rigid and Flexible
- PWB coupons will be evaluated prior to flight.

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EEE Parts, Materials, & Processes Overarching View



* Manufacturing Failure Modes & Effects Analysis (FMEA) relies upon effective EEE, M&P Program.

** Areas successfully being addressed today.

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QUALIFICATION AND VALIDATION OF PLASTIC August 16, 2001 ENCAPSULATED MICROCIRCUITS (PEMs) DAC, ADC and ASICs



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GLAST LAT Project Trigger & Data Flow Preliminary Design Review PLASTIC ENCAPSULATED MICROCIRCUITS (PEMs) SCREENING (100%) DAC, ADC, and ASICs



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ASIC Part Evaluation



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ASIC Part Evaluation continued





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Design Verification

- Design verification facilitate effective communication of concepts.
- Design validation and verification occurs very early.





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Risk Management Process and Data Flow



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Manufacturing Flow Diagram of PWB Assembly



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Manufacturing Flow Diagram of PWB Assembly





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System Safety Program

- The T&DF safety program will be in accordance with the LAT System Safety Program Plan, LAT-MD-00078-01.
- Will support GSFC for assessment of orbital debris and acceptable level of risk.
- Will perform hazard analysis and risk mitigation.
- Will identify and control hazards to personnel, facilities, support equipment, and flight hardware during all stages.

Contamination Control

- Contamination control program will be implemented as per LAT-MD-00228-D.
- Fabrication and integration of the T&DF Subsystem components will occur in a minimum of class 100,000.
- Will review all manufacturing and integration processes for contamination hazards.
- Will take protective measures necessary to prevent contamination especially during I&T and environmental testing.
- Surface cleanliness verification of fight hardware by optical witness samples, particle fallout plates, tape lifts, and/or NVR Rinses/Swabs

Integration Readiness Review Checklist

- Verify that all Cert Logs, PRs, Material Review Board (MRB) reports, drawings, logbooks, etc. are completed & reviewed by QA.
- Subsystem/component test plan completed
- Review of special handling requirements
- ESD, cleaning, pre-integration checkout, temperature, humidity, etc.
- Walk-through of the integration flow
- Functional test script completed
- GSE in-place or available
- Precursor activities identified & completed (thermal preps, other supporting systems, etc.)
- Work Order Authorization form filled out and approved
- Mechanical Integration Procedure ready
- Contamination Control Plan for the item completed
- Electrical Integration/safe-to-mate procedure ready
- All supporting software (flight and test) complete and tested
- Functional test procedures complete and tested

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