Single Event Effect Characteristics of CMOS Devices Employing Various Epi-layer Thicknesses

Kenneth A. LaBel, Donald K. Hawkins
NASA/GSFC
Code 735.1
Greenbelt, MD 20771

James A. Kinnison
The Johns Hopkins University/Applied Physics Laboratory

William P. Stapor
Naval Research Laboratory

Paul W. Marshall
Independent Consultant

Abstract

Latchup resistant process, combined with SEU mitigation circuitry, may provide sufficient protection for many satellite applications. We report proton and heavy ion cross section measurements to illustrate the epitaxial layer thickness dependence on a First-in, First-out (FIFO) memory and microprocessor devices fabricated in a commercial CMOS/EPI process.

I. INTRODUCTION

Complementary Metal Oxide Semiconductor (CMOS) devices have a long history of being susceptible to single event effects (SEE). This includes not only cell error events like single event upset (SEU), but also destructive conditions such as single event latchup (SEL). SEL, in particular, is acknowledged as being a major concern to spaceflight electronic designers leading to potential mission failure. SEU, while also being of concern to spacecraft designers, has multiple potential mitigation techniques that aid device usability [1].

Latchup mechanisms in CMOS processes are fairly well understood [2], and the literature has many examples showing susceptibility in both bulk and epitaxial layer processes [3]. The parasitic n-p-n-p pathways are particularly troublesome in bulk CMOS processes and in thick epitaxial (epi) processes involving n-well transistors. One such example is the Integrated Device Technologies' (IDT) proprietary CEMOS-5 process investigated in this study which utilizes a standard12 micron epi-layer. This "radiation-enhanced" or RE process is a twin-well, dry-etched, stepper-aligned process with a minimum feature size of 1 μm and a minimum effective channel length of 0.6 μm. As was shown in [4], the latchup sensitivity of this process is highly dependent on the depth at which charge is deposited. By varying the particle range to examine this sensitivity, Levinson, et al. examined two latchup paths in the IDT process and mapped out the sharp latch up cross section dependence on the ion penetration depth for distances below 15 microns.

Methods certainly do exist to insure latchup-free parts, but these typically involve additional structural and processing related steps which may not be compatible with low cost or high performance [5]. In this study we explore, with quantitative cross section measurements of proton and heavy ion SEU and SEL, the dependance on the thickness of the epi-layer (resistivity of the material was unknown). The expectation of such a dependance is strongly suggested in the findings of [2-4], and based on the expected latchup benefits. IDT has fabricated two different test devices in which the epi-layer thickness is systematically varied from 6 to 12 microns. For convenience, we shall note these devices as being fabricated on a "split-epi" process.

II. TEST DEVICE DESCRIPTION

The 7201T is a parallel architecture, cascadeable FIFO, typically used by spacecraft designers as a data buffering device. This FIFO allows asynchronous read and write operations and has several status flags (device full, empty, and half-full) available for user monitoring. The device may be run statically up to a 33MHz access frequency [6].

The 3081 is a highly-integrated, high-performance, Reduced Instruction Set Computer (RISC). This RISC is based on the highly-successful, commercial R3000 instruction set family. The 3081 includes a R3000A-compatible central processing unit (CPU), floating point accelerator, instruction and data caches, plus system control logic (i.e., memory arbiters, etc...). The device is capable of operating at clock speeds of 40 MHz [7].

Relevant device characteristics are shown in Table 1.

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Part #	Description	Date Code	Epi thickness in μm
7201T	512x9 FIFO	JEG8334	6
		JEG8339	8
		JEG4333	10
		JEG8335	12
79R3081 (3081)	32-bit RISC Microprocessor	JEG8379	6
		JEG8378	8
		JEG8380	10
		JEG8377	12

Table 1. Device characteristics

III. TYPES of SEUs - FIFO

In addition to SEL, three types of SEUs may be apparent in FIFO devices: single bit errors, multiple bit errors, and control (or pointer) errors. Single bit errors are the traditional SEU event in which a single ion passage causes a single bit to change state or flip. If that single ion causes multiple bits to flip in adjacent cells, then a multiple bit upset occurs. Note that a multiple upset is only of concern to electronics designers if the adjacent memory cells that flip are in the same logical word since single bit error detection and correction (EDAC) codes can easily handle this[6]. Lastly, control errors are those SEUs that cause operational difficulties in the device such as reading or writing to the incorrect address or the occurrence of a functional halt. Often, a cycling of device input power (power reset) must be provided to clear this error.

IV. TEST FACILITIES

A. *Heavy Ion Test Facility*

The test facility used was the Brookhaven National Laboratories (BNL) Single Event Upset Test Facility (SEUTF). This setup utilizes a dual Tandem Van De Graaff accelerator suitable for providing ions and energies for SEU testing. The test devices are mounted on a device-under-test (DUT) board inside a vacuum chamber. All devices were delidded for heavy ion testing in order to accommodate beam penetration limits.

The SEUTF uses a computer-driven monitor and control program to provide a user-friendly interface for running the experiments. Hard copies and computer floppy disks of the test data and graphs are made available.

Table 2 represents the ions utilized for testing.

Ion	Atomic Number	Energy in MeV	LET in MeV*cm^2/mg*
F	19	140	3.36
Cl	35	195	11.8
Ni	58	262	26.6
I	127	305	59.6
Au	197	329	81.2

* = at normal incidence

Table 2. Ions used at BNL

Additional effective LET values in Si were attained by varying the angle of incidence of the ion beam to the device. All LETs discussed are in units of MeV*cm^2/mg.

B. *Proton Test Facility*

The test facility used was the University of California at Davis Cyclotron facility. Maximum energy at the facility is 63 MeV. The energies listed in the next sections are those incident on the device or device package.

V. TEST METHODS

For the 7201T FIFO, typical operating currents for the devices under test (DUTs) were 13 mA with a maximum (or SEL) current set to 28 mA. All devices were tested in a dynamic mode of operation (as per project-specific requirements). The testing was performed using an all logical high (ones) data pattern with alternating Read/Writes at a 50% duty cycle. Device operation was nominally at 1 MHz. An SEU was defined as a non-compare of the data between test device and reference data. Collected test data was then analyzed further to determine control errors.

The 3081 RISC microprocessor, however, was tested for SEL only. Testing was performed on a biased and clocked device.

Two to three device samples of each epi-thickness were tested. This is a compromise between test costs and statistical results.

It should also be noted that all tests were performed at room temperature. As has been observed throughout the radiation effects community, SEE results may vary based on temperature. For SEL, in particular, lower a LET_{th} and higher device cross-section is common.

VI. HEAVY ION SEL TEST RESULTS

The primary goal of our tests was to study the variability of SEL sensitivity with the differing epi-layer thicknesses. Figure 1 illustrates the test results for the FIFO; Figure 2 for the microprocessor.

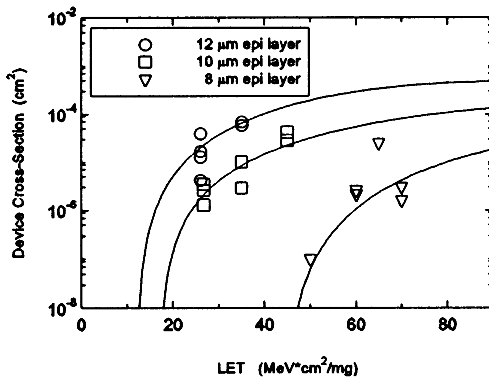

Figure 1 7201T SEL Results with Weibull Fit

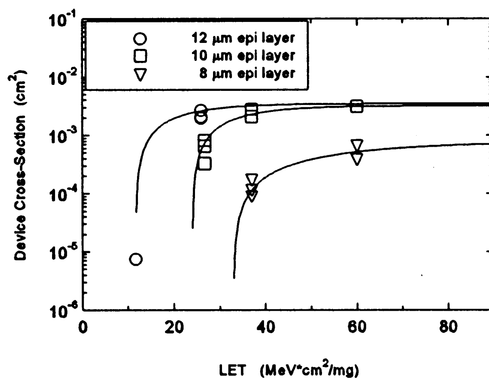

Figure 2 3081 SEL Results and Weibull Fit

Equation (1) represents the standard Weibull equation utilized to fit the experimental data.

$$\sigma(LET) = \left[1 - e^{-\left(\frac{LET-a}{b}\right)^{c}}\right]\sigma_{sat} \quad (1)$$

The dataset for the FIFO test, as provided by NASA/GSFC, the SEL susceptibility decreased as the epi-layer thickness decreased. No SEL was observed on the 6 μm devices even though greater than 1E7 particles/cm^2 were incident with an LET of 81.1. Table 3 summarizes the results observed and Weibull parameters to fit the data. As may be noticed, the SEL LET_{th} increased while the device cross section decreased as the device epi-layer thickness increased.

For the dataset for the microprocessor test, as provided by NRL, the SEL susceptibility also decreased as the epi-layer decreased. No latchup was observed on the 6 μm device. Table 4 summarizes the results observed and Weibull fits to the data. A similiar relationship, as observed by the FIFO, between LET_{th}, device cross section, and epi-thickness is noted.

It should be noted that Weibull plots, while not usually utilized for SEL, appear to provide a relatively "good fit" to the data and hence are provided for convenience. The plots, herein, would also find a better Weibull fit with an extension of experimental data.

VII. FIFO HEAVY ION SEU TEST RESULTS

All test samples were susceptible to SEUs. The single bit SEU LET_{th} for the 6 μm epi thickness FIFO was less than 3.5 with a saturation device cross-section of 3E-3cm^2. Figure 3 illustrates this test data along with the data points taken for the 8 and 10 μm epi thicknesses. No LET_{th} or saturation cross section were determined for the other epi-thickness devices either due to the occurrence of SEL or mission-specific test criteria..

Sporadic multiple bit and control errors were seen periodically throughout the testing. It is thought that since these are simply a special-case type of SEU, their test results are extremely dependent on such items as the number of cells, layout, and design rules as compared to the memory storage cells within the same device. In particular, multiple bit upsets normally require that the adjacent cells be mapped to the same logical address. SEU LET_{th} for control SEUs was approximately 20. Because of the relative randomness of occurrence, no statistically significant cross sections were determined.

As can be noted in Figure 3, there appears to be no statistically significant variance between device SEU cross sections and the associated epi thicknesses. This, however, may be limited to the number of test samples utilized and test runs performed (cost and time constraints). More detailed SEU testing would be needed to provide more thorough results.

VIII. FIFO PROTON TEST RESULTS

Testing was performed on the 6 μm test samples only, using a monoenergetic proton beam. Both lidded and delidded device samples were tested. With 63 MeV protons, the measured device error cross section was 3E-11cm^2 on average with a variance of less than a factor of two between samples (lidded or delidded). No proton-induced SEL was observed.

EPI Depth µm	Measured LET_{th} MeV*cm^2/mg	Measured $_{sat}$ (cm^2)	Weibull LET_{th} MeV*cm^2/mg	Weibull $_{sat}$ (cm^2)	Weibull scale/shape -b- and -c-
6	> 81	$< 10^{-7}$	-	-	-
8	50-60	3×10^{-6}	44	5×10^{-6}	60 / 2.9
10	< 26.6	$> 4 \times 10^{-5}$	17	1.4×10^{-4}	70 / 2.5
12	< 26.6	$> 6.5 \times 10^{-5}$	11	3.5×10^{-4}	50 / 2.5

Table 3: IDT 7201T SEL Results

EPI Depth µm	Measured LET_{th} MeV*cm^2/mg	Measured $_{sat}$ (cm^2)	Weibull LET_{th} MeV*cm^2/mg	Weibull $_{sat}$ (cm^2)	Weibull scale/shape -b- and -c-
6	> 59.7	$< 2 \times 10^{-5}$	-	-	-
8	26.5-37.1	3×10^{-6}	33	8×10^{-4}	25.6 / 1
10	< 26.5	$> 4 \times 10^{-5}$	24	3.2×10^{-3}	10.3 / 1
12	12	$> 6.5 \times 10^{-5}$	12	3.5×10^{-3}	10.3 / 1

Table 4. IDT 3081 SEL Results

Total Dose in kRad (Si)	Icc in mA
0	12
54	15
81	21
108	27

Table 5. IDT 7201T FIFO Proton Total Dose Results

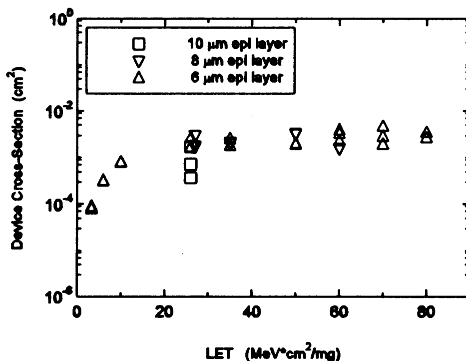

Figure 3 7201T SEU Results

Proton SEU testing also provides an opportunity to gather total dose degradation information. Though no constraints were placed on the test with respect to dose rate, we note that greater than 100 kRad (Si) dose was delivered incrementally at less than 100 rads/sec over the course of several hours. Table 5 shows device current consumption in normal operating mode versus proton doses.

IX. Discussion

It is interesting to note that two separate devices fabricated in the split-epi lot were aided by the reduction in epi-layer thickness from SEL concerns. As the epi-layer became thinner, the device became less susceptible to SEL through both a reduction in asymptotic cross section and an increase in LET_{th}. In both device types, SEL was not seen with a 6 μm epi thickness. This leads to further discussion in several areas.

First, even though the process was the same, the results for the two device types had some variance (SEL LET_{th}s for instance). Other device design characteristics influence this. Items such as material resistivity, device geometry and layout, contact characteristics, etc... may bias the device SEL response. Thus, simply thinning or adding an epi-layer on an existing process may not always mitigate SEL effects

It is also important to note that these devices were commercial devices, not military-screened versions with strict process controls. Results, therefore, may vary from lot-to-lot within the same device type. Thus, lot screening is recommended on such devices if they are to be used in spacecraft.

Data has been reported on other FIFO devices on IDT's standard RE process (12 μm epi) as well as on non-epi IDT devices [8]. The SEU results correlate well with those presented here: little observable difference exists between device types with differing thickness (or no) epi-layers. SEL results are consistent as well: the thinner the epi-layer, the more promising the results.

X. IMPLICATIONS

The SEE testing of these devices was performed in support of spacecraft programs. This has unique connotations: spacecraft designers realistically care only whether they may use a device or if there are any constraints on usage.

Relevant to design constraints is the architecture of a device. The 7201T FIFOs are 9-bit wide ICs. The typical design usage is to utilize 8-bit (or byte) wide paths (or multiple 8-bit wide paths). Thus for most design applications, the ninth bit may be used for parity. This enables detection of single bit errors, the most prevalent SEU characteristic of these parts. If the designer is able to accept the spurious SEU, then the 6 μm device (no SEL observed) may be acceptable for his or her application. This must be judged on a case-by-case basis.

Even though full SEU characterization was not presented herein on the 3081 microprocessor, one would expect SEUs to occur in this device based on the 7201T FIFO data. Again, if the spacecraft design utilizes mitigation techniques as described in [1], devices may have a potential usage in spaceflight.

For reference, SEL rates were calculated for the 3081 SEL results. Table 6 presents a summary of SEL rates.

Epi-layer thickness in μm	SEL rate (average time/event/device), Geosynchronous orbit (Solar Min), 20 mils Al shielding, 1 latchup every ... days
12	211
10	661
8	6950
6	6630 years (assuming SEL at worst case test parameters)

Table 6. 3081 SEL Rates

It is clear that the thinner epi-layer has distinct advantages for SEL properties.

XI. CONCLUSION

We have presented a set of data concerning the SEE effects on CMOS devices utilizing various thickness epi-layers. The SEL results show a clear improvement with decreasing thickness. This knowledge may have a definitive use in applying commercial devices to spacecraft programs.

In particular, data was presented on the same device with only varying epi thickness. The implication is clear; a reduced epi thickness in a commercial device is capable of reducing the risk of SEL.

XII. REFERENCES

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