Radiation Effects on Current Field Programmable Technologies

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Summary

I. Scope of Presentation

II. Device Categories

III. Radiation Performance
   A. Configuration Technologies
   B. Fabrication Considerations
   C. Design
   D. Architectural Features

IV. Conclusion
Basic Architecture

A Sea of Gates Architecture
Has the Routing Network
Above The Logic Array

Channeled FPGA Architecture

Atmel Architecture - Lowest Level

Actel Architecture
Device Categories

- Programmable Substrate
- PLD/CPLD
- Field Programmable Gate Arrays
  - SRAM
  - Non-Volatile
  - Antifuse
    - Amorphous Silicon
    - Dielectric
- LPGA/One-Mask
- Mask-Programmed ASIC
SER - Single Event Reprogramming

SER Cross Section detected by function failure. This curve serves as a lower bound.
### FPGA Configuration Memory

<table>
<thead>
<tr>
<th>Device Class</th>
<th>User Flip-Flops</th>
</tr>
</thead>
<tbody>
<tr>
<td>A14100A</td>
<td>905</td>
</tr>
<tr>
<td>AT6010</td>
<td>131,000</td>
</tr>
<tr>
<td>XC4020</td>
<td>329,000</td>
</tr>
<tr>
<td>XC6216</td>
<td>173,000</td>
</tr>
<tr>
<td>2C26</td>
<td>274,000</td>
</tr>
</tbody>
</table>

- This Device Class Typically Has 1-2,000 User Flip-Flops
- Configuration Memory Increases SEU Cross Section By ~ 2 Orders of Magnitude

- Hardwired Off (MODE PIN)
Antifuse Radiation Effects

- Unprogrammed Reliability is the Key Concern
  - Both Dielectric and Amorphous Silicon Can be Damaged

- Manufacturers: Actel, L-M, Pico Systems, Quick Logic, UTMC

- Circuits and Instrumentation Techniques for Characterization

- Investigated Failure Thresholds and Cross Sections
  - Improvements in Antifuse Design
  - Effects of Materials

- Failure Analysis Techniques and Results
Switch Technology

ONO Antifuse
Poly/ONO/N++
Heavy as doped Poly/N++
Thickness controlled by CVD nitride
Programs ~ 18V
Typical Toxono ~ 85 Å
RH1280 Toxono = 99 Å
R = 200 - 500 ohms

TD Amorphous Silicon Antifuse
‘Pancake’ Stack Between Metal 2 and 3
Designed for 3.6V Operation in Sea Of Gates FPGA

‘Logic’ Devices Program at ~ 10V
‘Substrate’ Devices Program at ~ 30V
Thickness ~ 500 - 1000 Å
R = 20 - 100 ohms
Antifuse Failure Thresholds

Antifuse Threshold Voltage

Antifuse Electric Field Strength

Two processes were used for this 3.3 V device:
Process 1 failed immediately @ 3.3 VDC
Process 2 didn't fail @ 4.0 VDC

- A1230A (87 A)
- RH1020 (96A)
- RH1280 (99A)
- Pico-amorphous (500A)
- TD-amorphous (1000A)
- SiO₂ - reference
Dielectric Antifuse Cross Sections

ONO Antifuse Testing with Iodine (LET=60)
Bias = 5.5 VDC
Normal Incidence

Fluence (ions/cm$^2$)

$I_{cc}$ (mA)

0 200x10$^3$ 400x10$^3$ 600x10$^3$ 800x10$^3$ 1x10$^6$

A1280A @ 87 A
RH1020 @ 96 A
RH1280 @ 99 A
## Latchup Performance

<table>
<thead>
<tr>
<th>Latched</th>
<th>Not Latched</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1020B/TI</td>
<td>RH1020</td>
</tr>
<tr>
<td>🌟 A1020B/MEC</td>
<td>A1280XL (0.6, 0.8)</td>
</tr>
<tr>
<td>A32200DX</td>
<td>A32140DX</td>
</tr>
<tr>
<td>AT6002</td>
<td>A1460A, A14100A</td>
</tr>
<tr>
<td>QYH580 @ 5.5V</td>
<td>QYH580 @ 3.6V</td>
</tr>
<tr>
<td>GF10009K</td>
<td>CLAy-31</td>
</tr>
<tr>
<td>2C40</td>
<td>KJ911</td>
</tr>
<tr>
<td>pASIC 1</td>
<td>MKJ911</td>
</tr>
<tr>
<td>XC3090</td>
<td></td>
</tr>
</tbody>
</table>

- Latched devices have latchup performance values.
- Not Latched devices do not have latchup performance values.

*Note: The table entries represent specific latchup performance values for certain devices.*
Latchup Susceptibilities - Bulk

- 0.8 um Bulk Process
- High Latchup Threshold @ 5.0 V
- No Latchup Detected @ 3.6 V

QYH580 Latchup Data (S/Ns 1, 3, 4)

- LET (MeV·cm$^2$/mg)
- X-Section (sq. cm)
- $V_{CC} = 3.3$ V
- $V_{CC} = 3.6$ V
- $V_{CC} = 5.0$ V

Plot:
- X-Axis: LET (MeV·cm$^2$/mg)
- Y-Axis: X-Section (sq. cm)
- Different markers for different $V_{CC}$ values

Graph shows the latchup data with the specified threshold and absence of latchup at a lower voltage.
Latchup Susceptibilities - EPI

A3200DX Latchup Data

A32200DX Readily Latches
A32140DX No Latchup

0.6 um Epi Process
Epi Thickness: 8.5 - 9.0 um
For Two Lots Tested

A32200DX: SRAM
A32140DX: No SRAM
SRAM Structure Lacks Guard Rings
## Total Dose Performance

<table>
<thead>
<tr>
<th>Device</th>
<th>Recent Capability in kRads (Si)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1280A</td>
<td>1.0 m (MEC) ~ 7</td>
</tr>
<tr>
<td>A1280XL</td>
<td>0.8 m (WIN) &lt; 3</td>
</tr>
<tr>
<td>RH1280</td>
<td>0.8 m (L-M) &gt; 300</td>
</tr>
<tr>
<td>A1280XL</td>
<td>0.6 m (CH) &lt; 3</td>
</tr>
<tr>
<td>Act 3</td>
<td>0.8 m (MEC) 15-50+</td>
</tr>
<tr>
<td>Act 3</td>
<td>0.8 m (WIN) &lt; 5</td>
</tr>
<tr>
<td>A32140DX</td>
<td>0.6 m (CH) &lt; 3</td>
</tr>
<tr>
<td>MKJ911</td>
<td>0.6 m (MEC) 30-50</td>
</tr>
<tr>
<td>KJ911</td>
<td>0.6 m (L-M) &gt; 200</td>
</tr>
<tr>
<td>QYH580</td>
<td>0.8 m (CHIPX) ~ 15</td>
</tr>
</tbody>
</table>

- Act 1, Act 2 Data
- Testing with Protons
- Charge Pump Investigation
  - Internal Measurements
- Design vs. Process
  - A1020Z
TID: Recent Devices

(M)KJ911 Total Dose Performance

A32140DX (Chartered) TID Test
0.5 kRad (Si) / Hour

Hit Power Supply Trip Point
Proton Test: Recent Devices

MKJ911 196 MeV Proton Test
Dynamic Bias

Delta Current (mA)

Total Fluence = 810 x 10^9 protons/cm^2
Zero upsets over the course of the test.

rbk 11/21/96
Proton Test: Recent Devices

A1280XL 196 MeV Proton Test
Dynamic Bias

- A1280XL S/N 61 - 0.6 um; Chartered
- A1280XL S/N 62 - 0.6 um; Chartered
- A1280XL S/N 82 - 0.8 um; Windbond
### Sensitivity to Protons

<table>
<thead>
<tr>
<th>Upset</th>
<th>Likely To Upset</th>
<th>No Upset</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1280XL ‘S’  (0.6, 0.8)</td>
<td></td>
<td>A1280XL ‘C’, I/O</td>
</tr>
<tr>
<td>RH1280 ‘S’   (0.8)</td>
<td></td>
<td>RH1280 ‘C’, I/O</td>
</tr>
<tr>
<td>A1460A ‘S’, I/O (0.8)</td>
<td>Act 3 ‘S’, I/O (0.6)</td>
<td>A1460A ‘C’ (0.8)</td>
</tr>
<tr>
<td>A14100A ‘S’, I/O (0.8)</td>
<td></td>
<td>A14100A ‘C’ (0.8)</td>
</tr>
<tr>
<td>CLAy-31 (0.8)</td>
<td>XC3090 (0.65)</td>
<td>MKJ911 (0.6 um)</td>
</tr>
<tr>
<td>AT6002 (data) (0.8)</td>
<td>- LET&lt;sub&gt;TH&lt;/sub&gt; ~ 4-7</td>
<td>QYH500 3.3, 5.0V (0.8)</td>
</tr>
<tr>
<td></td>
<td>2C04 (config)</td>
<td>- high LET&lt;sub&gt;TH&lt;/sub&gt;</td>
</tr>
<tr>
<td></td>
<td>- LET&lt;sub&gt;TH&lt;/sub&gt; &lt; 7.9</td>
<td></td>
</tr>
</tbody>
</table>
SEU: 5V vs. 3.3V Performance

QYH580 SEU Data (S/Ns 1, 3, 4)

A1460A/RK3 SEU DATA

X-Section/F-F (sq. cm.)

10^5
10^6
10^7
10^8
10^9
10^10

LET (MeV-cm^2/mg)

0 10 20 30 40 50 60 70 80

X-Section/F-F (sq. cm.)

10^{-10}
10^{-8}
10^{-6}
10^{-4}
10^{-2}

LET (MeV-cm^2/mg)

0 10 20 30 40 50 60 70

3.3 Volts
5.0 Volts

CMOD(5V)
SMOD(5V)
CMOD(3.3)
SMOD(3.3)
Flip-Flop Design

Effect of *Hardwired* F-F Design

Effect of *Routed* F-F Design

1E-8 Denotes No Upset

LET (MeV-cm²/mg)

- TD 'S' F-F @ 3.0V, 0.6 um
- A1280A 'S' Storing '0' @ 5.0V
- A1280A 'S' Storing '1' @ 5.0V

X-Section F-F (sq. cm)

LET (MeV-cm²/mg)

- QYH580 Balanced F-F
- A1280A 'C' Storing '0'
- A1280A 'C' Storing '1'
Architectural Features

• Configuration Storage Technology
  ‘Soft’ SRAM Requires Monitor & System Protection
  Input pin ? Output Pin
  Internal Driver Fights (Routing, Tri-State Bus)
  State of the Device: i.e., Programmed, POR

• Higher Complexity Structures
  I/O Modules
  XC6216: Bit Controls Clock On/Off

• DFT/IEEE JTAG 1149.1 Boundary Scan
  State Machine Controls Mode of Device
  Potential For Failure/Damage Modes
  Hard Reset Should Be Implemented
I/O Module Architectures

Act 1: No Storage
Act 2 Latch: \( \text{LET}_{TH} \sim 20\text{’s} \)
Act 3 Reg: \( \text{LET}_{TH} \sim 10 \)

XC4000 (SRAM config)
- input or output
- pullup/pulldown
- slew-rate control
- input delay
- etc
- \( \text{LET} \sim 4-7 \)

XC4000 and XC4000A Families

Input/Output Block

Act 2 Input/Output Block

Act 3 Input/Output Block
IEEE JTAG 1149.1

- Boundary Test Standard
- On All Modern FPGAs
- Can Command Each Pin as an Output (EXTST)
- Variety of Test Modes
- Optional Hard-wired Reset
In-Flight Radiation Experiment

- Power Control Circuit Bus A -- 5V/3.3V
  - Actel A1460A DUT
  - Actel A1460A DUT
  - Actel A1460A DUT

- Power Control Circuit Bus B -- 5V only
  - Actel A1460A DUT
  - Actel A1460A DUT
  - Actel A1460A DUT

- A1280A Interface and Control
  - 250 kHz DUT Clock
  - 1.0 MHz Clock
  - AD590
  - Dosimeter
  - Programmable Bias & Current Monitor

- Telemetry and Commands
  - Shield

- Shield

- MPTB Connector
MPTB FPGA Board
Conclusions

- Scaling vs. Process vs. Voltage vs. Design
  - Many ‘Rules of Thumb’ Fail
  - Testing and Analysis Required
- New, Modern Architectural Features
  - Increase Rad Effects and Affect System Reliability
  - May Introduce New Failure Modes
- COTS Circuit Structures and Radiation
  - ‘Qualification By Similarity’ Can Fail
  - Screening Procedures for Antifuses Critical
- Test Methods Must Be Continuously Updated