Update on Total Dose and Single Event Effects Testing of the Intel Pentium III (P3) and AMD K7 Microprocessors

James W. Howard Jr.

Jackson and Tull
Chartered Engineers
Washington, D.C.

Martin A. Carts
Ronald Stattel
Charles E. Rogers

Raytheon/ITSS
Lanham, Maryland

Kenneth A. LaBel

NASA/GSFC Code 561
Greenbelt, Maryland

Timothy L. Irwin

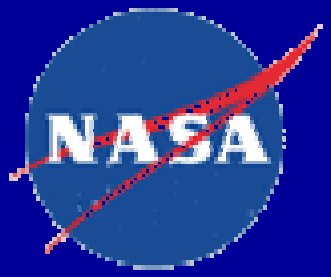
QSS Group, Inc.
Lanham, Maryland

Tony Sciarini

Orbital Sciences Corp.
Dulles, Virginia

Curtis Dunsmore

Swales Aerospace
Beltsville, Maryland



Outline

- *Introduction*
- *Test Methodologies*
- *Hardware*
- *Software*
- *Test Issues*
- *Sample Data*
- *Summary*

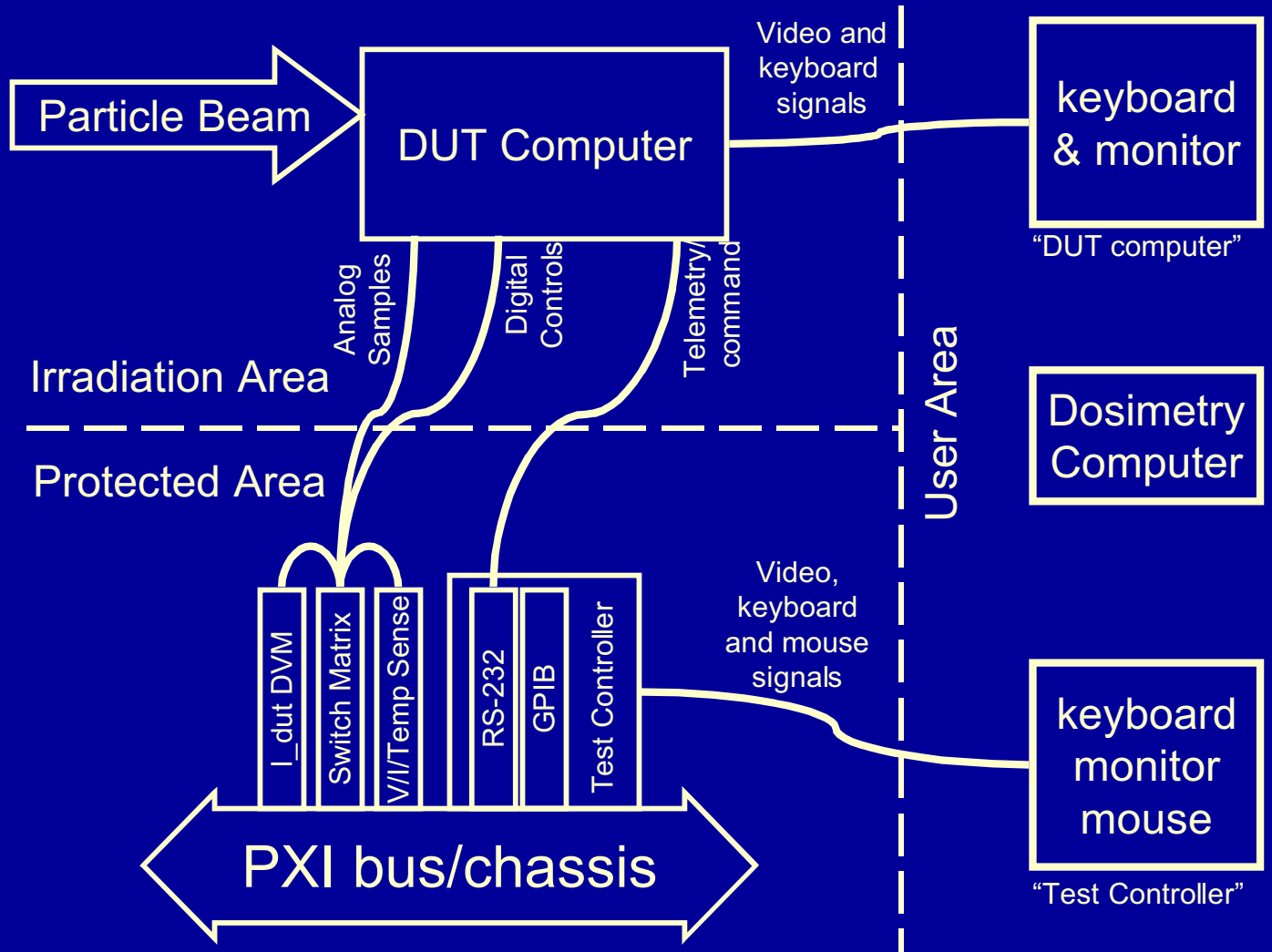
Test Methodologies

- Total Ionizing Dose/Displacement Damage Dose
  - Level of performance testing
    - Functional failure levels, timing errors, power draw
    - Biased vs. Unbiased, idle vs. operating
  - Changing technology testing
    - Vendors (Intel vs. AMD)
    - 0.25 μm vs. 0.18 μm vs. ??
    - Design and operation speeds

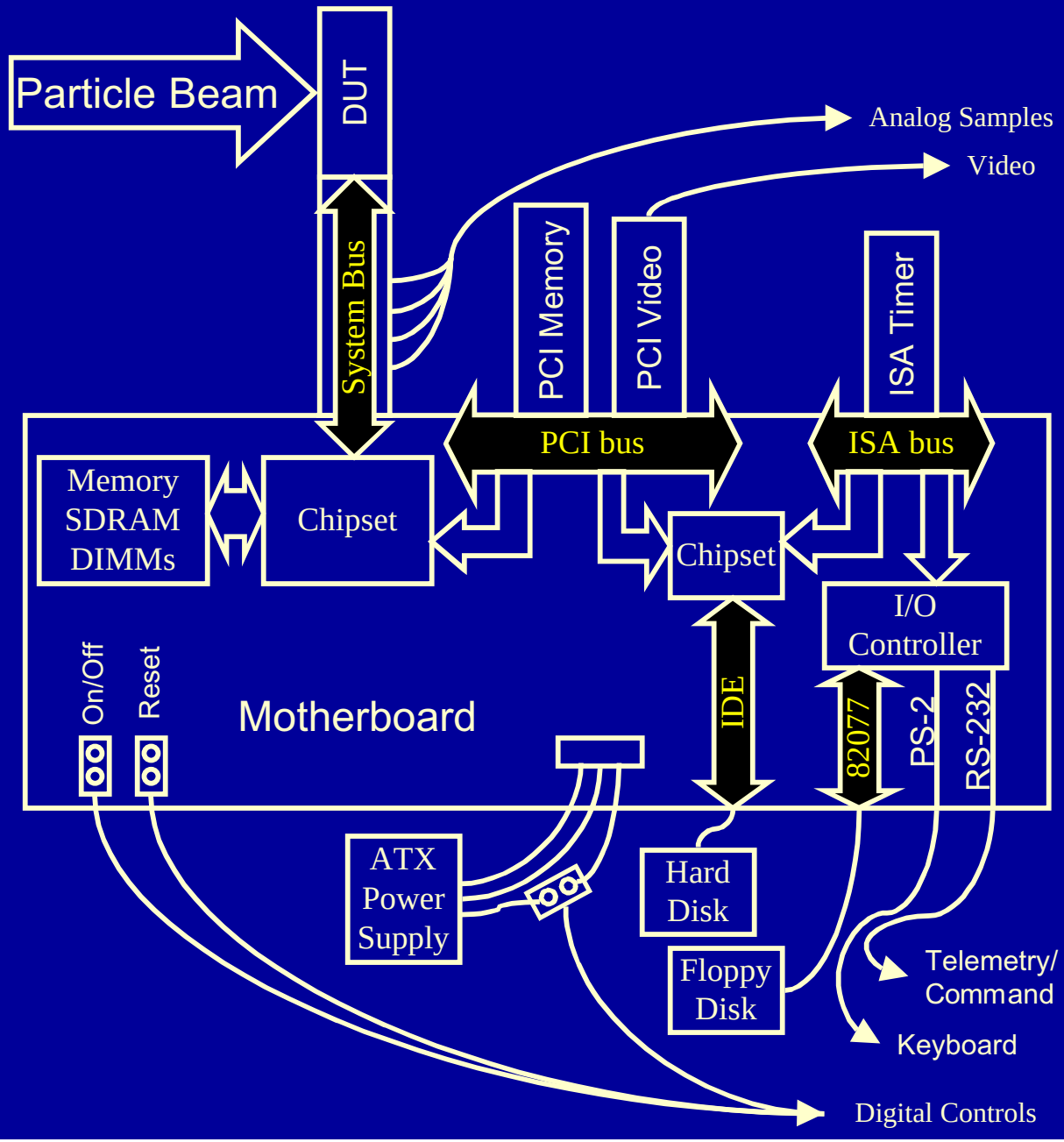
Test Methodologies (2)

- Single Event Effects
  - Architecture and technology implications
    - Test SOTA technology and exercise that technology
    - Exercise independent pieces of the architecture with maximum duty cycle
    - Investigate technology versus operational conditions (e.g., rated versus operation clock speeds)
  - System level impacts
    - Destructive events
    - Function interrupts vs. non-recoverable upsets vs. recoverable upsets

P3 and K7 Test Controller System



P3 and K7 DUT Computer Test System



Programming Environment

- The DUT Software is written in the Microsoft Visual C++ environment with a Pharlap Add-in.
- Tests are written in a combination of C and Assembly Language.
- The software is executed on the DUT using the Pharlap Real-Time Operating System.
- Pharlap was chosen for its low overhead, preemptive multithreading, short interrupt latency, and price.
- The kernel has been stripped to its minimal functionality so that boot time is minimized.
- Kernel interrupts have been disabled to allow the test running full attention of the processor.

DUT Tests

There are eight tests designed to exercise the various aspects of the CPU:

A: Register Test

B: Floating Point Unit Test

C: Memory/Data Cache Test

D: Task Switching Test

E: Instruction Cache Test

F: Floating Point Unit Test (Operation Intensive)

G: MMX Test

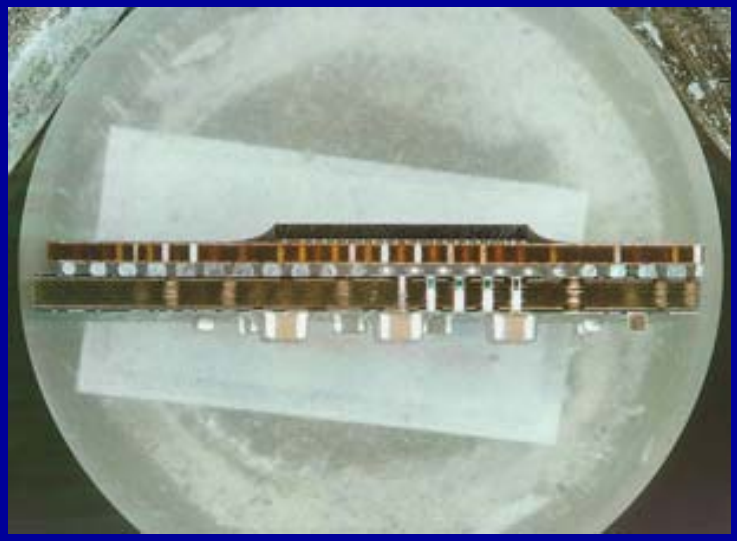
H: Timing Test

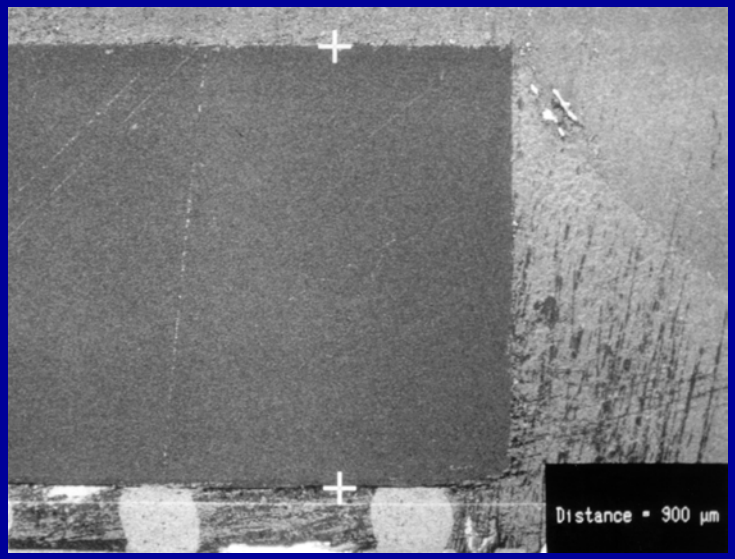
Data Analysis Software

- GUI Interface
- Relational Database (3 Stages)
  - Setup data entered into database
    - Test configurations, software, dosimetry, etc.
  - Telemetry files analyzed and errors entered into database
    - Filter for allowed errors
    - Accuracy (Program shows possible errors and description)
  - SQL statements for filters to extract data

Testing Issues

- Die Penetration
  - The Pentium III die is a flip chip solder bubble bonded die.
  - The sensitive regions of the processor are approximately 900 microns deep in the silicon die.
  - Thermal issues compound this by requiring cooling material in the beam line, as well.
- Thermal
  - The Pentium III can draw in excess of 20 watts of power.
  - The packaged heat sink and cooling fan are removed and replaced with a water-cooled jacket, that is thinned to 10 mils over the die.
  - The large thermal issue is also the reason that the die cannot be thinned.





What Have We Tested

- Intel Pentium III
  - Speed ranging from 550 through 1000 MHz
  - Represents 0.25 and 0.18 μm technology
- AMD K7
  - Speeds ranging from 600 through 1000 MHz
  - Details of technology not available

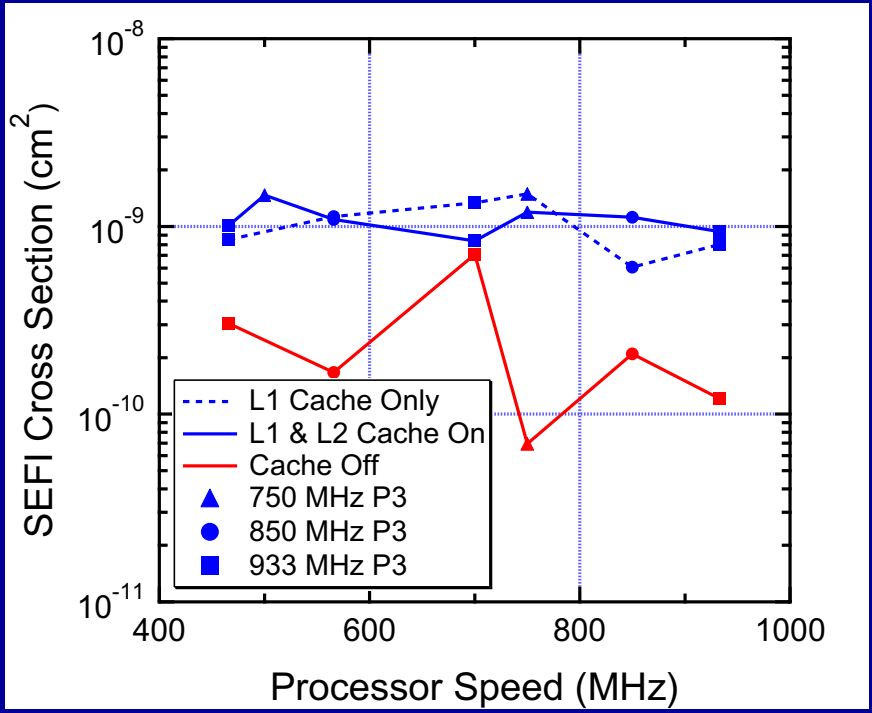
Where Have We Tested

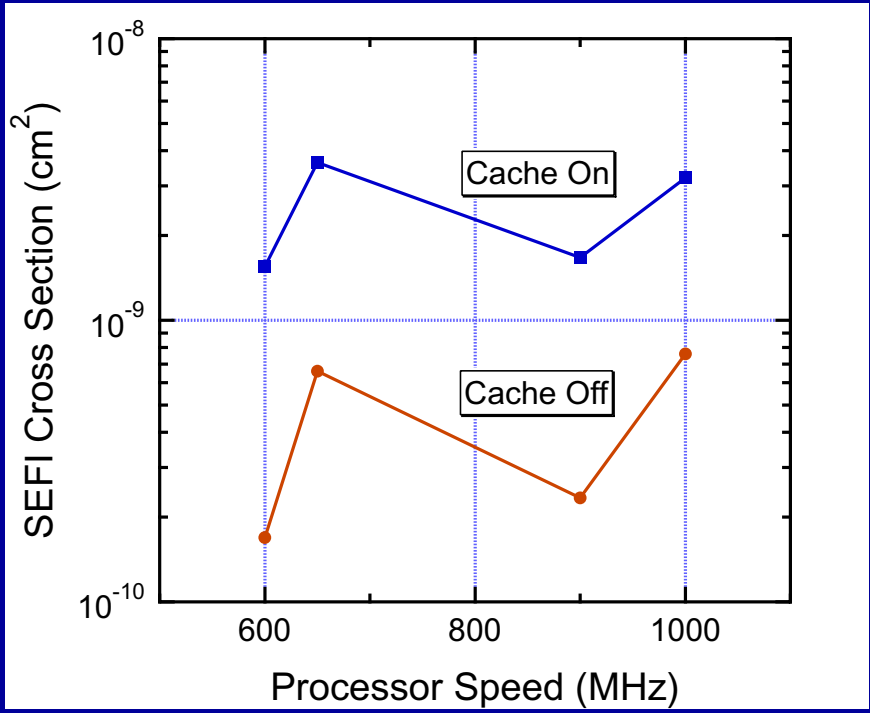
- GSFC TID Facility
  - Biased and Unbiased Co-60 Testing
- Indiana University Cyclotron Facility
  - Proton Displacement Damage
  - Proton SEE
- Texas A&M University Cyclotron
  - 55 MeV/amu Argon and Neon
  - LET range from approximately 3 through 20 MeV-cm^2/mg

TID/DDD Data

TID Device Under Test (DUT) Table				
Device	**Rated Speed**	**Operating Speed**	**Source**	**Exposure Level**
P3	650 MHz	Unbiased	Protons	26 krad
P3	650 MHz	650MHz	Protons	52 krad
P3	550 MHz	Unbiased	Co-60	336 krad
P3	650 MHz	Unbiased	Co-60	336 krad
P3	650 MHz	Unbiased	Co-60	*2.14 Mrad
P3	700 MHz	700 MHz	Protons	100 krad
P3	700 MHz	Unbiased	Co-60	336 krad
P3	*800 MHz*	*800 MHz*	*Co-60*	*511 krad*
P3	850 MHz	Unbiased	Co-60	*635 krad
P3	933 MHz	Unbiased	Co-60	*635 krad
K7	650 MHz	Unbiased	Protons	100 krad

Proton SEFI Data



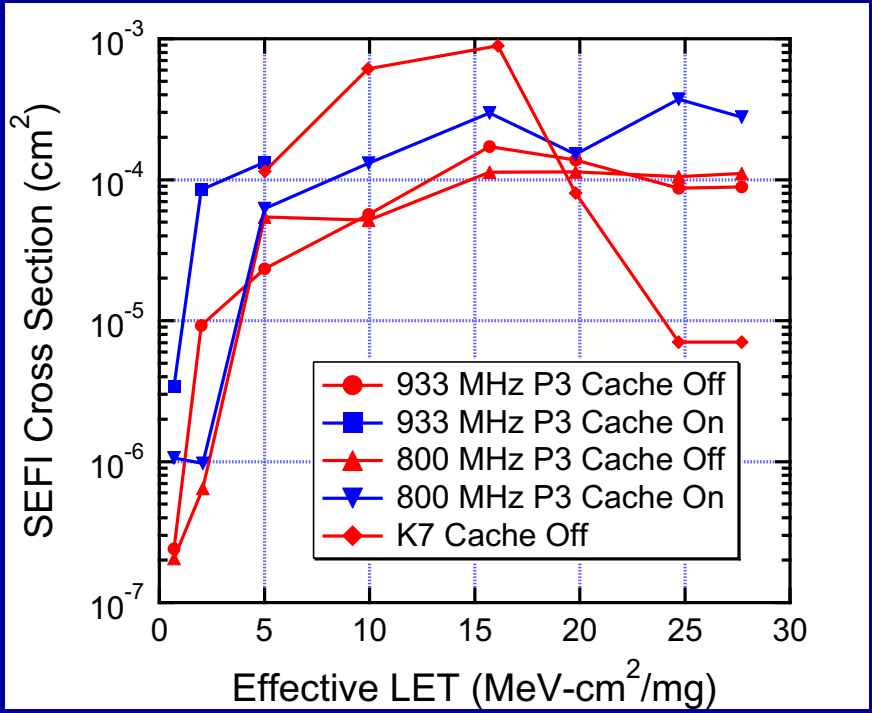


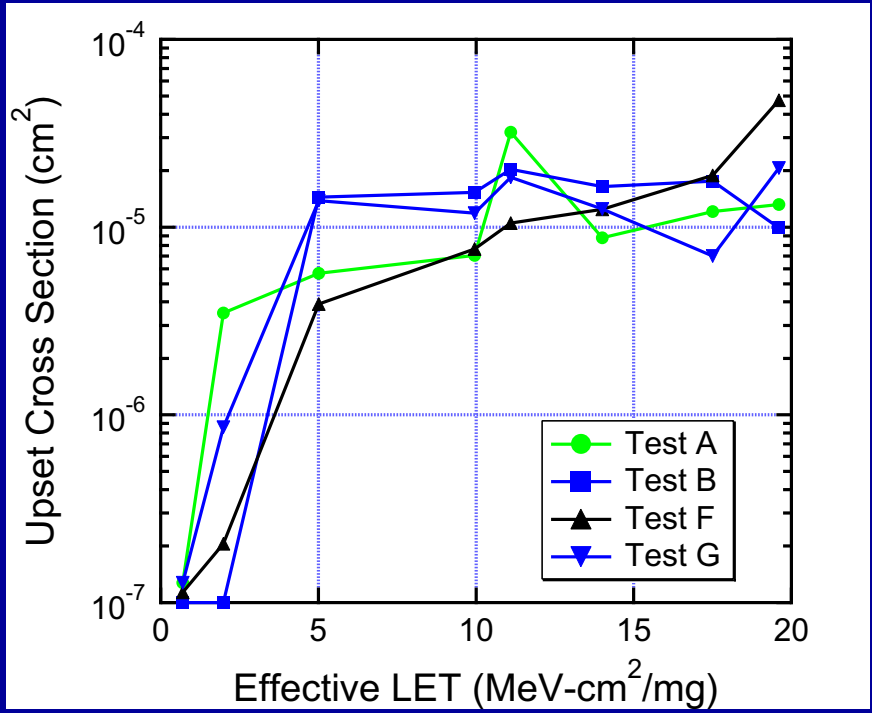
Proton SEU Data

Per Bit Cache Cross Sections				
DUT Spd	**Cache State**	**Single Tag Errors**	**Multiple Tag Errors**	**Cache Bit Errors**
1000	Off	0	0	0
1000	L1 Data	2.8×10^{-14}	0	3.88×10^{-14}
1000	L1 & L2	4.5×10^{-14}	9.36×10^{-17}	2.64×10^{-15}
933	Off	0	0	0
933	L1 Data	2.33×10^{-14}	0	4.07×10^{-14}
933	L1 & L2	3.39×10^{-14}	2.11×10^{-16}	2.43×10^{-15}
850	Off	0	0	0
850	L1 Data	1.9×10^{-14}	0	2.89×10^{-14}
850	L1 & L2	3.83×10^{-14}	3.54×10^{-16}	1.57×10^{-15}

DUT	**Test**	**Number of Upsets**	**Fluence (p/cm^2)**	**Cross Section (cm^2)**
P3	A	1	2.39×10^{11}	4.19×10^{-12}
P3	B	0	2.56×10^{11}	$< 3.91 \times 10^{-12}$
P3	D	1	3.96×10^{11}	2.52×10^{-12}
P3	E	562	3.22×10^{11}	1.75×10^{-9}
P3	F	6	3.92×10^{11}	1.53×10^{-11}
P3	G	4	2.62×10^{11}	1.53×10^{-11}
K7	A	0	5.11×10^{10}	$< 1.96 \times 10^{-11}$
K7	B	0	1.4×10^{10}	$< 7.14 \times 10^{-11}$
K7	D	1	$3.47x\ 10^{10}$	2.88×10^{-11}
K7	F	3	3.04×10^{10}	3.29×10^{-11}
K7	G	0	2.85×10^{10}	$< 3.51 \times 10^{-11}$

Heavy Ion SEE Data





Summary

- Extensive data has been collected on the total ionizing dose and single event response of the Intel Pentium III and the AMD K7 microprocessors.
- The data indicates:
  - high tolerance to TID
  - no susceptibility to SEL from protons or heavy ions to an LET of 15 to 20 MeV-cm^2/mg
  - Single event upsets and functional interrupts are present
- If running with the caches disabled is an option and with mitigation in place, these events may be controllable to allow for operation in the space environment.