Technology Readiness Overview: Embedded Actives

Revision A
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Mark Strickland
NASA/MSFC/EI42
Lead, Electronic Fabrication & Test Team

David Gerke
JPL

Jim Blanche
MSFC/Jacobs-Sverdrup

Prepared for the NASA Electronic Parts and Packaging Program

Overview

Embedding of integrated circuits or bare die in substrates has been a practice of hybrid and multi-chip module (MCM) manufacturers for a number of years. Many of the same methods used in hybrid and MCM manufacturing can be extended to embedding of die and discrete components in the next level of assembly. This approach appears to be gaining favor with developers whose products must withstand severe shock loads, those who desire higher speeds and greater density, and/or those who require cooler and more reliable assemblies.

This technology overview is limited to those technologies that can be extended to packaging of box-level circuitry using embedded techniques in laminate/copper substrates. This approach integrates the motherboard function into the stacked substrates via "vertical interconnects". This TRO is not intended to be an in-depth review of embedding and interconnect methods used in MCM's, however, it focuses on those methods from MCM's that are readily transferable to board level packaging. The technical details of 3D MCM's is the subject of another technology readiness overview (TRO) developed by Auburn, MSFC, and JPL.

Embedded active circuit technology is very much lagging the embedded passive technology. Embedded passive circuit technology has been worked for a number of years and consists of laying down resistors directly on substrates within the circuit board using thin film technology. Tight tolerances can be achieved by laser trimming. Inductors are also being created within the boards and capacitors are created on adjacent layers. These materials are already commercially available, primarily in telecommunications. The NASA Electronic Parts and Packaging (NEPP) TRO on embedded passives contains detailed information. For the most part embedded actives have been used in multichip modules. Bare chips are wirebonded to substrates or flip chips are soldered to substrates along with the passive elements and they are either canned or overmolded.

There are various methods of connecting the die and components to circuit traces within a substrate. One of the more commonly used approaches is the General Electric (GE) High Density Interconnect (HDI) high performance MCM technology invented at the GE Corporate Research and Development Center in Schenectady, NY. It places bare chips into cavities on a base substrate, then builds up a multilayer interconnect over the top of the chips and the substrate using polyimide films, laser via formation and laser photopatterning of the interconnect metallization. It produces a planar assembly with the chips recessed below the interconnection structure [1][2]. Similar work has been published by the Frauenhofer Institute in Berlin where bare dice are directly embedded into substrate openings (cavities) and the interconnection and wiring system is created using thin film technology on the planar chip/substrate surface [3][4].

The Applied Physics Lab at John Hopkins University predicted in 1999 that MCM manufacturers would use embedded techniques to enable zero-clearance stacking of substrates in MCM's [5]. Figure 1 is APL's sketch of a chip first method to embedding which results in high density interconnections utilizing multilayer thin film circuitry.

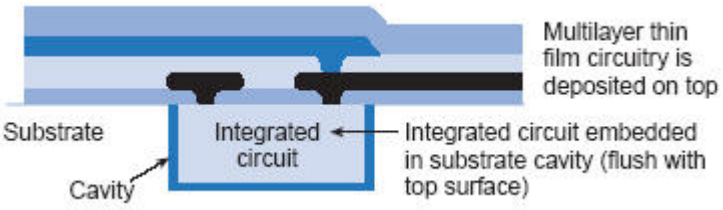

Image courtesy of JHU APL

Figure 1, Chip First Embedded

Mentor Graphics, in a white paper on the subject [6], details several methods of embedding components. The white paper points out that functional density can be increased considerably by placing the die directly into the printed circuit board (PCB). PCB's must accommodate wirebonds, cavities, die on board, die on die, and flip chips. Microvias can be used to accommodate fanouts, and solder bumps can be placed on internal layers to allow mounting of flip-chips. Wirebonding is also mentioned by Mentor Graphics as a method of interconnect which eliminates the need for solder. When solder bumps are used the cavity can be completely laminated over whereas wirebonds require the cavity to be left-open or filled by a flexible material (e.g., silicone).

Industry (Commercial) Trends

By embedding components inside PCB's the surface area is reduced, the design flexibility is increased and high frequency response and other characteristics are improved. Components in low-temperature co-fired ceramics (LTCC) are available; however, they are limited to specific functions/multi-chip modules (MCM's) and are perceived as another type of part. At present, a number of technologies are under development to embed both passive components and IC's inside PCB's made of resin (see Figure 2). Unlike the LTCC boards that suffer from a number of drawbacks such as weight, fragility, difficulty in usage in large boards, and an inability to embed the IC because of the high process temperatures demanded, resin imposes few restrictions on board size. PCB's with embedded components are entirely feasible for use as equipment motherboards. Each technology has its own strong and weak points, and its own target date for practical utility. Development is more advanced for embedded passives, and samples are already available.

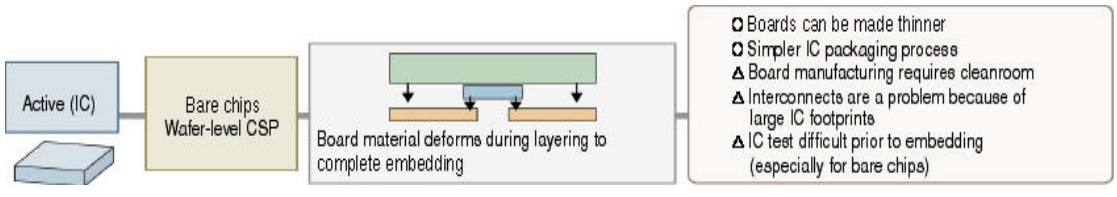

Figure 2

The key problem is that while the technology makes it possible to embed ICs with large footprints in smaller boards, test standards and inspection methods are just beginning to become available and are works-in-progress.

EDR-4703 is a quality assurance guideline developed by the Japanese Electronics and Information Technology Industries Association for bare die including known good die (KGD), but it is a guideline rather than a standard. IEC 62258 – "Semiconductor Die Products: Requirements for Procurement and Use" is an International Electrotechnical Commission (IEC) standard that deals with the production, supply and use of semiconductor products. It addresses wafers, singulated bare die, die and wafers with connection structures, and minimally or partially encapsulated die. As the technology grows closer to practical application, the role of the component-embedded board will no doubt change from modules implementing a function subset to equipment mainboards.

Casio Computer, Matsushita Electric Industrial, and Sony Corp are all developing embedded integrated circuits (ICs). Embedded ICs are normally bare chips and several problems have been identified with this technology. Testing is difficult prior to embedding and a cleanroom is required for board manufacturing. Casio Computer and CMK have packaged the ICs into a wafer-level chip scale package to resolve these problems. Matsushita Electric Industrial and Denso Corp of Japan are separately developing practical technology to embed ICs and passives in the same board and have already begun to test actual embedding characteristics [7].

Shinko Electric Industries Co., LTD. has done some evaluation of interconnect technologies for chips embedded into organic substrates. They embedded ultra-thin Si chips in both a face-up and a flip chip mounting. The face-up chips were interconnected by copper-filled laser-drilled vias and the flip chips by ultrasonic bonding. They determined that in the grinding of ultra-thin chips, a stress relief process was desirable to eliminate backside wafer damage. Their stress simulation showed that thinner, smaller chips were more suitable for embedding. The thinner chip was flexible and the stresses were reduced [8].

A European consortium including Nokia (Finland), Philips (Netherlands), AT&S (Austria), Datacon (Austria), CWM (Germany), IMEC (Belgium), and the Technical University of Berlin (Germany) is cooperating in what is called the HIDING DIES project based on the "Chip in Polymer" concept developed by Fraunhofer IZM and Technical University of Berlin. A chip is attached to a board, and subsequently covered with a suitable epoxy layer. As of April 2006 at least one embedded-chip product has already reached consumer markets, and others are likely to follow shortly.

At Imbera Electronics (Finland) development of board-embedded chip technology has taken a slightly different route. Their product is called an Integrated Module Board, or IMB. IMB uses HDI printed-circuit-board manufacturing processes that have been optimized. Unlike the Fraunhofer die, which is thinned to 50 microns or less, Imbera uses an unthinned die. The IC components are embedded inside the printed circuit board core layer during the core manufacturing process and are connected directly to the core layer copper foil. Microvias are then drilled with a UV laser, and metallized using a semi-additive process with pattern plating process. (9)

Industry is not only focusing on the methods of embedding but also the design and test tools needed to implement this technology. The Die Products Consortium has published a set of PCB design guidelines for chip on board (COB) applications. Much of this information is equally applicable to chip in board applications. Design software previously used in the MCM and hybrid industry is proving useful for layout of PCB's to accommodate embedded devices. Mentor Graphics recently acquired an E-CAD package to bolster their position to provide software to second-level packaging organizations to enable packaging of die/components simultaneously with PCB drill/trim and layout. CAD Design System also has software available for layout that is capable of providing intelligent wire bond net list checking along with full 3D output.

As industry attempts to develop higher circuit density they have looked at 3-dimensional MCM's with stacked substrates. Many of these approaches are also applicable for stacking PCB's with embedded parts. The companies providing periphery interconnection between stacked elements are Matsushita with solder leads on stacked MCM's, General Electric with HDI thin film interconnect laminated to the side of the stack [10], Harris and CTS Microelectronics with blind castellation interconnection, and Trymer with solder dipped stacks to create vertical conductors on the edge. Companies providing area interconnection between stacked MCM's are Raytheon (E-Systems) with fuzz buttons in plastic spacer and filled vias in substrate, Technical University of Berlin with elastomeric connectors with electrical feedthroughs, AT&T with compliant anisotropic conductive material, Hughes with microbridge springs and thermomigration vias, Motorola with solder balls on top and bottom of substrate layers, and Micron Technology and Lockheed with stacked silicon wafers with filled vias [11].

Description of Embedded Packaging Technology

The seemingly most practical and achievable approach to Embedded Packaging Technology (EPT) consists of mounting a printed circuit board(s) on a metal core, bonding bare microcircuit die to the metal core within cavities in the board, bonding passive chip devices to the substrate within cavities in the board, and then wirebonding the die and chip devices to the circuitry on the substrate (see Figure 3). The subassembly depicted in Figure 3 is a Marshall Space Flight Center (MSFC) daisy-chained test vehicle for long-term reliability testing developed by STI Electronics. The subassembly is based on the footprint of a functional subassembly fabricated for the military. The parts within the cavities are conformal coated then the cavities are filled with a protective damping material and are capped with a conductive cover.

The resulting solder joint free assembly is smaller, lighter, runs much cooler, and is capable of surviving much higher vibration and shocks than a conventional printed circuit assembly [12].

Assembly Methods

The STI Electronics assembly approach consists of two multi-layer printed circuit boards (PCB's) bonded to a central copper core. The thickness of the copper core is in the range of .010" to .090". Oversized via holes are drilled in the copper core and filled with an epoxy material for later redrilling and plating to isolate the "thru-vias" from the copper core. Core thickness is a function of design which is primarily dependent upon use environment and circuit power consumption. The PCB's layers are bonded to the core by a sequential lamination process to allow the cavities to be formed with steps down to the core. These steps are where the wirebond pads for electrically connecting die reside. Discrete components can be bonded directly to the core using an electrically insulating adhesive or to the bottom layer of the PCB. Aluminum wire bonds (0.0012") on Al and Au metallizations are used. After placement of tested die and components, the assembly is functionally tested. Then, the assembly is demoisturized and the cavity is coated to provide the first moisture barrier. After coating, each cavity is filled with a silicone gel

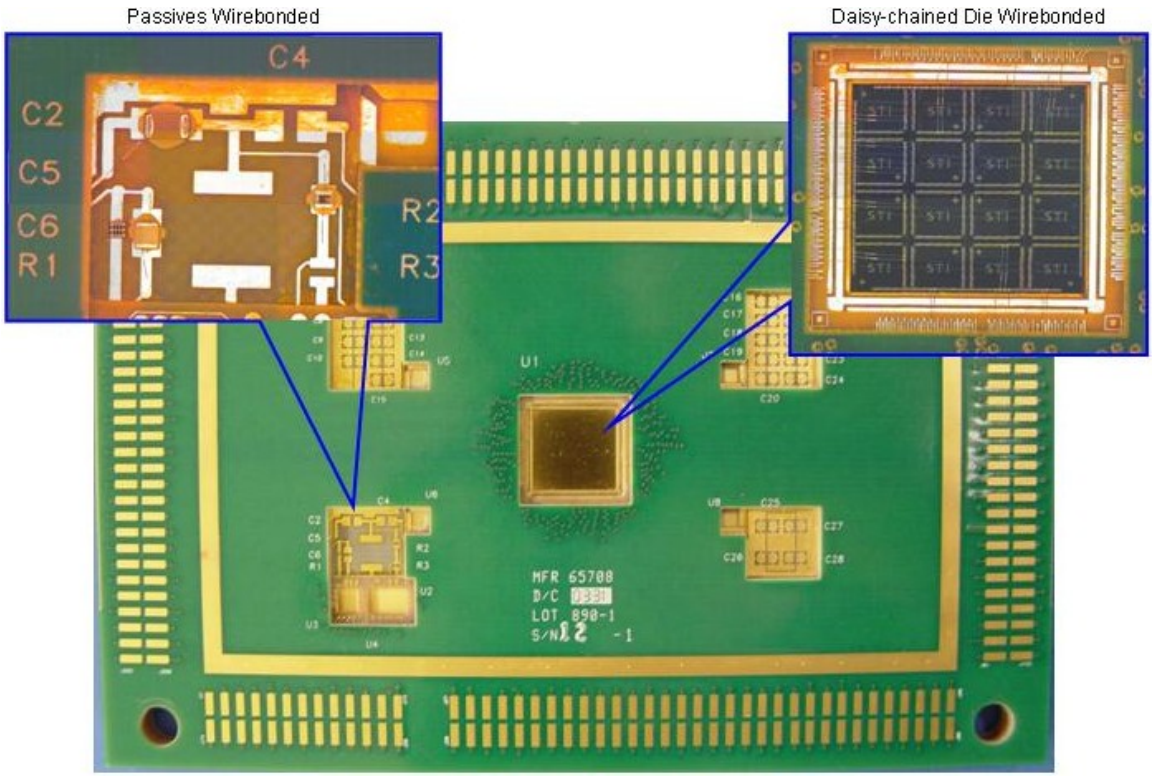

Figure 3, Embedded Subassembly (Cover Removed)

for shock/vibration protection and to provide a secondary moisture barrier. The cavities are then capped over with a copper/laminate plate. The plate can be attached with adhesive, or soldered into place if removal is necessary.

While this approach doesn't yield the functional density of such approaches as the GE HDI it uses demonstrated and proven technology. It does increase the functional density of the circuitry significantly over traditional packaging techniques, is more practical for low volume applications, and is repairable until the cavities are coated. A space

reduction calculation was performed on 12 integrated circuits from a Real-Time Vibration Monitoring System used in the Health Monitoring Computer for Space Shuttle Main Engine ground testing. The average percent reduction was 92% for bare die versus the traditional packaged part size. This calculated reduction was based on bare die size and part body size only. Actual space savings calculations would have to consider the space necessary for die attach bleed-out, bond pads for bare die, and escape area and leads for packaged parts. The die used for these calculations require approximately 20 mils to accommodate bleed-out and substrate bond pad which indicates that the densification is still significant.

JPL has previously experimented with embedded actives in cavities of low temperature co-fired ceramic and polyimide substrates [13]. This was done for the Deep Space 2 project of the New Millennium program. Deep Space 2 generally implemented chip-on-board technology but due to shock loads some of the chips were embedded into cavities in the boards. The JPL approach differed from the previously described embedded method in that an epoxy overmold was applied prior to parylene application.

Producability and Manufacturability Concerns

Some of the concerns for broad application of embedded die technology are die availability, known good die (KGD) testing, rework and non-reparability of the finished assembly, and electrical connection between stacked assemblies and with the outside world.

Die Availability

The die availability issue is improving with time. Dynalog Systems, Inc. has invited a number of the die manufacturers to join the Die Products Consortium, which is a collaborative effort of a dozen major microelectronic companies to expand the market for semiconductor bare die products and processes. Information on them is available at http://www.dieproduct.com. Table 1 presents the results of a survey of additional available bare die.

Table 1, Bare Die

Company	Products	Contact Info.	Shipping Method
Advanced Linear Devices http://www.aldinc.com/	Discretes	Don Howland | Ph.: 1-800-359-4023 sales@linearsystems.com	Wafer, Sawn Wafer, Waffle Pak, Gel Pak, Pocket Tape, Surf Tape
Advanced Micro Devices http://www.amd.com/us-en/	Memory	AMD Field Sales Office	Sawn Wafer, Waffle Pak, Gel Pak, Pocket Tape, Surf Tape

Arizona Microtek http://www.azmicrotek.com/	ASIC, Logic	Ph.: 1-480-962-5881 sales@azmicrotek.com	Wafer, Sawn Wafer, Waffle Pak, Gel Pak
Catalyst Semiconductor, Inc. http://www.catalyst-semiconductor.com/	Analog, Memory	Irv Kovalik | Ph.: 1-408-542-1100 irv-k@catsemi.com	Wafer, Sawn Wafer, Waffle Pak, Gel Pak
Celeritek http://www.celeritek.com/	RF, GaAs	Damian McCann | Ph.: 1-408-330-1274 dmccann@celeritek.com	Wafer, Sawn Wafer, Waffle Pak, Gel Pak
Central Semiconductor http://www.centralsemi.com/	Discretes	Ph.: 1-631-435-1110 inquiry@centralsemi.com	Wafer, Sawn Wafer, Waffle Pak, Gel Pak, Pocket Tape
Delta Microelectronics http://www.delta.dk/	ASIC, Analog, DSP, Logic, RF, Microsystems	Gert Jorgensen / Mette Brunbjerg | Ph.: +45 72 19 40 00 asic@delta.dk	Wafer, Sawn Wafer, Waffle Pak
Dialog Semiconductor GmbH http://www.dialog-semiconductor.com/	ASIC, DSP, MicroProcessor	Malcolm Edwards | Ph.: +49 7021 805 0 malcolm.edwards@diasemi.com	Wafer, Sawn Wafer, Waffle Pak
Dionics Inc. http://www.dionics-usa.com/	Discretes	Ph.: 1-516-997-7474	Wafer, Waffle Pak
EM Microelectronic-Marin SA http://www.emmicroelectronic.com/	ASIC, Analog, Logic, MicroProcessor, RF	Rick Mintle | Ph.: 1-719-598-9224 rick.mintle@emmicro-us.com	Wafer, Sawn Wafer, Waffle Pak, Pocket Tape, Surf Tape
International Rectifier Corp. http://www.irf.com/indexsw.html	Analog, Discretes	Graham Neil | Ph.: +441633811338 diesales@irf.com	Wafer, Sawn Wafer, Waffle Pak, Gel Pak, Pocket Tape, Surf Tape
IXYS Corporation http://www.ixys.com/	Discretes	Ralph Locher | Ph.: 1-408-982-4384 r.locher@ixys.net	Wafer, Sawn Wafer, Waffle Pak
Knox Semiconductor http://www.knoxsemiconductor.com/	Discretes	William Gilbert | Ph.: 1-207-236-6076 knoxsemi@midcoast.com	Waffle Pak

Linear Integrated Systems, Inc. http://www.linearsystems.com/	Discretes	Paul Norton / Don Howland | Ph.: 1-510-353-0216 Sales@Linearsystems.com	Wafer, Sawn Wafer, Waffle Pak, Gel Pak, Pocket Tape, Surf Tape
LSI Computer Systems Inc. http://www.lsicsi.com/	ASIC, Analog, Logic	Jeff Sarment | Ph.: 1-631-270-0400 jeff@lsicsi.com	Wafer, Waffle Pak
Micron Technology http://www.micron.com/products/baredie	Memory, Discretes	barediesupport@micron.com	Wafer, Sawn Wafer
National Semiconductor Corporation http://www.national.com/appinfo/die/	Analog, Logic, RF, Chip Sets	Bruce Blaisdell | Ph.: 1-207-541-8896 Bruce.G.Blaisdell@nsc.com	Wafer, Sawn Wafer, Waffle Pak, Gel Pak, Pocket Tape, Surf Tape
Nippon Precision Circuits http://www.npcamerica.com/	ASIC, Analog, RF	Thomas Hardy | Ph.: 1-408-855-8589 sales@npcamerica.com	Sawn Wafer, Waffle Pak
Semicoa http://www.semicoa.com/main.asp?	Discretes		Waffle Pak
Supertex Inc. http://www.supertex.com/	Analog	Pete Peterson | Ph.: 1-214-596-9010 petep@supertex.com	Wafer, Waffle Pak
Sussex Semiconductor, Inc.	Discretes	Harvey B. Charter | Ph.: 1-239-768-6800 hbcharter@sussexsemiconductor.com	Waffle Pak
Texas Instruments http://focus.ti.com/docs/prod/folders/print/tmp320c50kgd.html	DSP		Individual

Known Good Die Testing

Known Good Die (KGD) are tested bare unpackaged integrated circuits (ICs). IC suppliers often offer several levels of KGD, where each successive level entails a more rigorous test plan. High KGD levels often come with a quality and reliability guarantee, such as guaranteeing them to function on delivery, or to last through a certain time period. Industry aims to provide KGD that have at least as much quality and reliability as they would have if they were packaged.

There are four ways to ensure that a bare IC is "known good": 1) through the process under which the manufacturer fabricates the IC, 2) through the IC design, 3) through bare IC testing, and 4) through sample packaged IC testing.

1) Process: Nothing is more important than having a mature process. While testing at the end of the line can reveal problems, quality cannot be "tested-in". Thus, finding stable processes (six-sigma if possible), understanding process history, and assuring that the process has proper statistical process control are all first steps toward producing KGD. Process maturity dictates the degree of further KGD assurance required. For instance, high yield and favorable process statistics can often justify lower KGD assurance levels than using new or unstable processes.

2) IC Design: One cannot assure that a die works unless it is tested. IC designers use several design strategies (called design-for-testability) to make ICs testable. Besides providing extra pads for testing, designers enhance testability by using techniques such as scan-paths, built-in self test (BIST), boundary-scan, and test structures. Scan-paths are register chains that, in test mode, configure as shift registers through which test engineers send test patterns. Using such shift registers enhances the controllability and observability of each node in the circuit. That is, shift registers enable the circuit to set registers to certain values and determine whether they function correctly. Nodes in the IC that do not function properly cause faults. Engineers measure the comprehension level with which a scan path can test an IC in terms of fault coverage, defined as the ratio of detectable faults to the total possible faults. BIST is test circuitry designed on the chip to enable an IC to exercise about 50% to 80% of non-random logic (PLAs, ROM, RAM, etc.) automatically. While extremely costly, the limited chip accessibility on embedded assemblies often justifies using BIST. Also, by using BIST, the manufacturer does not need to disclose proprietary information such as test patterns for internal design features. BIST can be exercised at-speed without the loading effects or speed limitations associated with external test equipment. Finally, burn-in can utilize BIST by having engineers perform dynamic burn-in without supplying external vectors. Boundary scan is a JTAG (Joint Test Action Group) standard (IEEE 1149.1) method where test engineers use a 4-wire serial bus as a test access for verifying bond wire integrity and assembly-level interconnects. This method employs a shift register chain amongst several chips on an assembly from the test data input pin, around each die's periphery, and finally to the test data output pin. Besides verifying interconnects, chips can use boundary scan as a gateway to internal device logic. This gateway facilitates using BIST at all assembly levels. While mainly a DC test, boundary scan also verifies parametrics such as input switching threshold, output drive, and slew rate. Its most powerful feature is its ability to drive I/O to specific known states as required for parametric tests. This typically would otherwise require thousands of test patterns to set up.

Test structures test the quality of the metallization, the dielectrics, and other material properties of ICs. Test structures come in three forms: 1) as entire ICs, 2) as circuits or transistors in wafer scribe lines, and 3) as part of an IC. As entire ICs (called drop-ins), test structures characterize the wafer on which they are fabricated. As circuits in wafer scribe lines, test structures characterize the wafer, but can only be used at wafer level, since sawing the wafers destroys them. As part of an IC, test structures like BIST are an expensive but effective way to test a particular IC.

3) Bare IC Testing: KGD testing includes electrical, mechanical and environmental tests. Engineers use two basic approaches to electrically test bare ICs: with pressure contact and with metallurgical connections. Wafer probes and temporary carriers use pressure contact while semi-permanent and permanent carriers use metallurgical contact. Bare IC electrical testing aims to rigorously test the die using low resistance connections that do not damage the IC pads. However, some dice require more testing than others. For instance, a state-of-the-art high-density memory that pushes the limits of a process's capability will most likely have a high infant mortality, requiring burn-in on every die.

Conversely, a part with a long history fabricated on a mature process line may require a less comprehensive test plan.

4) Sample Packaged IC Testing: Quality and reliability information about an entire lot can be obtained by packaging IC samples and performing tests on them. Testing packaged IC samples from a given lot can reduce required bare die testing needed. However, this requires close cooperation between the KGD supplier and the embedded actives assembler, and many statistics. Sample packaged IC testing espouses the QML philosophy, in that it promotes doing as much testing on each die as demonstrated necessary and then leaving the other tests out. In general, the less testing required on each die the better, since less testing implies less handling. Handling, in many cases, may actually cause more defects than the tests detect.

Tests for KGD

Tests for KGD can be grouped into six categories: 1) DC parametric tests, 2) AC parametric tests, 3) functional tests, 4) structural tests, 5) burn-in, and 6) other mechanical and environmental tests. MIL-STD-883 describes burn-in and many mechanical and environmental tests.

1) DC Parametric Tests: DC parametric tests measure analog voltage and current values at I/O pads under different I/O loading, temperature, and supply voltage conditions. Since these tests do not run at full speed, they typically run at wafer level. DC tests do not take long to perform and thus test the vast majority of ICs whether further testing occurs or not. However, DC tests alone typically provide only about 85% confidence that an IC has no defects. DC parametric tests measure shorts and opens by applying current and measuring forward diode p-n junction voltage drops on I/Os. DC tests also include leakage tests (excessive current flow through internal paths), and measure parameters such as input switching thresholds, output voltage levels, output current source and sink capability, static supply current, and for CMOS circuits, dynamic supply currents where IDD varies with frequency.

2) AC Parametric Tests: AC parametric tests measure signal timing attributes to determine minimum, typical, and maximum timing values at differing supply voltages and temperatures. AC parametric tests require a much higher bandwidth than DC tests. Since wafer probes tend to have limited bandwidth, usually test plans can include only limited wafer level AC parametric tests. To do full AC parametric testing requires establishing a high bandwidth connection. Thus, AC tests normally occur after packaging an IC. For KGD this implies using some kind of carrier. The NRE costs associated with AC testing can run from $2K to over $30K. AC tests measure propagation delays (input to output time), setup and hold times (verifies signal validity before and after asserting a second signal), signal timing (signal edge placement), pulse width (period), and clock frequency tests (duty cycle and period).

3) Functional Tests: "Function" refers to the set of inputs and resultant outputs that the designer intends the device to process. Functional tests thus test that a device outputs meaningfully correct responses to a given set of inputs. Since function can only be

interpreted by the designer, designers are responsible for developing functional tests. Ideally, functional tests verify that the device will function during actual system operation so functional tests ideally run at system level speed. Like AC tests, full-speed functional tests usually occur after packaging an IC (again implying using a temporary carrier for KGD) due to wafer probe bandwidth limitations. However, functional tests at the wafer level sometimes run at lower speeds. In special cases, low device speed and a high bandwidth wafer probe may enable wafer level at-speed testing. Functional tests, excepting non-random logic devices such as memories, do not thoroughly test every node in a circuit. Structural tests help test the nodes that functional tests miss.

4) Structural Tests: "Structure" refers to the physical layout of logic elements, without regard to their function. Structural tests detect manufacturing defects by providing input to a device and comparing the output with expected results. Because structural tests do not limit input and output vectors to those the device would use for functioning, structural tests can test for many more faults than functional tests. Structural tests especially facilitate testing complex random logic devices such as ASICs, where functional tests particularly lack thorough fault checking. Automatic test pattern generation (ATPG) tools normally generate input vectors and expected output vectors which analyze the device from a structural standpoint without regard to functionality. Structural tests rely heavily on scan paths and other design-for-testability features for achieving high fault coverage (see the discussion on scan paths under "IC Design" earlier in the document). Since structural tests typically do not test for timing problems they need not perform at operating speed. In some cases, engineers apply structural tests at the wafer level.

5) Burn-in: Burn-in exercises ICs at high supply voltage and temperature for several hours (for military applications, 168 hours and for commercial applications, anywhere from 10 to 168 hours). Burn-in exercises IC's in one of two ways: 1) static, applying a static voltage pattern to the circuit, and 2) dynamic, applying varying input patterns so as to flip the states of as many nodes in the circuit as possible. Burn-in screens "infant mortalities" which are parts that have imperfections (such as contamination and process variations) that do not cause failures during electrical testing but will likely cause failures within the first few operating months. Even as processes become more reliable, infant mortalities are inherent in every new design. Performing burn-in on the assembly rather than on each die separately may appear to cost less. However, performing assembly-level burn-in usually costs more and measures less than die-level burn-in. It tends to cost more because it detects problems later in the production cycle, and tends to measure less since it cannot control and observe nodes on each IC as effectively as die-level burn-in. Some companies have "intelligent" burn-in which combines functional, programmable testing with burn-in in the same chamber. These systems can compute infant mortality rates as a function of burn-in time, establish optimal burn-in time per product, and correlate burn-in failure rate and life test data to determine field failure rate.

6) Other Mechanical and Environmental Tests: Engineers can perform several mechanical and environmental tests by packaging a dice sample from a given lot. Temperature and humidity tests, die shear tests, bond pads cross-section, centrifuge, and passivation integrity exemplify such tests. MIL-STD-883, method 5008 and MIL-H-

38534, contain procedures for performing what the military calls “element evaluation”. Element evaluation refers to testing various parts of a hybrid, including the bare dice. Bare die element evaluation is the closest test procedure military specifications have to a KGD procedure.

KGD Procurement

Companies tend not to commit large resources to KGD programs because bare die sales still comprise a small fraction of total IC sales. This segment is growing, and as it grows these programs will become more readily available. Thus, most IC suppliers are slow to develop or acquire special equipment such as the KGD fixtures necessary for burn-in and testers. They also tend not to provide data sheet information unique to die applications. Supplying die data sheets would be a good first step toward placing emphasis on bare die issues. Because the industry has placed little emphasis on bare die issues, the industry lacks bare die standards. Bare die issues that lack standards include mechanical dimensions (die size and pad locations), bare die circuit models, and test programs. Also, vendors supply most bare die without circuit models such as functional models for designing and laying out larger systems. Finally, bare die test vectors often do not come in a format readable by the KGD tester’s test machinery. Translation can be very time consuming. Clearly, establishing standards would greatly simplify procuring and subsequently dealing with bare die.

There are three ways for embedded actives assemblers to acquire KGD. First, assemblers can procure KGD from a die supplier such as Micron who will fabricate ICs, test them, and supply them as KGD. Second, they can procure KGD from a die test house (third party) who buys bare ICs, tests them, and supplies them as KGD. Third parties include Chip Supply, Elmo Semiconductor, Minco, and Semi Dice. Third, the manufacturer can procure bare untested die from an IC fabrication facility and then test the die themselves. Micro Module Systems exemplifies this third KGD acquisition strategy. Each of these strategies entails a different KGD procurement approach.

A die will be tested in an assembly at some point, therefore, the procurement package should also include boundary scan information and other testability features. Furthermore, considering that a die eventually must perform in an assembly, information such as minimum and maximum junction temperature should accompany the die. Finally, the IC fabricator should indicate any process limitations so that engineers can account for them later. Other procurement issues are associated with handling, marking, packing, shipping, and assembly. For instance, bare dice can be packed in sleeves, trays, waffle packs, pocketed tapes, and GEL-paks. Each of these packing strategies has their own set of handling issues.

Because so many different people handle, assemble, test, and otherwise exercise bare dice, bare die suppliers concern themselves with a legally important issue: who has the liability when a die fails? And who, if anyone, is responsible to perform failure analysis in such an event? After all, a die can fail at assembly, test, burn-in, or in the field. Since failures can result from poor handling, poor assembly, poor testing, and poor system-level design as well as from defects and infant mortality, liability is indeed a complex

issue, often implying lengthy contracts between the supplier and the customer. This is yet another reason IC manufacturers hesitate to sell bare die. Many IC manufacturers prefer to sell fully tested KGD rather than partially tested or untested die to reduce the chances that this liability problem will ever manifest itself. Or, they offer minimally tested or untested die with no guarantee.

Die Recovery

For microcircuits that are not available as bare die there are companies that will harvest the die from already finished packaged parts by removing the encapsulation from plastic parts, and in some cases ceramic parts, and either repackaging them or providing the bare die. Some will also screen prior to decapsulation and provide only known good die. DPA Components International (DPACI) has a patent pending die recovery process, DPEM/DCEM (De-encapsulate Plastic/Ceramic Encapsulated Module), for successfully retrieving die from plastic or ceramic packaged parts. The DPEM solution can save hundreds of thousands of dollars over reinventing the device and offers extremely rapid turnaround. A DPEM device can meet all the requirements of military and space level specifications in terms of form, fit, function, quality and reliability.

The Microelectronics Center of Excellence of Harris GCSD is making revolutionary improvements in performance, size, power and weight through collaborative technology developments and process innovations in die harvesting.

Rework

The need for KGD decreases as rework costs go down. That is, in some cases, it may make sense to decrease KGD testing and plan on reworking where needed. Thus, trading off KGD costs with rework costs helps test planners to figure out how much testing constitutes “known good-enough die”. Rework costs depend on several factors including: 1) Materials (ceramic withstands the heat required to remove die better than laminate), 2) die pad number and pitch (high number and low pitch are more labor intensive), 3) die-attach material (epoxy is relatively easy to remove), 4) die-to-substrate interconnect mechanism (tape automated bonding (TAB) and sometimes flip-chip dice can have pull strengths high enough to lift surface metallization), and 5) die costs (high die costs increase total rework costs).

The following assembly testing strategy illustrates a way to balance KGD testing with rework. Consider an embedded actives assembly with a microprocessor, an ASIC, and several support dice. A smart testing strategy would involve the following: test the substrate before committing any dice to the substrate. Then minimally test the support dice and commit them to the tested substrate. At this point, test the partial setup and plan to rework where needed. Then, fully test the microprocessor and ASIC and commit them to the assembly. Finally, test the entire assembly. Thus, this strategy commits small resources to testing the support dice and large resources to testing the complex and expensive dice. This approach minimizes reworking the complex dice, while exploiting the relatively low cost of reworking support dice (as support dice tend to have less I/O and cost less).

The issue of non-reparability is present with an embedded circuit assembly. In the communications industry the cost is low enough, and the designed lifespan short enough, that reparability is not a concern. In NASA's high reliability applications it will be necessary to maintain tight process controls on the build of embedded circuit assemblies to assure that the initial build is defect free so the inherent reliability will be achieved.

Full Array Interconnection

Another concern is that wire bond application currently only allows the use of chips with peripheral contacts. LSI and ChipPAC have developed technology to stagger two and three rows of peripheral bond pads to increase density without increasing size, but to achieve the maximum circuit density potential of this technology, a way must be developed to allow the use of chips with full area contacts. This will entail a different interconnection approach than wire bonds between the chip and board. The concepts being initially evaluated by MSFC include thermosonic bonding (gold-gold), conductive adhesive, and gold-gold surface contact using adhesive die attach.

Vertical Interconnection

The key to successfully building 3D assemblies by stacking EPT sub-assemblies will be developing/qualifying highly reliable vertical interconnections. MSFC is studying several configurations using fuzz buttons. Elastomeric and interposer interconnects are two other popular methods of forming vertical interconnects.

Subassemblies

A subassembly consists of a metal core with through-vias which has a multi-layer PCB bonded to both sides. Availability of manufacturers capable of fabricating PCB's to enable later packaging of die and components inside is a concern. Currently within the United States, two manufacturers have been identified that can perform the sequential lamination processes and meet the tolerances necessary for die level packaging. One fabricator in Asia has also been identified. Special tooling is required to form the cavities in the board which have stepped layers for wirebond terminations, so the PCB's for embedded technology have higher recurring costs. Placement and bonding of the die must be accomplished in a Class 10K cleanroom.

Cost Considerations

Costs of embedded assemblies are approximately 30% higher than conventional printed circuit assemblies. This higher initial cost is offset by lower life cycle costs since embedded assemblies should be more reliable than conventional assemblies due to the reduction in interconnects and elimination of a number of failure modes. Also, overall costs are reduced by virtue of reduced costs of traceability of multiple manufacturers for packaging of die since all die are packaged in one location.

Vendors

Since EPT (as described above) utilizes proven processes, it is possible to fabricate assemblies at numerous locations. Currently, STI Electronics plans to license their process for others who would like to fabricate electronic assemblies using their methods. The largest obstacles to implementing EPT are not fabrication of the assemblies but fabrication of the subassemblies and availability of known good die.

Reliability Issues

Reliability can be impacted by the same type of problems that are encountered in conventional parts packaging. Figure 4 provides a fishbone diagram of typical failure modes of traditionally packaged integrated circuits. For embedded die technology the

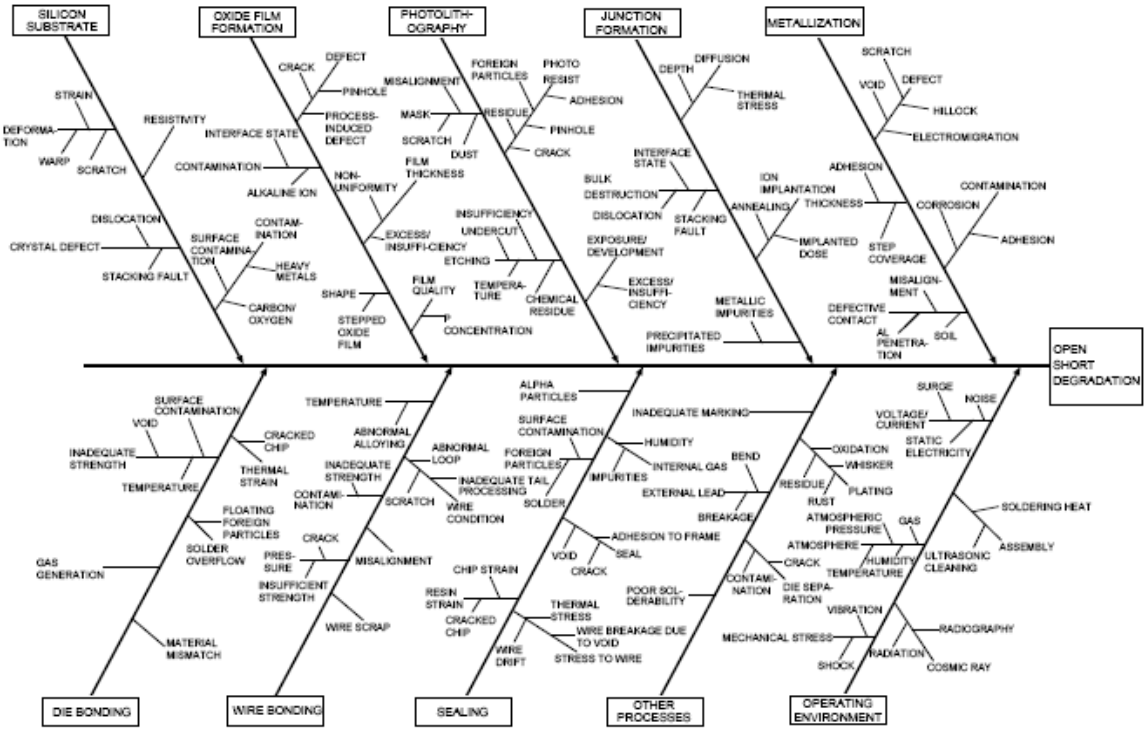

Figure 4, Characteristic Diagram of Semiconductor Device Failures

Courtesy of Mitsubishi Electric

entire top half of the chart can be eliminated if the process starts with a Known Good Die. Moisture and contamination are the greatest concerns. Both moisture ingress and contamination are minimized by the three barriers mentioned above – coating, gel, and lid. Preliminary testing indicates that this approach is successful; however, long-term reliability testing is required. One company has reported that cavity coating increases wire bond strength by a factor of approximately 7 over uncoated wire bonds. The introduction of contamination during fabrication is a potential problem. This obstacle can be overcome by rigorous process controls and a disciplined assembly approach. Vias are

another potential failure mode. This is driven largely by the aspect ratio of the vias and the mechanical properties of the copper plating. To lessen the risk of via problems, aspect ratios should be held as low as possible.

Future of Technology

Embedded circuitry is attractive for electronics that must be reliable in harsh environments over long duty cycles and where passive cooling is required. Embedded circuitry is also attractive where large shock loads are expected. NASA/MSFC first became interested in embedded circuitry because of the possibility of extending the mean time between failures of assemblies by eliminating a large percentage of the total interconnections as well as eliminating or significantly minimizing solder as a method of interconnects. Also, embedded circuitry can operate at lower temperatures than traditionally packaged assemblies due to mounting of heat producing elements directly on a thermally conductive core.

Currently, MSFC has completed two EPT projects: (1) Reliability Testing of Single Substrate EPT Assemblies, and (2) Development of Vertical Interconnects to Enable Module/Box-level Packaging Using EPT. A MSFC Independent Research and Development (IRAD) project for FY06-07 entitled "Development of Robust, Miniaturized, Solderless, Boxless Embedded Electronic Modules" is in the requirements definition phase and couples embedded die/passives with zero-clearance vertical interconnects to form an electronic cube.

The reliability testing of EPT subassemblies (shown in Figure 3) was a MSFC Center Director's Discretionary Fund project. Nine subassemblies were designed and fabricated. The assemblies included two daisy chained die per assembly and six passive components. The core thicknesses ranged between 0.010" to 0.040". Two different die attach materials were used in the test vehicles - traditional epoxy-based die attach and silicone-based die attach. The test vehicles were exposed to thermal testing (-55°C to 125°C) and were continuously monitored for continuity throughout the testing. Thermal testing began in January 2005 and most of the subassemblies were exposed to at least 2500 thermal cycles. Early problems were experienced on several assemblies that were coated with parylene and potted with silicone gel. Destructive physical analysis (DPA) revealed that these problems were caused in part by contamination of the bond pads and a faulty parylene application process. Interestingly, one subassembly whose cavities are not coated or filled experienced the fewest failures and was exposed to over 3500 thermal cycles; the first failure was after 2000 cycles. The current MSFC IRAD will explore various material mixes for cavity fill (i.e., epoxy overmold) and will include subscale material properties testing of ~.001" thick parylene samples by Auburn University.

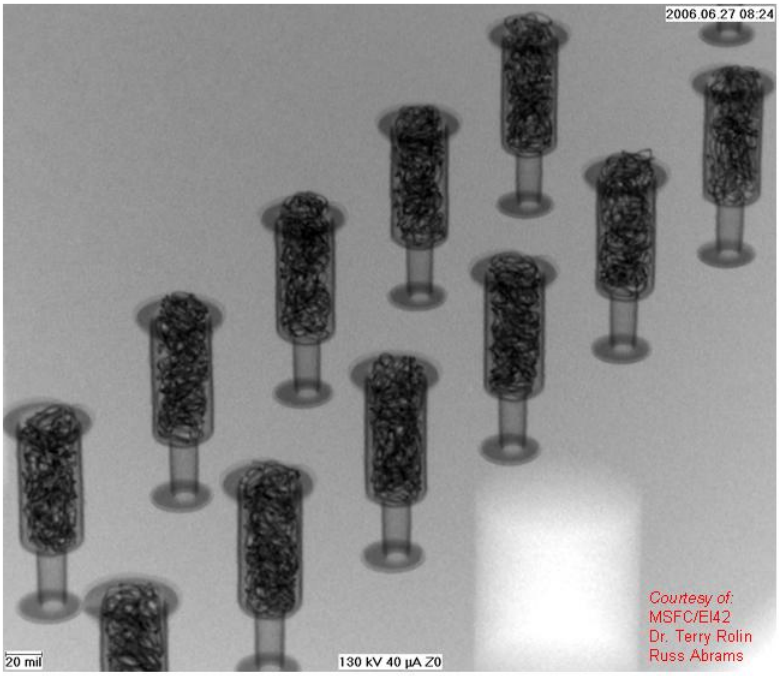

Figure 5, Vertical Interconnect (X-ray of Fuzz Button in Via)

Development of vertical interconnects was a MSFC task funded by the Next Generation Launch Technology program. This task started in April 2004. MSFC designed three different test vehicles to assess the reliability of fuzz buttons as vertical interconnects between substrates. The fuzz buttons are less than 0.8 mm in diameter and are fabricated from gold plated molybdenum wire. MSFC and Auburn University performed vibration and long term thermal testing. Each test vehicle design used a different configuration of fuzz buttons to determine the optimum design for the next phase of the EPT development. Figure 5 shows an x-ray image of fuzz buttons in vias which is the down-selected vertical interconnect configuration. One configuration that used serrated hardhats over the fuzz buttons suffered early failure due to severing of the PCB surface pads by the hardhats. Two of the configurations were exposed to over 4500 thermal cycles (-55°C to 125°C) and behaved very well. Each configuration contained 64 monitored channels. One configuration experience six failures out of 64 while the other configuration experienced only four failures out of 64. Failure analysis of these two configurations has identified the failure mode as circumferential via cracks and not the fuzz buttons.

In the current MSFC IRAD project, a component-level design will be developed, fabricated and tested with daisy-chained die, heater/stress and thermal sensor die, passive components, stacked substrates, through core vias and various cavity configurations. Figure 6 is the MSFC model of an embedded component that will be developed for this project.

Ultimately, the goal of these efforts is to package an avionics component using EPT which would be an electronic cube with no air gaps, no solder joints and no structural housing (black-box). JSC has a CDDF to repackage an existing functional circuit using embedded technology. This project is in the design phase.

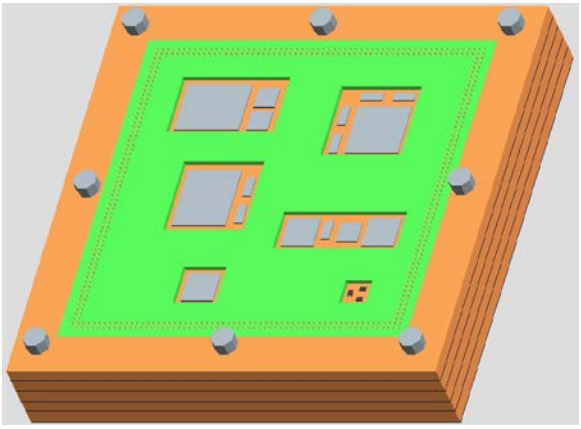

Figure 6, Embedded Component

JPL/Avionics and Auburn University have researched methods of reliably embedding die/flip chips in flexible laminate structures. The methods of interconnect being evaluated are stud bumps and solder/electroless nickel flash gold.

Potential Show Stoppers

Implementation of this technology is envisioned where size, modularity, passive cooling and/or reliability are drivers. Application of this technology to power electronics is questionable due to part sizes and to facilitate its use may require traditional piggyback modules to house larger inductive elements. Obviously, the up-front costs will be a deterrent in applications that do not have a specific need that EPT meets. Also, where bare die aren't available the efficacy of die harvesting is somewhat questionable as are the costs associated with it. Repairability is also a concern that must be dealt with by risk mitigation strategies such as simulation and subassembly test. A concern has been reported in literature [14] with silicone gel increasing stresses on wire bonds. The current program at MSFC is investigating whether the increase in bond strength that results from coating application minimizes this concern. Also, MSFC observed that parylene C used to coat the cavities rapidly became brittle when exposed to 125°C. The literature reports various glass transition temperatures for parylene C. Auburn University is conducting materials property testing on parylene C using samples of equivalent coating thickness. Cavity fill using parylene will depend on the outcome of these tests. Presently, epoxy overmold is the most attractive cavity fill material. Overall, there are no major show stoppers for most applications since this technology is based on building blocks of proven technology.

Technology Evolution

Near Term:

The near term evolution of this technology will be to implement it in module and box-level packaging for a standard space environment. This will include both periphery and arrayed die, standard passive parts, and printed passive parts. This architecture will need to be proven first in subscale extended environmental testing followed by qualification of functional modules/boxes. Near term evolution should also consider use of this technology in extreme thermal and radiation environments. Thermo-electric devices or

similar elements should be incorporated to allow box-level control of the natural thermal environment. For extreme cold environments (-120C and below) it may be necessary to incorporate either printed or silicon heaters or laminated foil heaters at various locations. Initial box-level packaging should be optimized by radiation and thermal analysis techniques. Densification of PCB's is predicted to continue. Currently, conductor width and spacing is around 3.5 mils. In the near term, this can be driven to 2 mils using subtractive processes. Chip stacking is possible today and should be incorporated once the technology has passed some of the early tests. Use of a composite core material with a coefficient of thermal expansion matched to silicon should be pursued and one candidate material is under investigation as part of another research project. Development of reliable solderless interconnects for full array flip chips should be pursued in the near term. Also, development of embedded power circuitry should be studied and if necessary a coupling of EPT and module technology should be employed to allow use of larger inductive devices. Near term, design of assemblies for space use in non-critical applications could begin as early as FY2008.

Long-term:
Long term, the technology should be driven to the highest density level possible using standard printed circuit board manufacturing capabilities. Functionally the packages should be designed to stand alone by incorporating in-package power generation and wireless communications functions. To accomplish this economically, advancement in ultra-low power technologies is necessary. This would greatly increase modularity.

Conclusions

EPT is a viable packaging technology that has many advantages over existing box-level architectures (see Table 2). EPT as described herein is a viable technology for applications where smaller size/weight, robustness, reliability and/or passive cooling are drivers. Although the TRL is estimated to be ~3-4 this could be rapidly increased to 6 or higher because the technology is built upon other proven technologies.

Table 2, Advantages/Disadvantages of EPT

Advantages	**Disadvantages**
Functional densification	Higher initial costs
Size/weight reduction	Limited bare die availability
Cooler circuitry	Availability of Known Good Die
Faster circuitry	Finished assembly non-repairable
Reduction of interconnects by ~50%	Design/testing complexity
Elimination of solder	More controlled assembly process
Improved shielding	More complex substrate fabrication process
Decrease in parasitics	More stringent cleanliness controls
Lower life cycle costs	Availability of board manufacturers
Increased reliability	
Die packaging traceability simpler	
Built on proven technologies	

Enhancements to the technology, such as die stacking, PCB densification, and incorporation of CTE matched cores should be considered in future work. Enhancements for application of the technology in extreme environments should be pursued in subscale test vehicles.

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