



EMBEDDED PASSIVES IN SPACE



- **DEFINITION**
- **TECHNOLOGY REVIEW**
- **CHOICE OF TECHNOLOGY TYPE**
- **ADVANTAGES**
- **DISADVANTAGES**
- **CURRENT STATUS**
- **FUTURE DIRECTIONS**



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WHAT ARE EMBEDDED PASSIVE DEVICES ?

THESE ARE THE CIRCUIT ELEMENTS SUCH AS RESISTORS, CAPACITORS, and INDUCTORS WHICH ARE NOT FUNCTIONALLY ACTIVE CIRCUIT ELEMENTS

ON PWB's OR OTHER PLANAR SUBSTRATES, THESE COMPONENTS ARE MOUNTED ADJACENT TO OR NEAR ACTIVE SILICON DEVICES.

PASSIVE ELEMENTS CAN OFTEN BE 50-80% OF THE TOTAL COMPONENT PART COUNT.

THE RESULT IS THAT 40-50 % OF THE AVAILABLE BOARD SURFACE AREA IS CONSUMED BY THE PASSIVE DEVICES.

EMBEDDED PASSIVES ARE THESE SAME DEVICES INCORPORATED INTO THE STRUCTURE OF THE SUBSTRATE .

FROM AN HISTORICAL PERSPECTIVE EMBEDDED PASSIVES ARE NOTHING NEW. THEY HAVE BEEN USED IN SILICON INTEGRATED CIRCUITS and HYBRID CIRCUITS SINCE THE ORIGIN OF THESE DEVICE TYPES IN EARLY 1960's.



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EMBEDDED PASSIVE TECHNOLOGY TYPES CURRENTLY AVAILABLE :

- **PRINTED WIRING BOARDS**
- **THICK FILM SUBSTRATES**
- **THIN FILM SUBSTRATES**
- **CO-FIRED SUBSTRATES; HIGH AND LOW TEMPERATURE TYPES**
- **FLEX SUBSTRATES**
- **SILICON SUBSTRATES**



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OF THE MANY TYPES AVAILABLE, THE ONE I CHOSE TO INVESTIGATE WAS THE FLEX TYPE SUBSTRATE.....

BECAUSE....

IT PRESENTS A NUMBER OF ADVANTAGES WHICH MAKES IT WELL SUITED TO OBJECTIVES WE HAVE AT JPL FOR FUTURE MISSIONS SUCH AS:

- **AUTONOMOUS SPACE CRAFT FOR DEEP SPACE MISSIONS**
- **SOLAR SAILS FOR BOTH INTER AND INTRA GALACTIC MISSIONS**



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ADVANTAGES:

- **NON-REINFORCED LOW DENSITY POLYMERS WILL BE USED**
 - / **COMPLETED CIRCUIT ~ 25% THE MASS OF A COMPARABLE PWB**
- **LAYER THICKNESSES AT 50 MICRONS**
- **MATERIALS WILL BE DEPOSITED ONTO THE POLYMER, THEN PHOTO-DEFINED AND ETCHED USING THIN FILM LITHOGRAPHIC TECHNIQUES**
- **VERY HIGH ROUTING DENSITY POSSIBLE**
 - **LINEWIDTHS FROM 5 TO 25 MICRONS**
 - **CONDUCTOR THICKNESSES FROM TENTHS OF MICRONS TO SEVERAL MICRONS DEPENDING ON CIRCUIT OPERATING VOLTAGES AND CURRENT LEVELS**
 - **VIAS FROM 25 TO 50 MICRONS DIAMETER, SO A/R's REMAIN PRACTICAL**
- **COMPLETED LAYERS CAN BE ELECTRICALLY TESTED PRIOR TO LAMINATION**
- **BY USING SILICON ACTIVE DEVICES THINNED TO LESS THAN 50 MICRONS ON THE TOP LAYER, THE ENTIRE CIRCUIT CAN BE DEFORMABLE**
- **THE CIRCUIT CAN BE FOLDED INTO A 3D STACK IF FOLD AREAS DESIGNED IN INITIALLY**
- **THE CIRCUIT CAN BE DEFORMED INTO A ROLLED TUBE TO FIT UNIQUE PACKAGING LOCATIONS**



DISADVANTAGES:

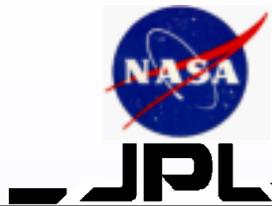
- **UNLIKE A PWB, THIS CIRCUIT IS FIXED ONCE IT HAS BEEN LAMINATED. FOLLOWING LAMINATION, THE PASSIVE DEVICES ARE NOT REWORKABLE. ALL DESIGNS MUST BE SIMULATED AND VERIFIED PRIOR TO FABRICATING ACTUAL CIRCUITRY.**

- **LAYER STACKING FROM BOTTOM –TO-TOP WOULD BE:**

- **RESISTOR(S)**
- **INDUCTOR(S)**
- **CAPACITOR(S)**
- **ROUTING LAYER(S)**
- **ACTIVE DEVICE LAYER**

THIS STACKING SEQUENCE IS ESSENTIAL TO ALLOW ACCESS TO RESISTOR LAYER FOR ACTIVE TRIMMING. ALSO PLACEMENT OF INDUCTORS INTO INNER LAYERS TO REDUCE INDUCTIVE COUPLING WILL BE NECESSARY.

- **VERIFIED SIMULATION MODELS MUST BE DEVELOPED. PROPER LOCATION OF INDUCTORS IS NOT WELL MODELED.**



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CURRENT STATUS:

- **ESTABLISHED PARTNERSHIPS WITH UNIVERSITY OF ARKANSAS/HiDEC, PENN STATE UNIVERSITY, and ADVANCED PROCESS CONCEPTS IN FY '00 TO:**
 - ...SURVEY THE CURRENT CAPABILITIES OF BOTH RESEARCH INSTITUTIONS AND INDUSTRIAL PRODUCERS**
 - ... SELECT THE MATERIAL SETS WHICH WOULD BE USED**
 - ... INVESTIGATE OPTIONAL MATERIALS WHICH WOULD BE SUITED FOR HIGHER PERFORMANCE FOR RESISTORS, CAPACITORS, AND INDUCTORS.**
- **HAD HiDEC PRODUCE ARRAYS OF RESISTORS, CAPACITORS, AND INDUCTORS**
- **PRODUCED RESISTORS OF VARIOUS GEOMETRIES FROM 10 OHMS TO 10000 OHMS, USING CHROME SILICIDE ON POLYIMIDE**
- **PRODUCED CAPACITORS RANGING FROM 1 PICO FARAD TO 100 NANOFARADS USING TANTALUM PENTOXIDE/POLYIMIDE AND BCB/POLYIMIDE**
- **PRODUCED INDUCTORS IN VARIOUS GEOMETRIES RANGING FROM 1 TO 40 NANOHENRIES USING COPPER/BCB/POLYIMIDE**



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CURRENT STATUS:

- **IN CURRENT YEAR, FY '01, WE ARE PARTNERING WITH INTEGRAL WAVE TECHNOLOGY, INC. TO PRODUCE AND DEMONSTRATE A SINGLE DECOUPLING CAPACITIVE LAYER WHICH COULD REPLACE MOST, IF NOT ALL, DECOUPLING CAPACITORS IN THE CIRCUIT.**
- **THIS TECHNOLOGY HAS BEEN DEMONSTRATED TO EXCEED THE PERFORMANCE OF CONVENTIONAL DECOUPLING CAPACITORS BY THE NCMS CONSORTIA**
- **A DECOUPLING CAPACITIVE LAYER IS ESPECIALLY WELL SUITED TO LAMINATED FLEX DESIGNS SINCE SIGNAL PATH LENGTH BETWEEN THE LAYER AND THE ACTIVE SILICON DEVICE CAN BE FROM MICRONS TO HUNDREDS OF MICRONS**
- **IN ADDITION, INTEGRAL WAVE IS DEMONSTRATING MICROVIA FORMATION USING REACTIVE ION ETCHING, LAYER LAMINATIONS WITHOUT ADHESIVE, AND CYCLING FLEXIBILITY TO DEMONSTRATE RELIABILITY OF THE FULLY LAMINATED CIRCUIT**
- **ADDITIONAL TESTING OF LAMINATES WILL BE PERFORMED AT JPL TO EXPOSE THE TEST VEHICLES TO DEEP TEMPERATURE CYCLING, -180 TO + 100 °C, AND TO RADIATION ENVIRONMENTS TO DETERMINE POLYMER CHAIN DAMAGE AND SPACE CHARGE ACCUMULATION EFFECTS**



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FUTURE DIRECTIONS:

- **IN FY'02, IF THE PROPER FUNDING ALLOCATION IS APPROVED, A FULLY FUNCTIONAL DEMONSTRATION CIRCUIT WILL BE FABRICATED. WE WILL SELECT A CIRCUIT WHICH HAS ALREADY BEEN BUILT AND TESTED IN PWB TECHNOLOGY AND DUPLICATE IT IN LAMINATED FLEX USING EMBEDDED PASSIVE ELEMENTS TO DIRECTLY DEMONSTRATE:**
 - **THE ELECTRICAL PERFORMANCE ADVANTAGE**
 - **THE REDUCED MASS/VOLUME**
 - **THE ABILITY TO PACKAGE IN UNIQUE CONFIGURATIONS**
- **THE X-2000 DEMONSTRATION PROGRAM IS ALREADY ADAPTING THIS TECHNOLOGY IN AN EFFORT TO IMPROVE PERFORMANCE AND SAVE MASS. SINCE RAPID TECHNOLOGY INFUSION INTO CURRENT PROJECTS IS ONE OF THE MAJOR OBJECTIVES OF THE NASA/NEPP PROGRAMS, IT WILL BE OUR PLEASURE TO SUPPORT THEIR EFFORTS.**



EMBEDDED PASSIVES IN SPACE



A SPECIAL THANKS TO MY JPL ASSOCIATES:

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- DAVID GERKE**
- DAVID MIH**

**AND ALSO TO OUR COLLABORATORS AT U of A
AND INTEGRAL WAVE:**

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- DAVID NELMS**