Performance of Rad-Hard Quad Receivers at Extreme Temperatures

Quiesup Kim, Shri G. Agarwal, and Tetsuo F. Miyahira

Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Dr., Pasadena, CA 91109-8099

Purpose

Performance of Rad-Hard Quad Receivers at Extreme Temperatures

- **Characterize the electrical performance and reliabilities as potential space electronic parts under extreme low and high temperature (-125 ~ +150°C) environments extending nominal device specifications (-55 ~ +125°C).**

- **Identify needed enabling technologies to improve operation, reliability, and lifetime of future space missions such as Mars.**

Presentation outline

Performance of Rad-Hard Quad Receivers at Extreme Temperatures

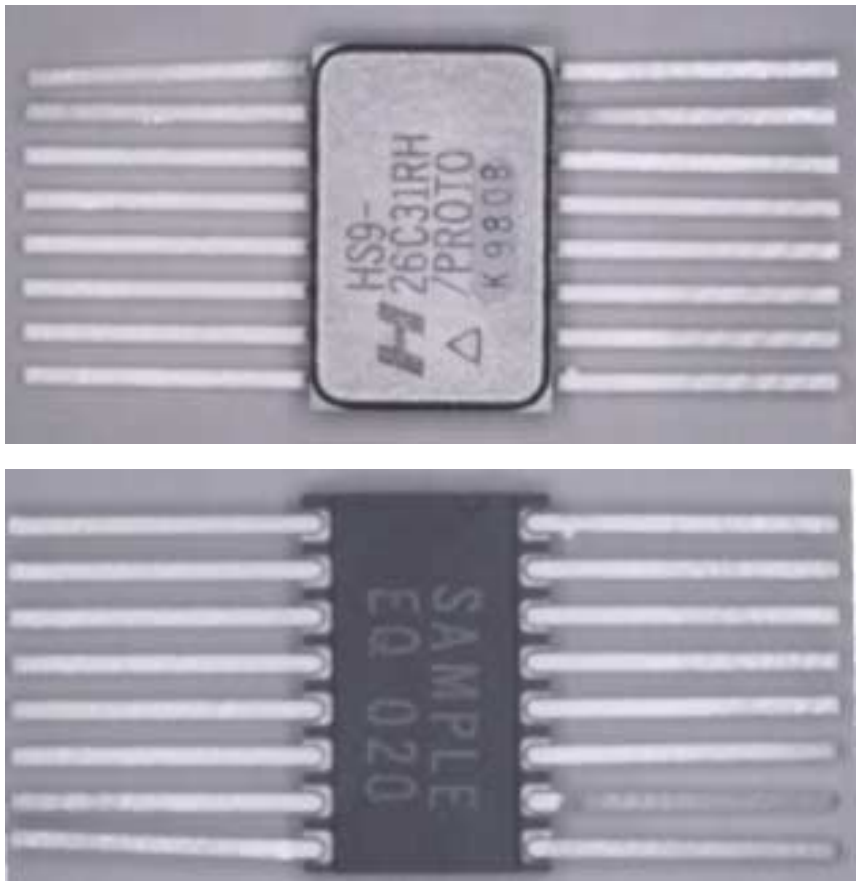
- **Purpose**
- **Rad-Hard Quad Receivers**
- **Test Method**
- **Results**
- **Conclusions**
- **Recommendations**

Rad-Hard Quad Receiver

Performance of Rad-Hard Quad Receivers at Extreme Temperatures

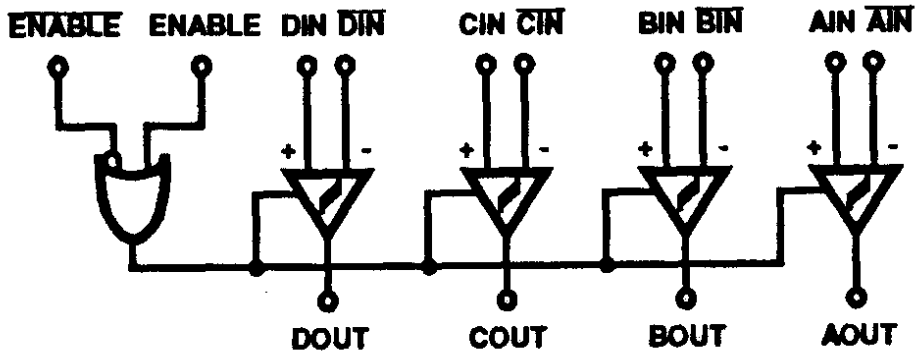
- **A quad differential line receiver designed for digital data transmission (logic input buffer) over balanced lines and meets the requirements of RS-422**
- **Radiation Hardened CMOS processing for low power consumption, high speed, and reliable operation in the most severe radiation environments.**
  - **Total Dose:100KRAD (Si)**
  - **Single Event Upset (SEU)**
  - **Single Event Latch-up (SEL)**
  - **Thresholds: >100 MeV/mg/cm2**
- **Supply current at low and high state**
- **Dynamic supply current**
- **Input current at high and low state**
- **Output high and low voltages**
- **Tri-state low and high current**
- **Propagation delays and transition times.**

Rad-Hard Quad Receivers



- **Radiation hardened RS-422 line receiver**
- **Has CMOS enable pin input levels and accepts TTL-level enable signals**
- **The two circuits are identical except for the configuration of the logic input buffers**
- **The HS-26C32RH has the same input characteristics (impedance, hysteresis, failsafe) as commercial types.**

Functional Diagram



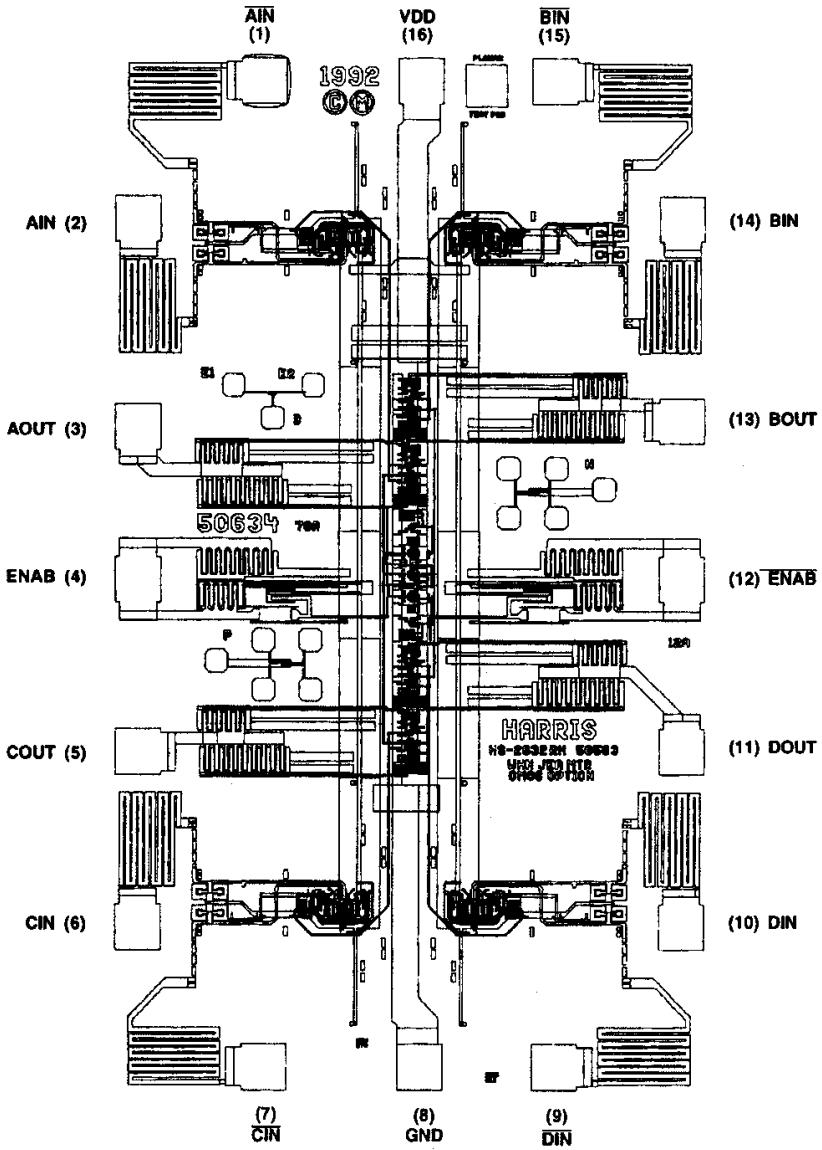
TRUTH TABLE

DEVICE POWER ON/OFF	INPUTS			OUTPUT
	ENABLE	ENABLE	INPUT	OUT
ON	0	1	X	HI-Z
ON	1	X	VID ≥ VTH (Max)	1
ON	1	X	VID ≤ VTH (Min)	0
ON	X	0	VID ≥ VTH (Max)	1
ON	X	0	VID ≤ VTH (Min)	0
ON	1	X	Open	1
ON	X	0	Open	1

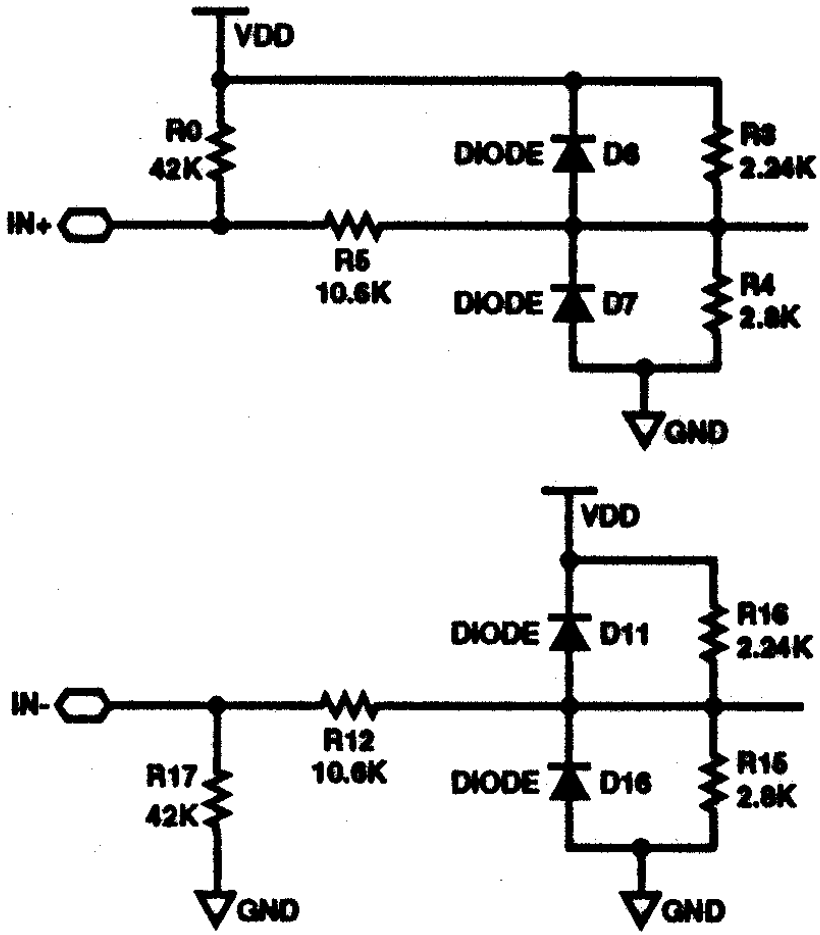
Die Characteristics

- **Die Dimensions: 2140μm x 3290 μm x 533μm ± 25.4μm**
- **Backside Finish: Silicon**
- **Passivation:**
  - **Type: SiO_2**
    - **»Thickness: 800nm ± 100nm**
- **Metallization:**
  - **M1: Mo/TiW**
    - **»Thickness: 580nm**
  - **M2: Al/Si/Cu**
    - **»Thickness: 1000nm ± 100nm**
- **Substrate Potential: Internally connected to V_{DD}**
- **Worst Case Current Density: < 2.0E5 A/cm^2**
- **Transistor Count: 315**
- **Process: Radiation Hardened CMOS, AVLSI**

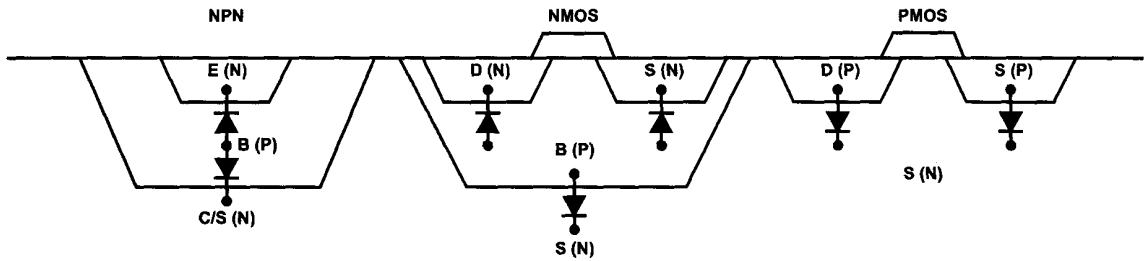
Die Layout


AIN (1)
VDD (16)
BIN (15)
1992
AIN (2)
(14) BIN
AOUT (3)
(13) BOUT
50634
ENAB (4)
(12) ENAB
HARRIS
COUT (5)
(11) DOUT
CIN (6)
(10) DIN
(7) CIN
(8) GND
(9) DIN

Schematic of the HS-26C(T)32RH input structure



Parasitic Diodes for Each Output



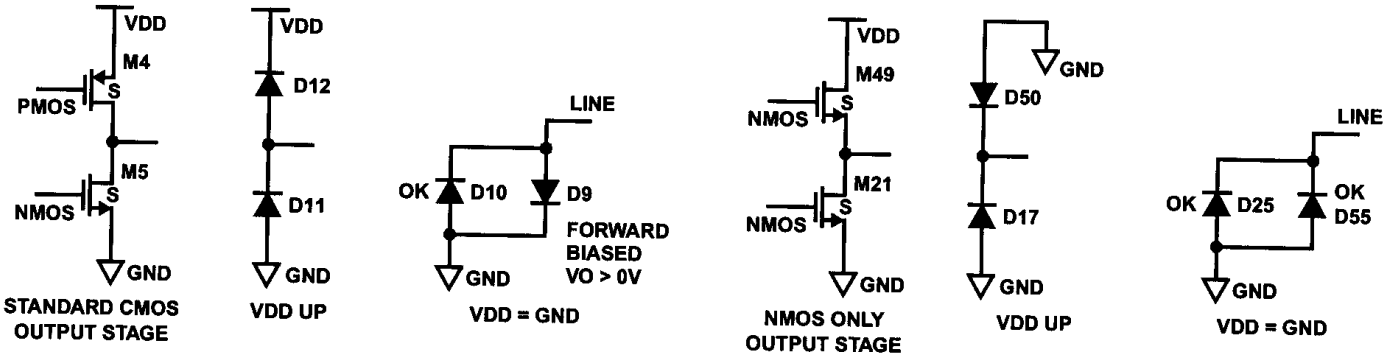


FIGURE 3A.

FIGURE 3B.

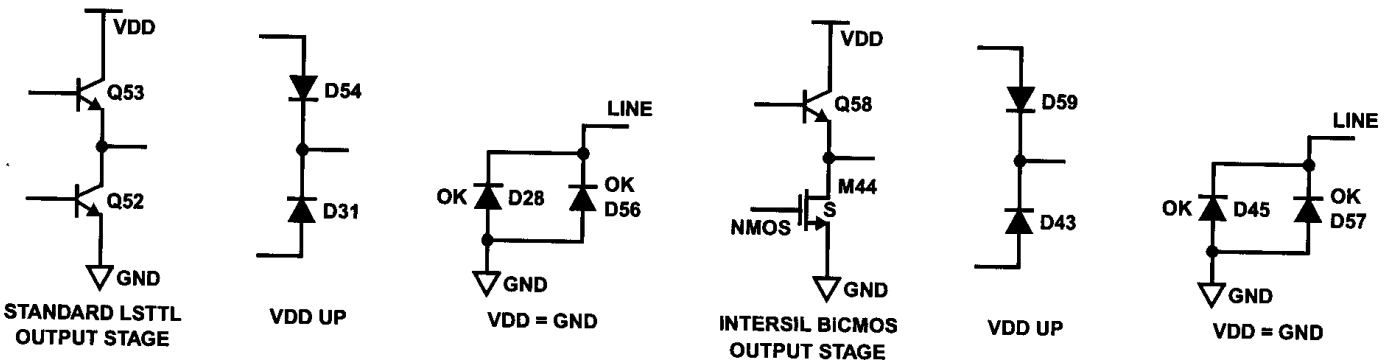
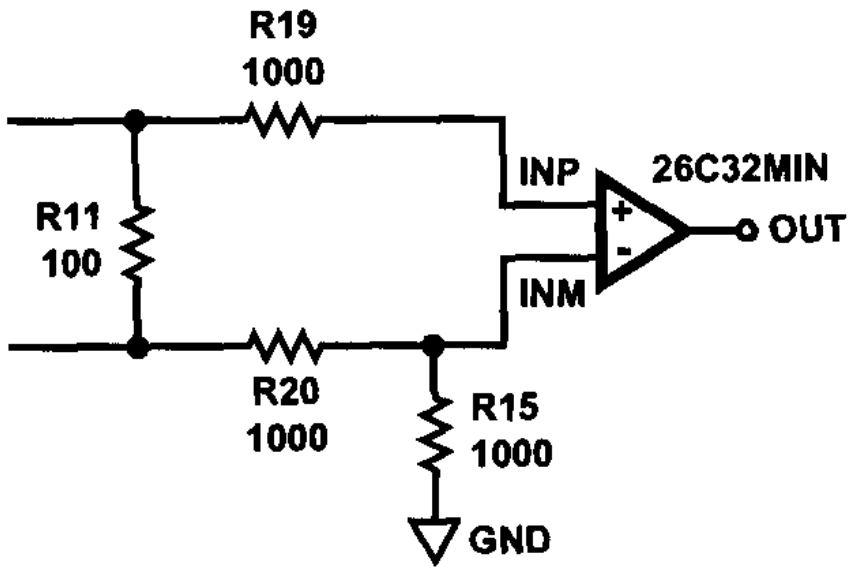


FIGURE 3C.

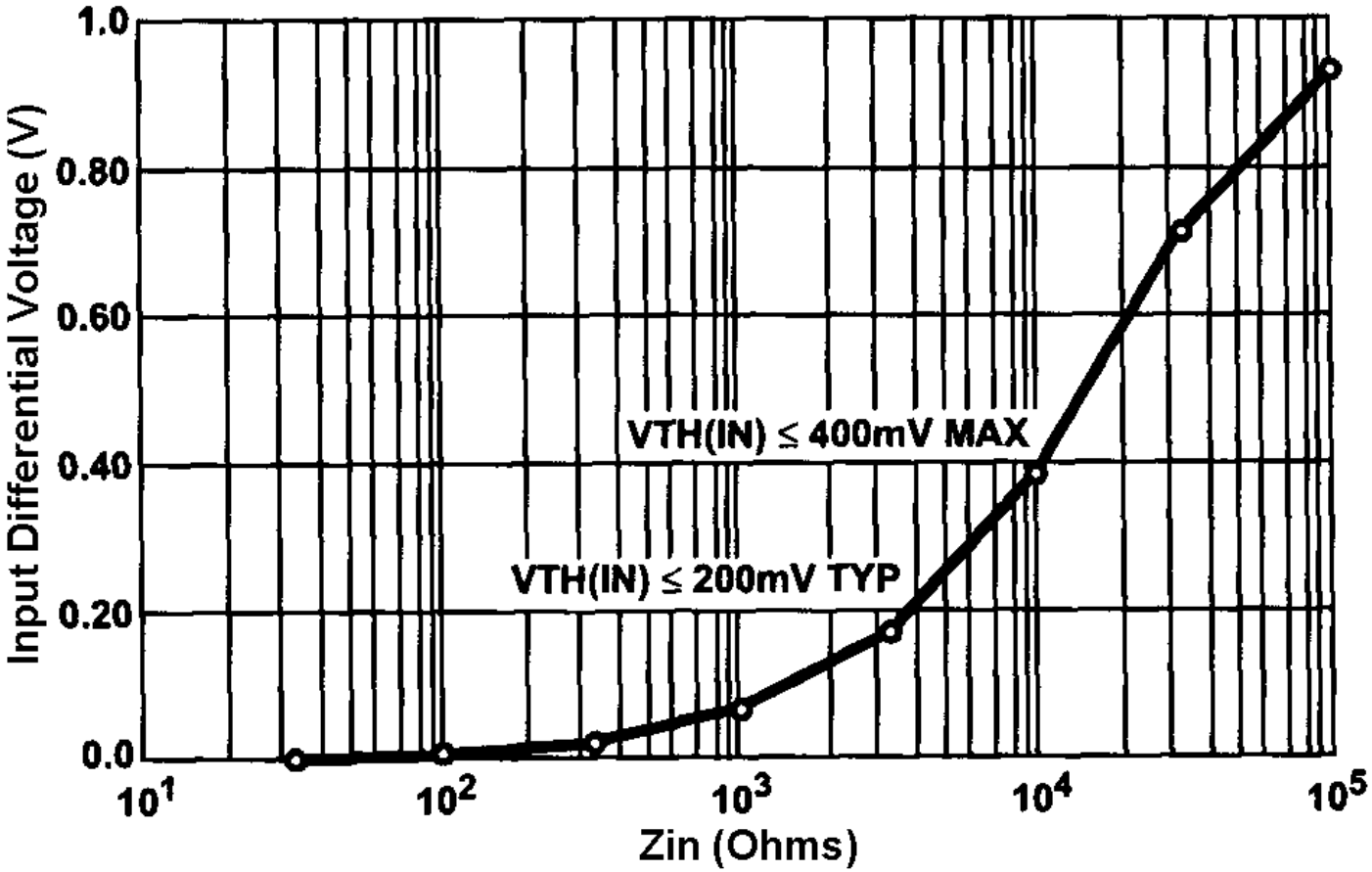
FIGURE 3D.

Adequate input differential voltage for open line fault conditions



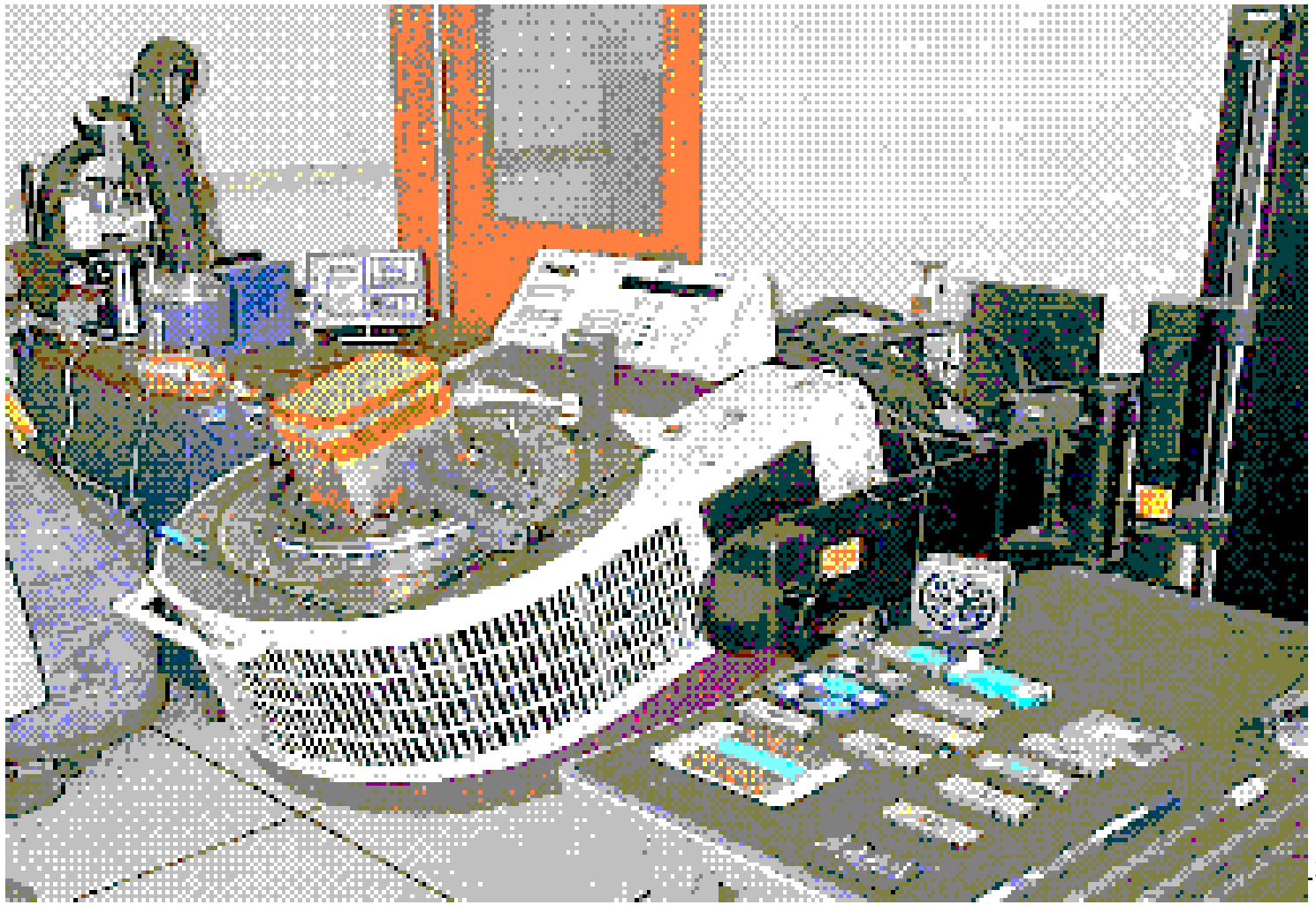
- **Produces too small an input differential voltage in the open-line fault condition**
- **The internal input bias network is shunted by the termination resistor**
- **The internal input bias network is supplemented externally to compensate for the termination resistor**

Input Fail/Safe Differential vs Z_{in} (Open)



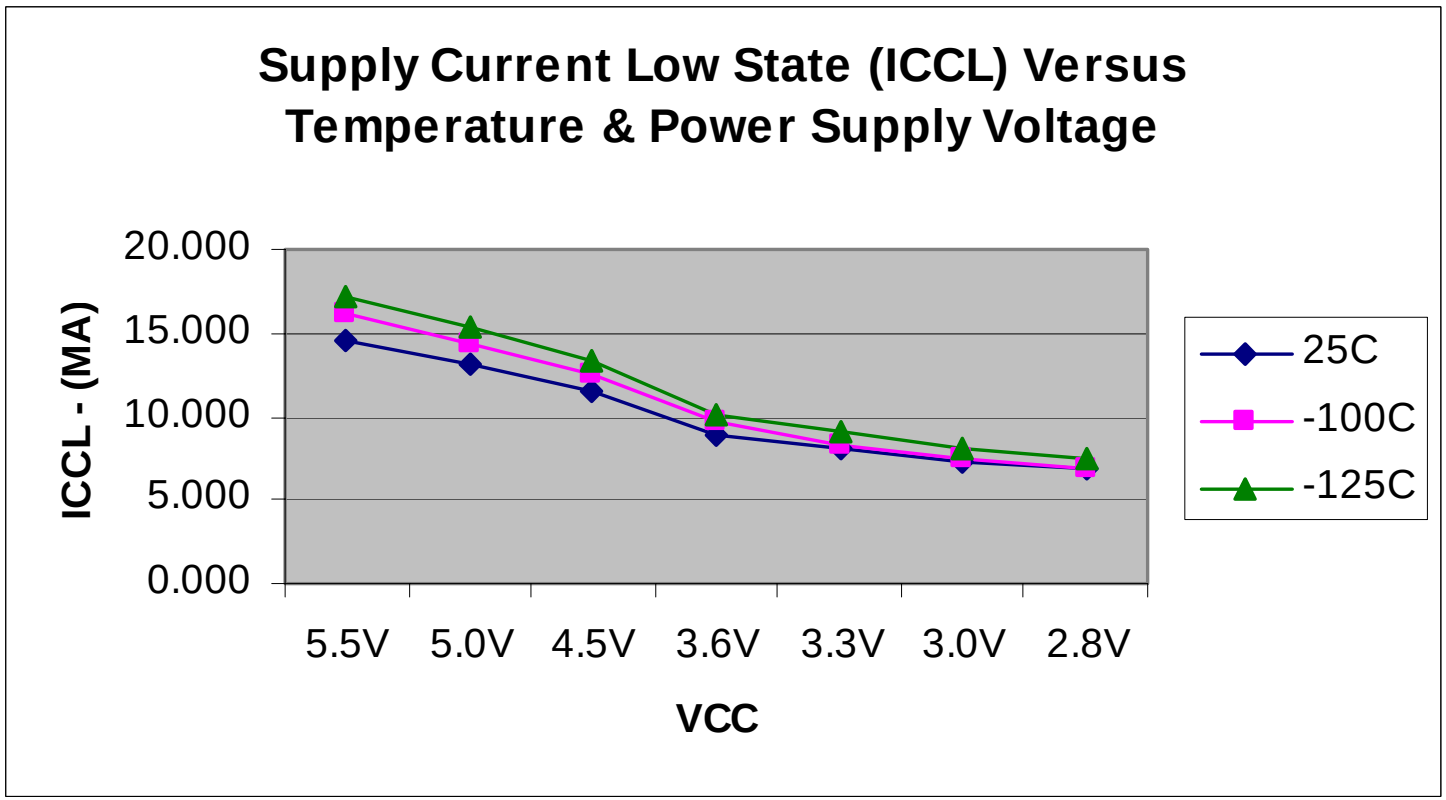
Test Setups

Performance of Rad-Hard Quad Receivers at Extreme Temperatures



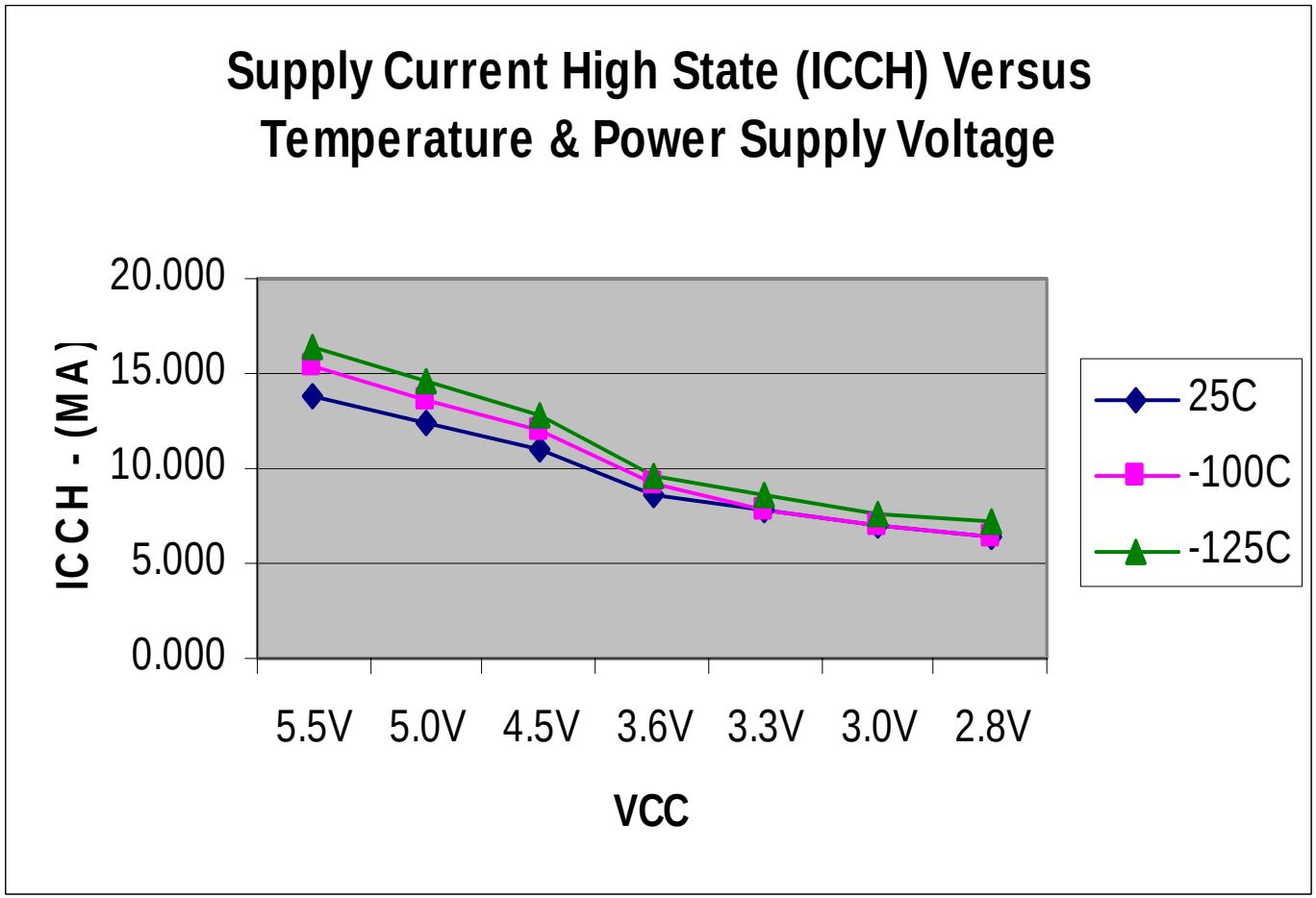
Characteristics of the quiescent power supply currents

Performance of Rad-Hard Quad Receivers at Extreme Temperatures



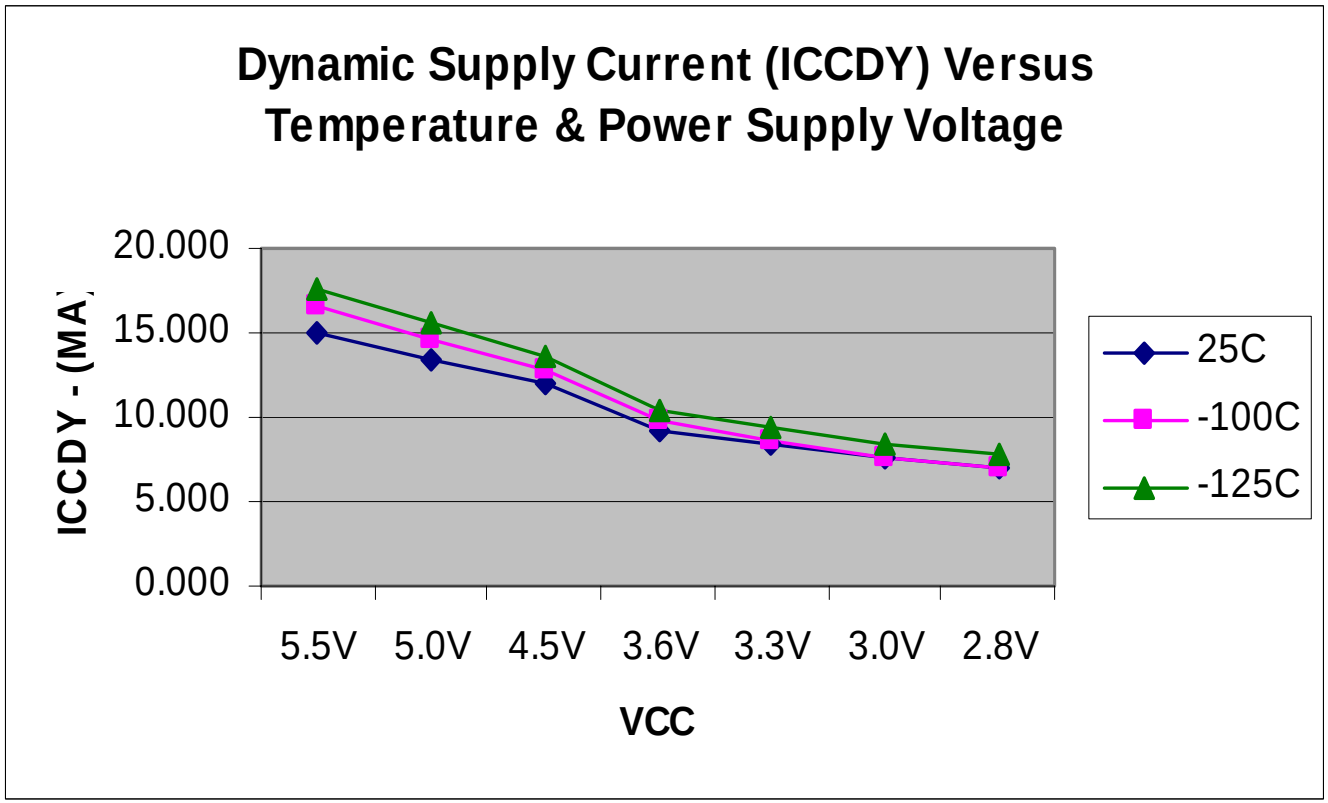
Characteristics of the input current

Performance of Rad-Hard Quad Receivers at Extreme Temperatures



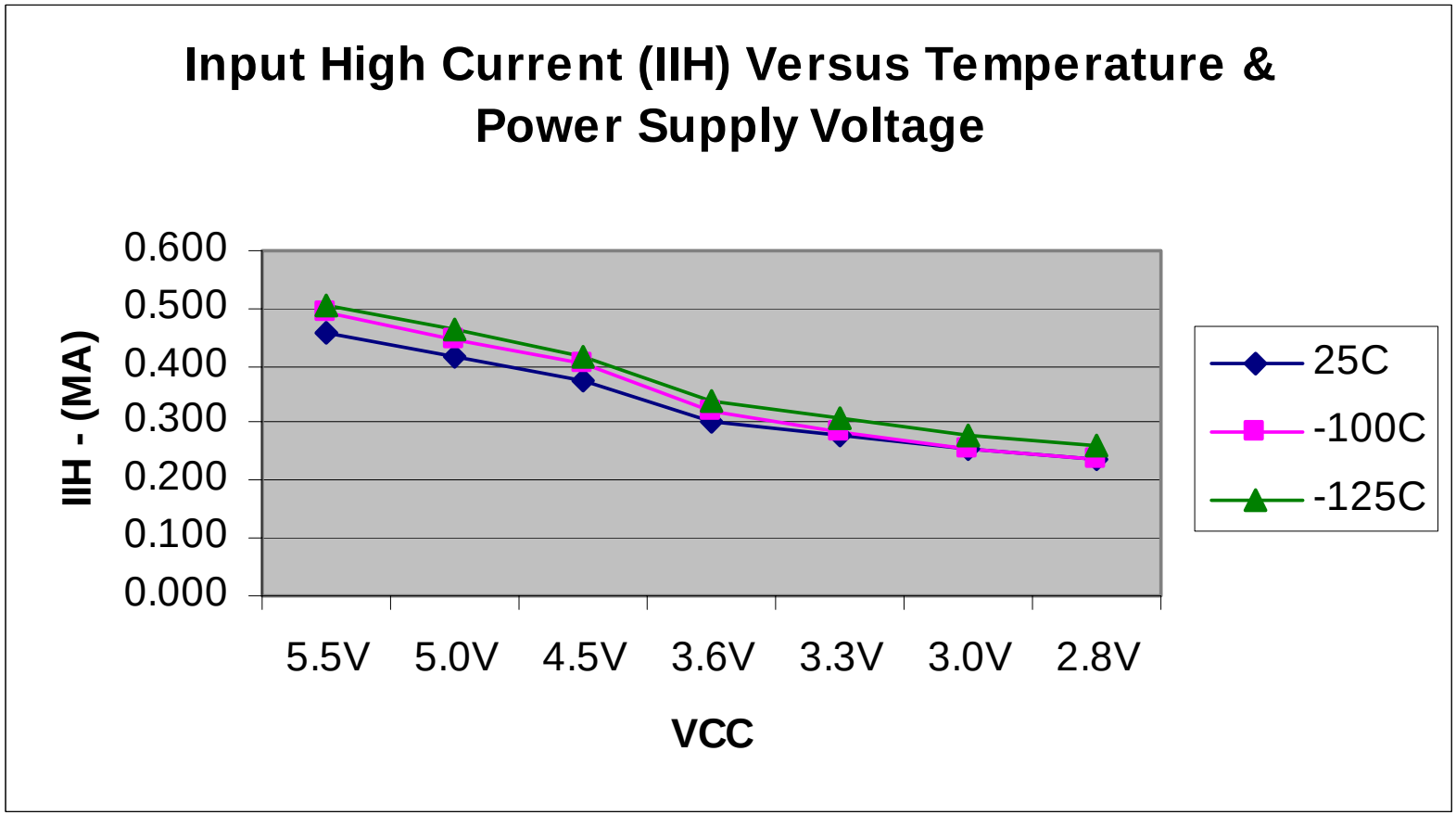
Characteristics of the dynamic supply current

Performance of Rad-Hard Quad Receivers at Extreme Temperatures



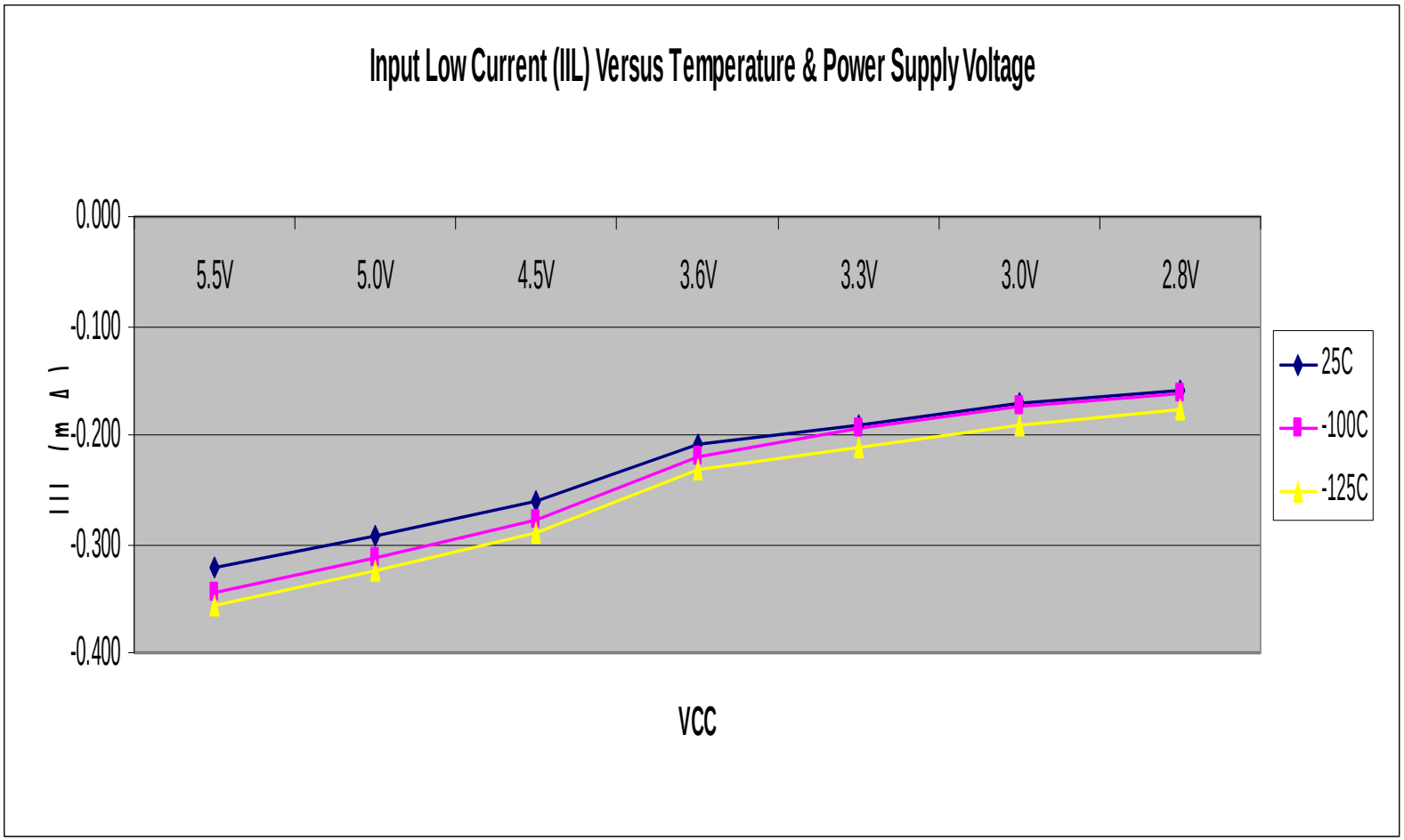
Characteristics of the input high current

Performance of Rad-Hard Quad Receivers at Extreme Temperatures



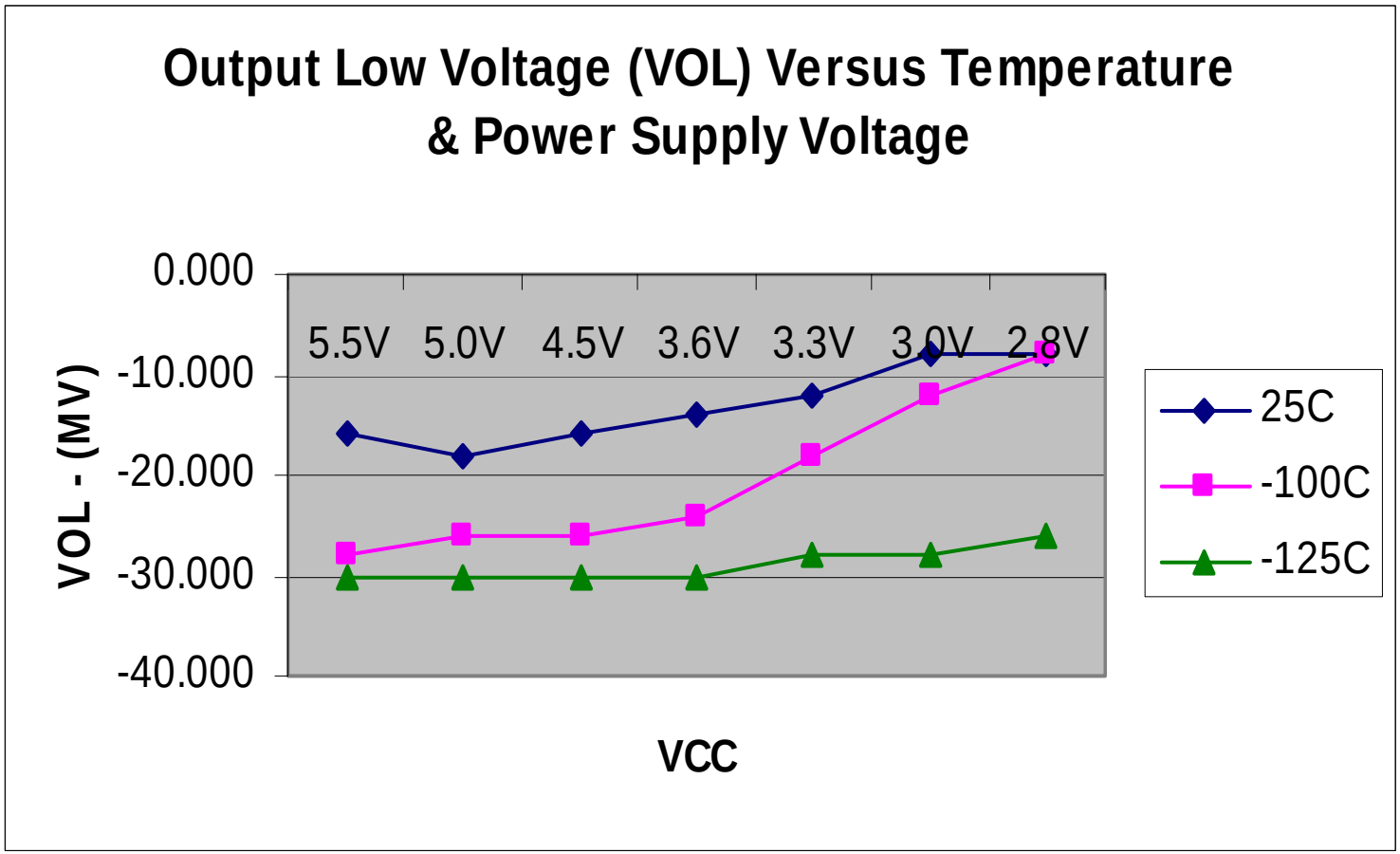
Characteristics of the input low current

Performance of Rad-Hard Quad Receivers at Extreme Temperatures



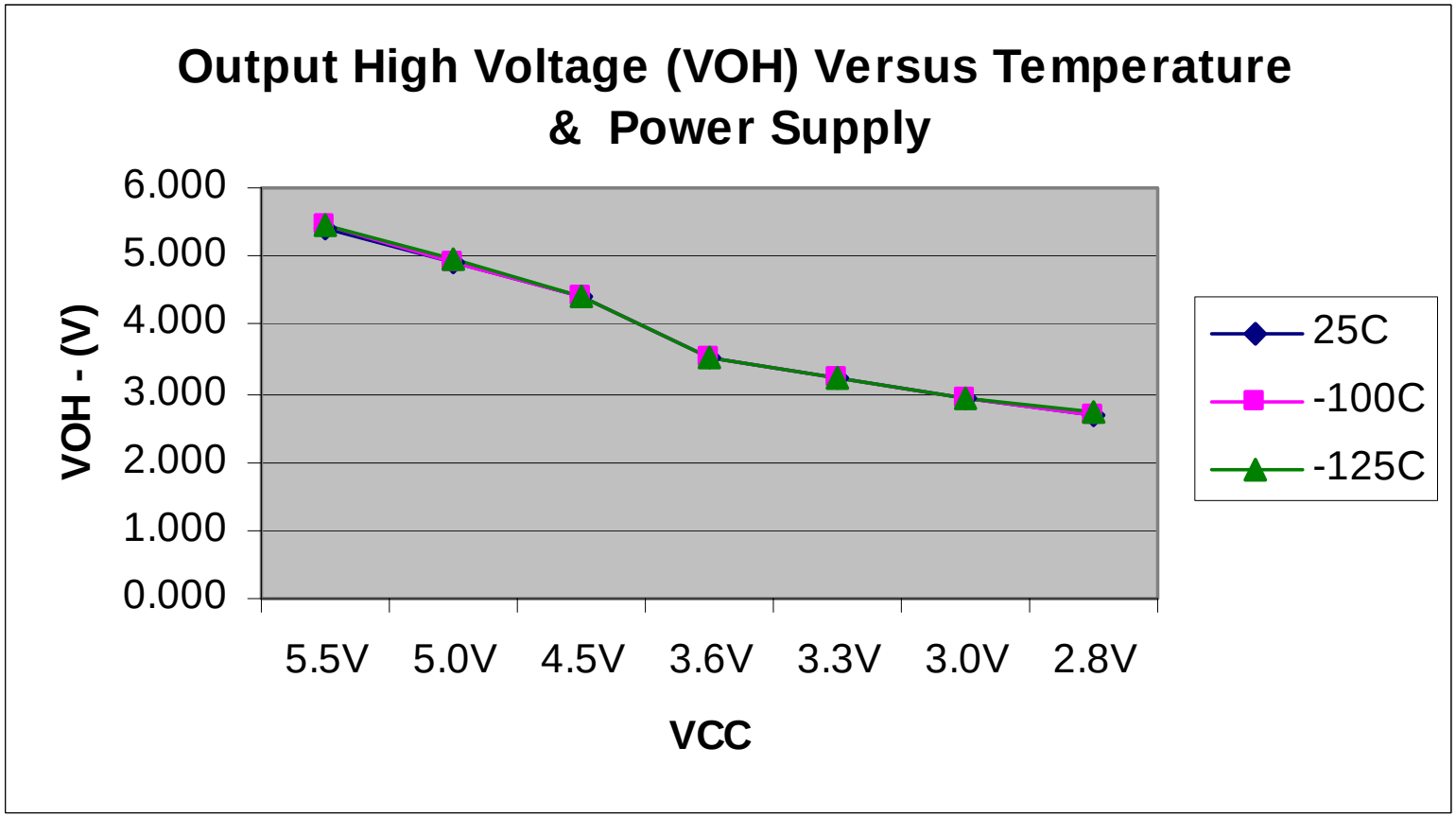
Characteristics of the output low voltage

Performance of Rad-Hard Quad Receivers at Extreme Temperatures



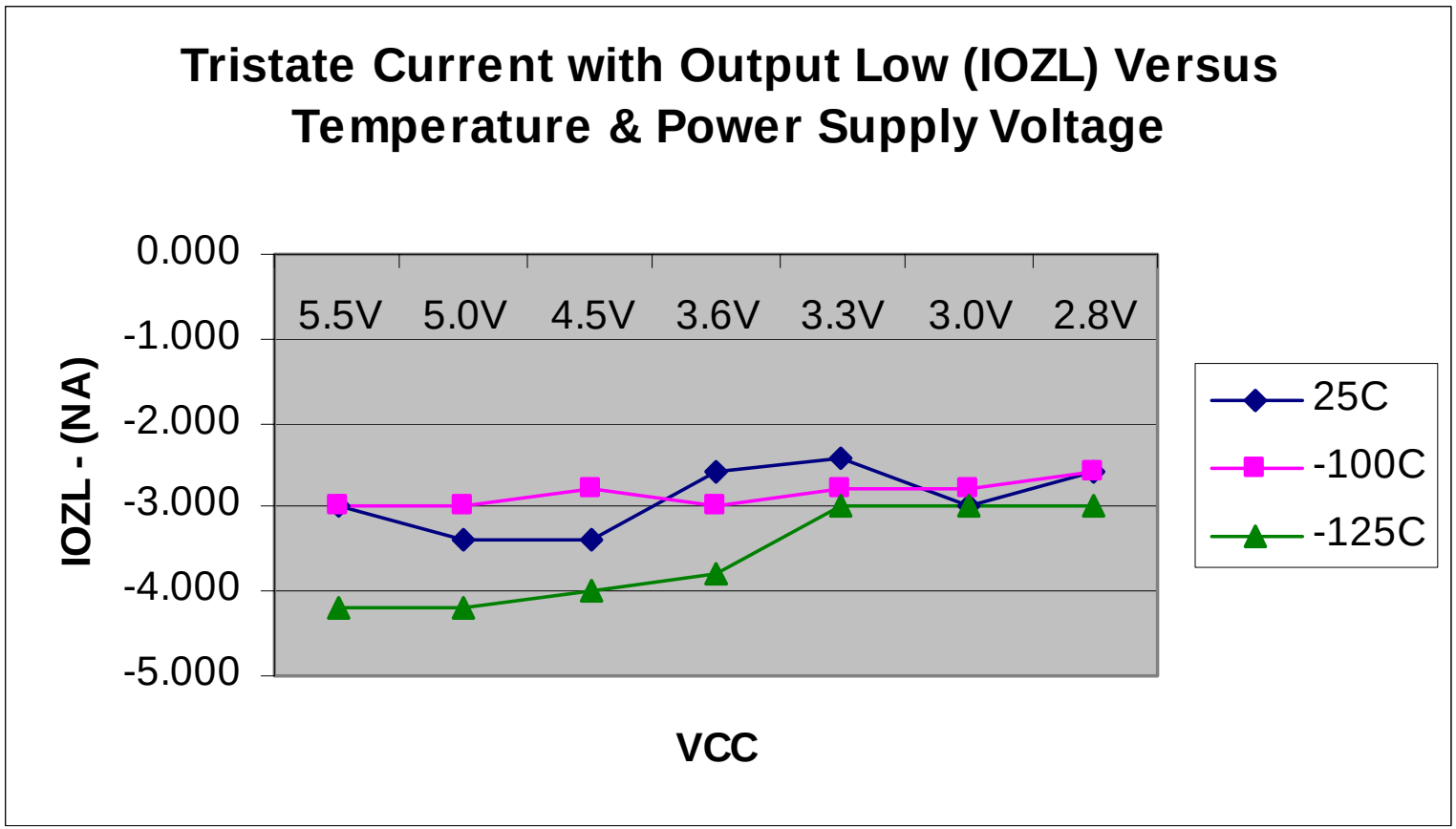
Characteristics of the output high voltage

Performance of Rad-Hard Quad Receivers at Extreme Temperatures



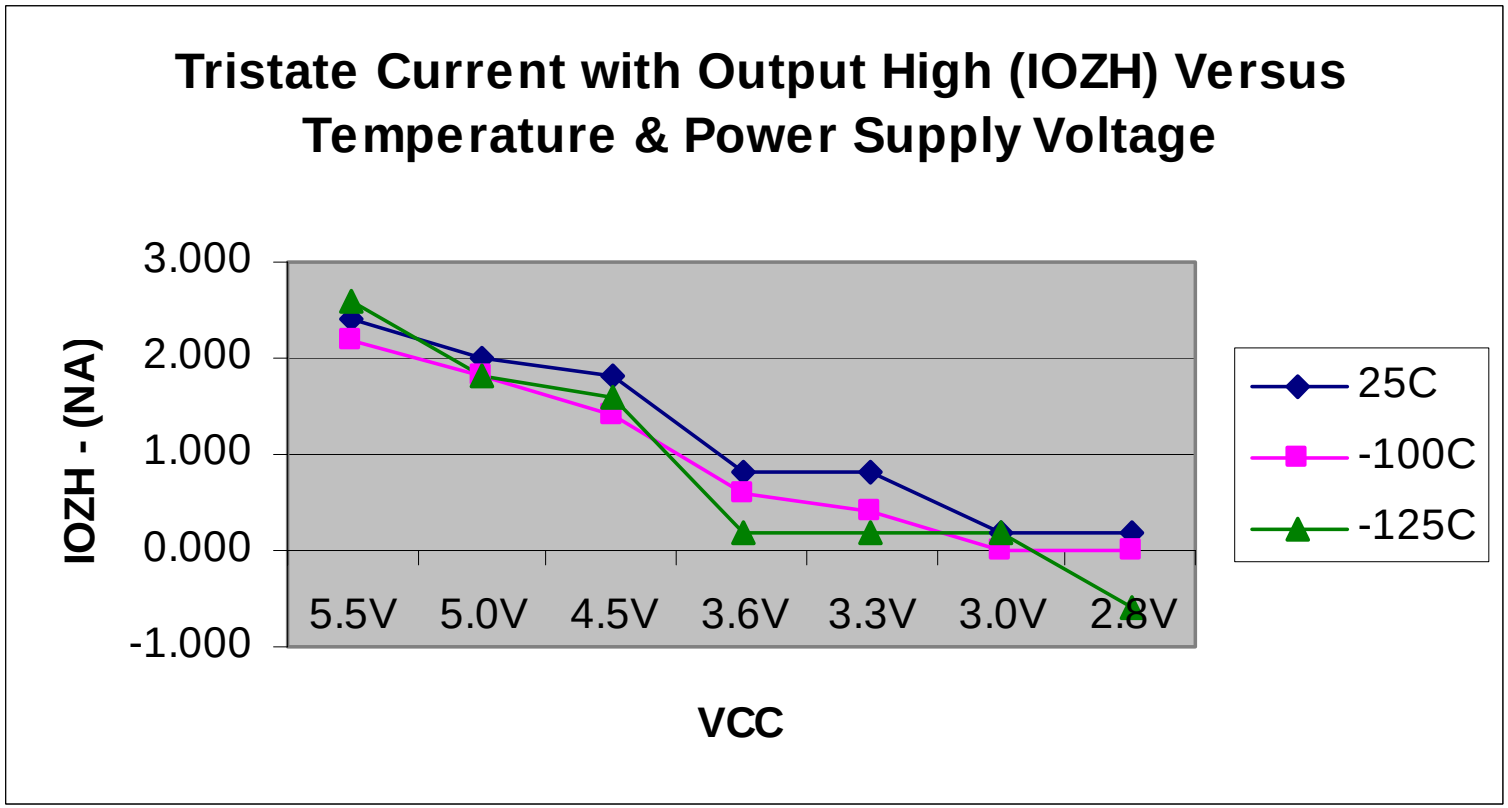
Characteristics of the tri-state leakage current for output low

Performance of Rad-Hard Quad Receivers at Extreme Temperatures



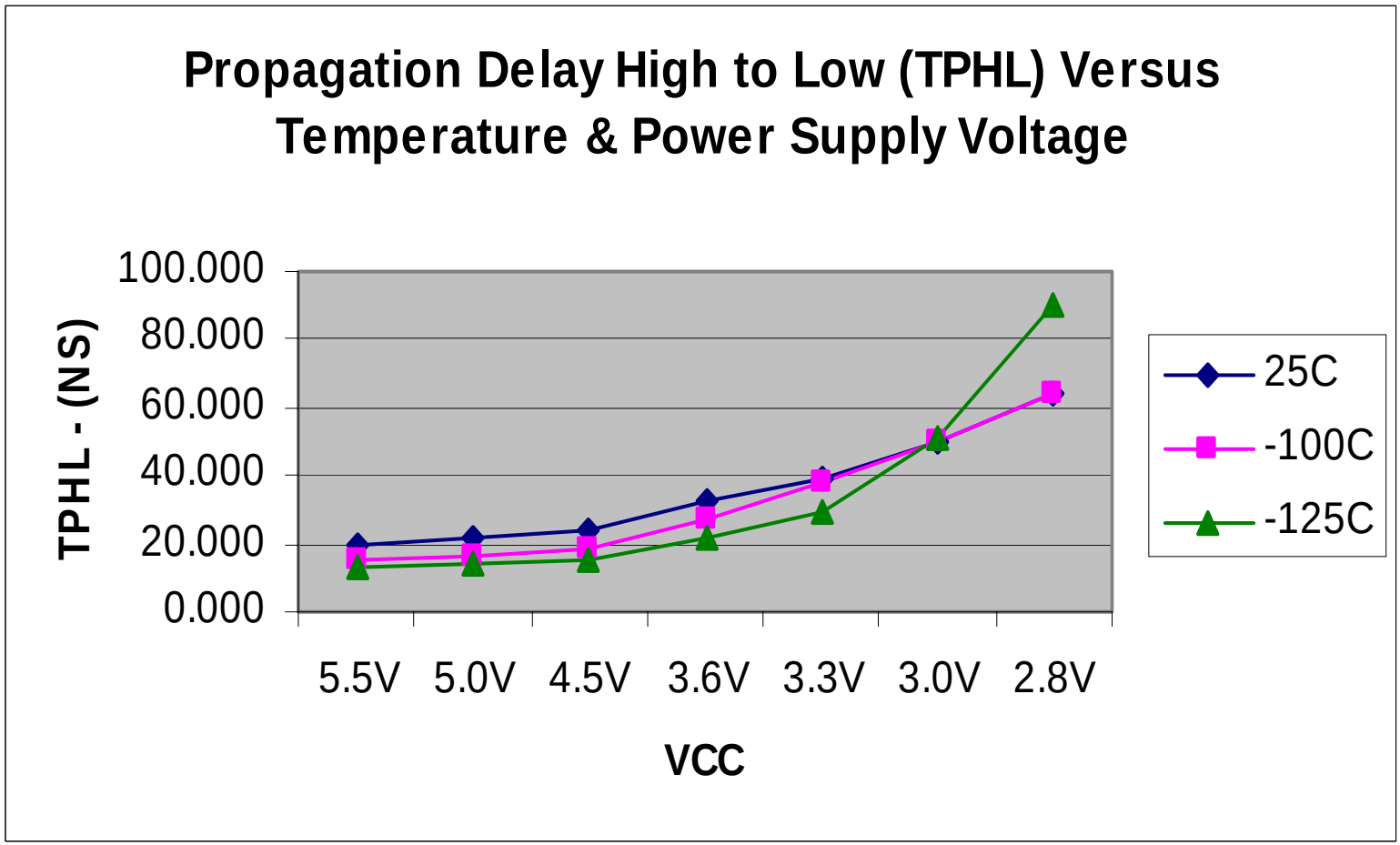
Characteristics of the tri-state leakage current for output high

Performance of Rad-Hard Quad Receivers at Extreme Temperatures



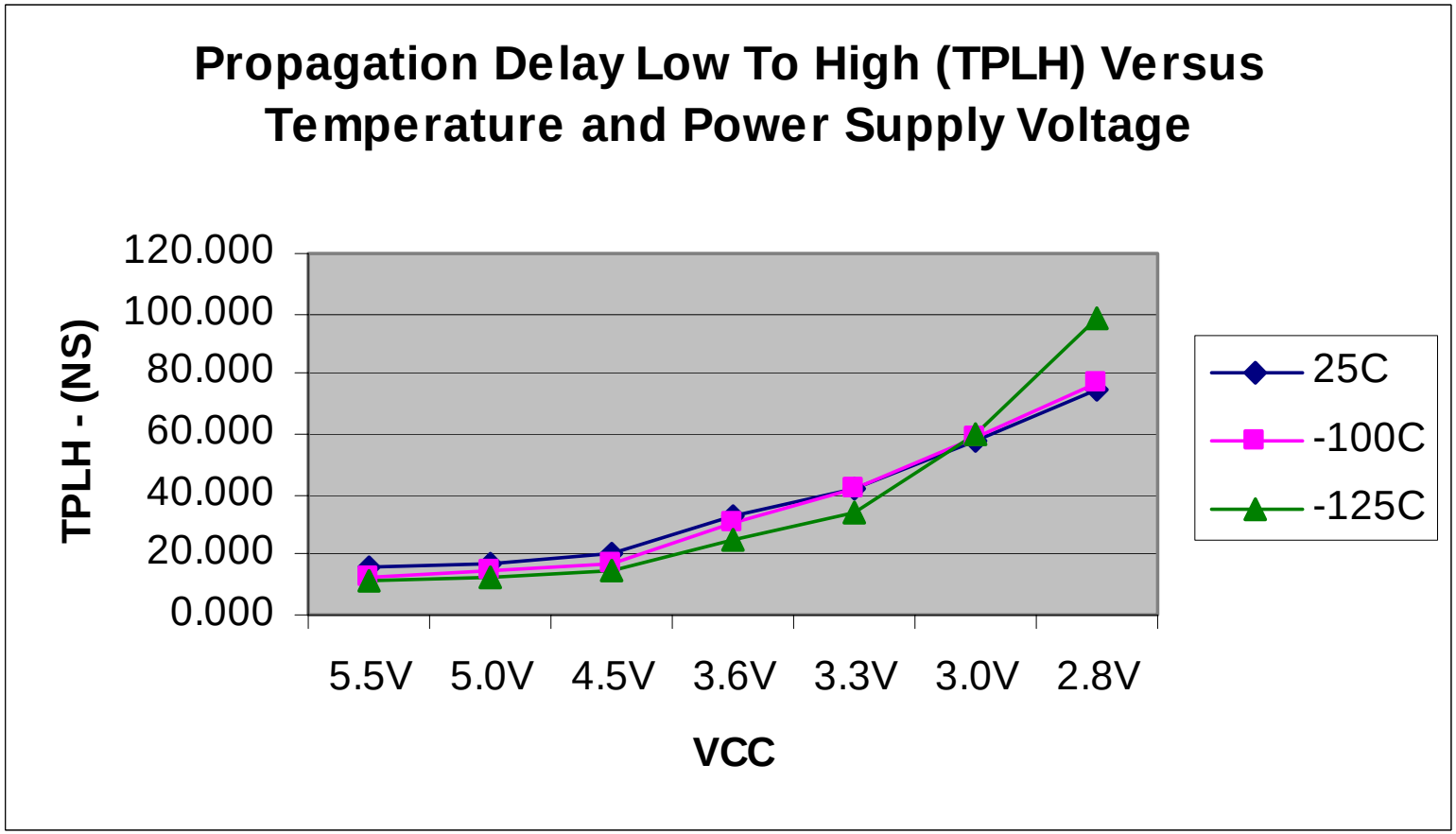
Characteristics of the propagation delay times from high to low state

Performance of Rad-Hard Quad Receivers at Extreme Temperatures



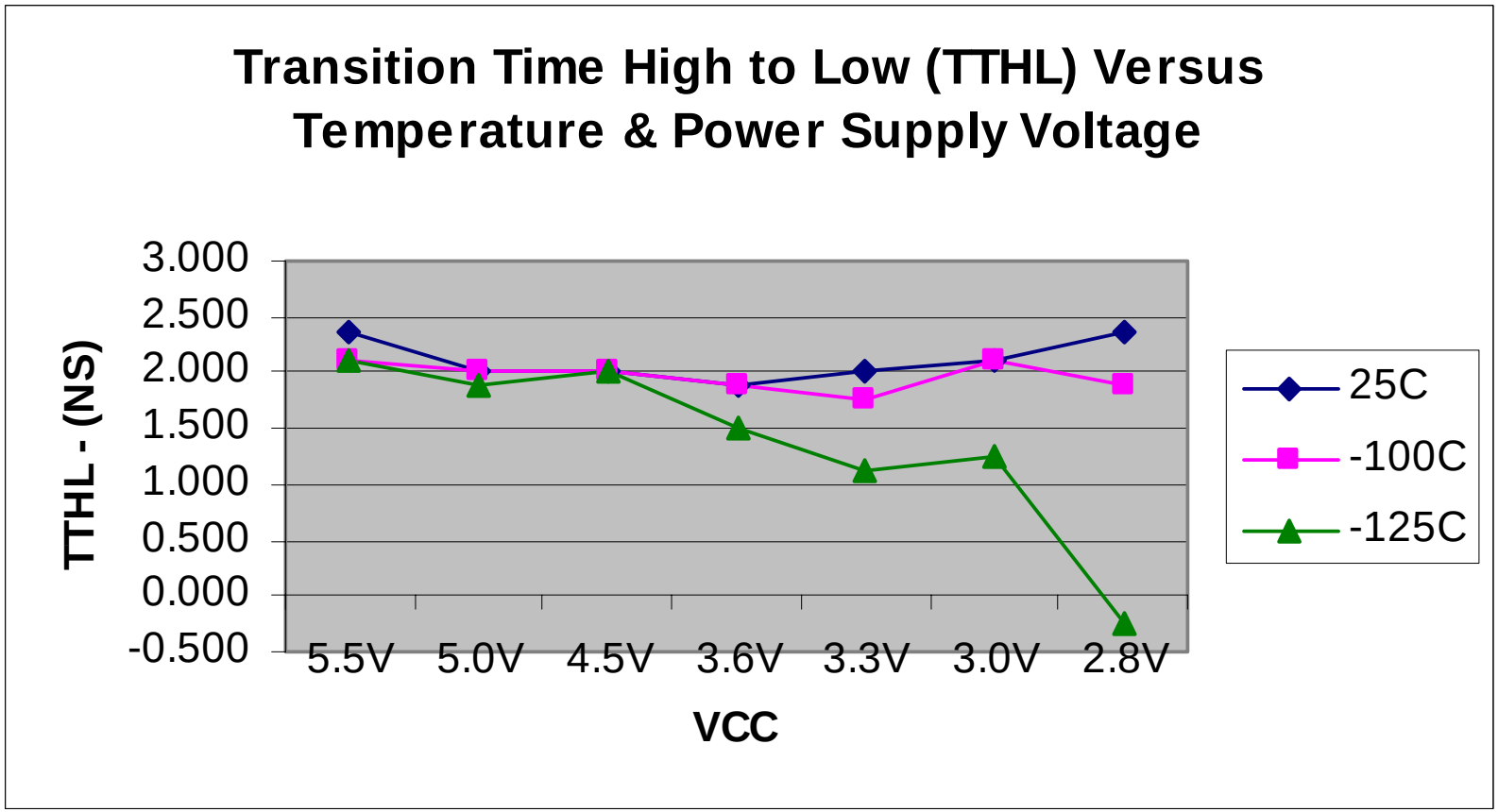
Characteristics of the propagation delay times from low to high state

Performance of Rad-Hard Quad Receivers at Extreme Temperatures



Characteristics of the transition times from high to low state

Performance of Rad-Hard Quad Receivers at Extreme Temperatures



Conclusions

Performance of Rad-Hard Quad Receivers at Extreme Temperatures

- **The test results of the basic parameters of a radiation hardened quad receivers at extreme cold environment indicates that the device can be applied for the potential application in Mars exploration missions even at -125 ^{o}C if the operating parameters such as power supply voltages chosen properly.**

Recommendations

Performance of Rad-Hard Quad Receivers at Extreme Temperatures

- **We do not recommend using this part below 3V supply voltage in applications requiring operation down -125°C.**
- **The output rise and fall times, t_{TLH} and t_{THL}, were well within the SMD max limits of 12ns at 5V±10% and 15ns at 3.3V ± 10%.**
- **The parts though exhibited anomalous behavior at the conditions of 2.8V supply voltage and low temperatures.**

Acknowledgements

The authors are grateful to their numerous colleagues including Jose Uribe of JPL for providing technical support for this study. In particular, the authors would also like to thank their colleagues at JPL for providing suggestions for the improvement of this device qualification for potential space missions. The authors appreciate the support of NASA HQ.

The study described in this report was carried out by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.