Building Reliability into ASIC Design

Jonathan Perret
Jet Propulsion Laboratory

Work performed under the Innovative Parts and Packaging Assessment and Qualification (IPPAQ) task within the NEPP Program has identified the key processes for qualifying complex mixed signal ASICs for space applications. The emphasis in this work was to achieve qualification by including design validations that are completed during the ASIC design phase, rather than after the fact when the ASIC has been built. A methodology flow was implemented to control the design flow and verification steps for both digital and analog mixed signal devices making up a complex ASIC. This design flow verification methodology has been used to implement reliable ASIC designs for an actual flight project application. Specific design requirements were developed in order to standardize the Europa PDR and CDR design review process for ASICs to be used in Europa flight systems. In the course of this implementation, the following seven new design principles/best practices were developed to help insure the production of flight qualifiable ASICs:

- Verify that the ASIC design is functional in the system via behavioral modeling prior to fabrication.
- Verify that ASIC hardware and software designs are compatible prior to fabrication.
- Verify back-annotated ASIC netlist prior to fabrication.
- Validate IP design compatibility prior to ASIC integration.
- Validate ASIC specification quality and control.
- Validate that screening tests are compatible with ASIC design verification prior to fabrication.
- Validate node-toggle (IDDQ), stuck-at-fault test coverage of digital ASIC designs prior to fabrication.

These design principles are generally applicable and will help to insure that ASICs for NASA flight systems have built-in high probability of being easily flight qualified.