Heavy Ion Single Event Effects Test Results for Anadigm AN10E40 Field Programmable Analog Array (FPAA)

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INTRODUCTION

This study was undertaken to determine the radiation-induced single event transient (SET) and single event latchup (SEL) sensitivity of the AN10E40 Field Programmable Analog Array (FPAA) manufactured by Anadigm Inc. Heavy ion testing was performed at Brookhaven National Laboratory's (BNL) Single Event Upset Test Facility (SEUTF). The output of the device was monitored for SETs and the supply current was monitored for SEL.

DEVICE DATA

The AN10E40 FPAA brings to analog, what FPGA's brought to digital; extremely rapid production and prototype circuit realization with field re-programmability. The AN10E40 consists of a 4 x 5 matrix of fully configurable switched capacitor op-amp cells, enmeshed in a fabric of programmable interconnect resources. These programmable features are directed by an on-chip SRAM configuration memory. The SRAM configuration memory is initialized on power up via an on off chip serial PROM or through the AN10E40'S standard microprocessor peripheral interface. All devices had the following markings: anadigm AN10E40 0051 AYV73901.1. There were no markings on the bottom of the package.

TEST FACILITIES

Heavy Ion Test Facility: BNL SEUTF
Flux: $1.5x10^4 – 5.4x10^4$ particles/cm^2/s.
Particles: Heavy Ions measured in Linear Energy Transfer (LET)

Ion	LET at normal incidence (MeV·cm^2/mg)
Si-28	7.88
Cl-35	11.44

TEST METHODS

General Methodology

The test setup was comprised of an Anadigm evaluation board that housed the DUT. From the evaluation board, a configuration of a gain stage of 5 was programmed into the DUT. A function generator provided a 1kHz signal, riding on a 2.5V rail, to the input and an output of a gain of 5 was captured using a 1 GHz Tektronix TDS784C digitizing oscilloscope. A counter built into the scope was used to count the number of triggers (SETs). An HP6626A power supply provided input voltage to the DUTs. Due to the nature of the evaluation board, the current could only be monitored for the entire board not the device alone. Typical current drawn by the board was 50-65mA with a SEL defined as >90mA.

Software

Customized LABVIEW® software provided user interface to control signals to the DUTs. The software also automatically monitored the DUT output via a trigger from the hardware and generated an SET/SEL file history.

Test Techniques

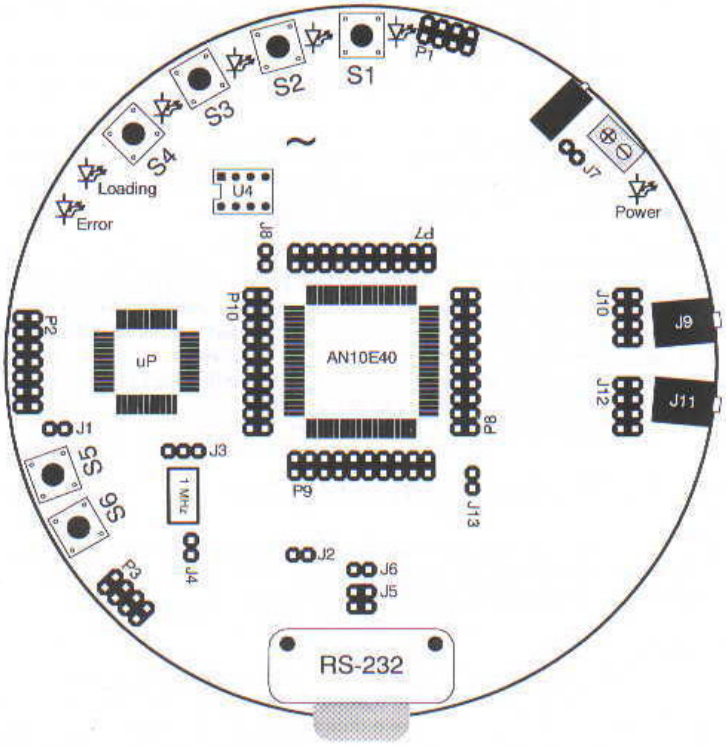
Tests were performed on the DUTs to measure the SET/SEL susceptibility as a function of particle LET for the specific application described in this report. The test setup did not allow for fluctuating temperatures, therefore temperature effects were not considered.

RESULTS

Two devices were tested, DUT 2 and DUT 3. DUT 2 and DUT 3 experienced SETs and loss-of-configuration errors at an LET of 11.44 MeV·cm^2/mg. DUT 2 was experiencing SETs with the beam off after approximately 10 krads(Si) total dose. DUT 3 also experienced non-destructive SEL at a threshold LET of 19.9 MeV·cm^2/mg (Cl-35 at 55°). Following these SELs, the current to the test board increased by a factor of two. The device reset after power cycling. It should be noted that due to the SETs, loss-of-configuration errors and SELs overlapping, it was not possible to reliably calculate cross-sections. However, one can safely predict an overall error rate by assuming a combined cross-section of ~1x10^{-5} cm^2, remembering that this includes latchup. Information about the device and evaluation board follows.

Development System Board Details

The AN10DS40 has everything you need to investigate the use of an AN10E40 FPAA as a peripheral to a microprocessor or as a stand alone device. The board has switches, connectors and sockets suitable for demonstration many of the devices possible uses.



Switches

Push Button Switches S1 through S4

As shipped from the factory, the AN10DS40 is ready to demonstrate the versatility of the AN10E40 FPAA. Simply power the board up and hit any one of the S1 through S4 switches. Nearly instantly, the microcontroller passes a segment of its Flash memory down to the AN10E40. After this very brief configuration sequence, the AN10E40 will be operating using the configuration associated with that section of Flash associated with the button pressed.

The P1 connector is wired in parallel to these 4 switches, allowing your own off board logic to emulate the closing of these 4 switches.

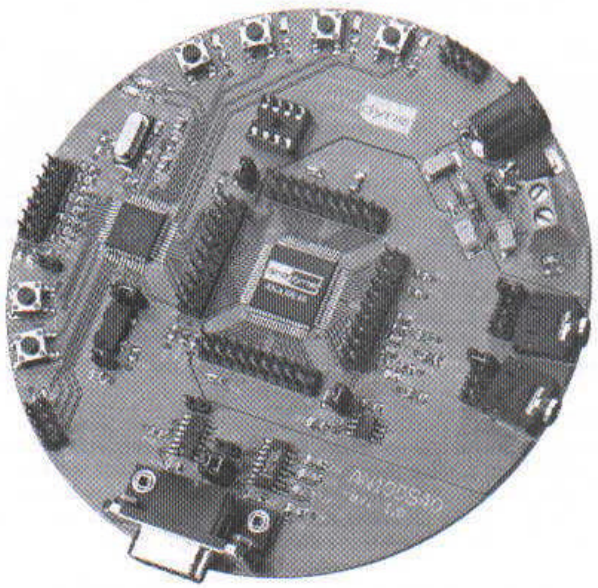
Push Button Switch S5 Reset

Pressing S5 resets the on board microcontroller, bringing the entire system back to its power on reset state. Access to this same RST signal is also provided on the P3 SPI connector.

2

A quick explanation of what is on board

Starting at 6 o'clock and working our way around clockwise, we first see a standard 9 pin RS-232 connector. Just behind the connector is jumper block J5, that allows the port to present itself either as a DCE or DTE interface. For the most common PC and cable combinations, the factory setting of DCE works fine.



P3 is a SPI port connection. Out of reset the design system watches for RS-232, SPI or push button activity. The design system is configures as a SPI slave. Any standard SPI master can talk directly to the AN10DS40 with no need for jumper setting or code changes.

IRQ and RESET buttons are provided. The reset button does the obvious thing, it resets the AN10DS40 back to its power up reset state. The IRQ button will cause an ABORT interrupt service routine to run. No matter what the AN10DS40 happens to be doing at the moment, pressing the IRQ button will take the ABK back to the IDLE state.

the 14 pin P2 connector brings a set of FPAA configuration signals off the board to facilitate connection to your own target system. Shorting jumper J1 causes the microcontroller to re-route configuration signals from the on board FPAA to this External Target Array interface.

The upper left quadrant of the board is occupied by 4 push button switches. Hitting any one of these 4 buttons tells the microcontroller to download the associated pre-stored configuration to the FPAA (either on board of to the target system). Adjacent to the switches is the P1 connector, which brings the pushbutton signals to a hand connector. A logic signal can be used to emulate a button press.

The P6 connector allows connection of any regulated 8-12 VDC power supply. Behind P6 is a 5 volt linear regulator. A pair of screw terminals is also provided if you should desire to bypass the on board voltage regulator (open jumper J7) and connect your own power.

conditions. Consider how a single physical circuit can be used in all of your different system designs. Consider all the advantages that programmable analog will bring to your designs.

AN10E40 Architecture

The AN10E40 is comprised of a 4x5 array of Configurable Analog Blocks (CABs), enmeshed in clocking, switching, local and global routing resources. Nearly every element of the AN10E40 is programmable giving the user tremendous flexibility in the sorts of processing circuits that can be realized.

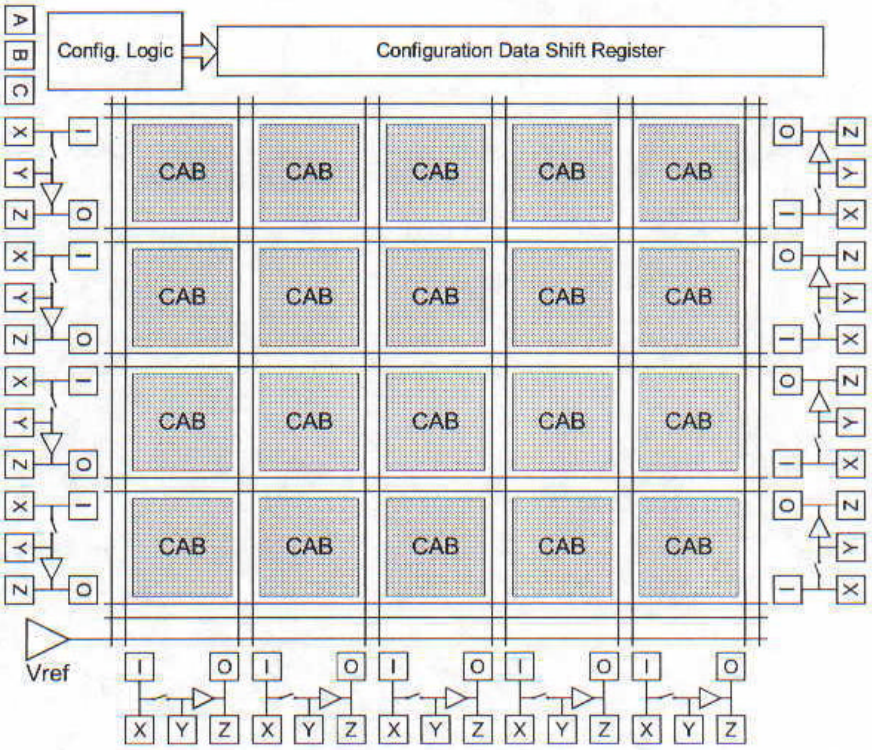


Figure 1. Block Level View of the AN10E40 array

The Configuration Logic and Shift Register work together whenever chip configuration is in process. More on configuration later. The array of CABs is surrounded on three sides by programmable analog input/output cells, 13 in all, with two spare uncommitted op-amps. The lower region of the chip also contains a programmable reference voltage generator.

The Configurable Analog Block

The basic building block of the AN10E40 is the Configurable Analog Block. Each CAB is an op-amp surrounded by capacitor banks, local routing resources, local switching and clocking resources, and global connection points. This collection of hardware enables the CAB to perform just about any function that could be performed with an op-amp and conventional passive components. All analog processing is accomplished with this switched capacitor circuit.