Preliminary Heavy ion Single Event Effects test of ADC 16 bits LTC1608 from Linear Technology. Test Report

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04/02/2002

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1 Introduction

This report gives preliminary heavy ion SEE test data on the 16 bits ADC LTC1608 from Linear Technologies. The main objective of this test was to check the Single Event Latch-up (SEL) sensitivity and get an idea of the Single Event Upset (SEU) sensitivity with a simplified test set-up. This work has been performed in the frame of the NGST project.

2 Tested Devices

The tested devices are described in Table 1.

Type	LTC1608
Function	16 bits, 500 ksps A/D converter
Package	36 pin SSOP
Technology	CMOS
Date code	0120
Package marking	LT0120 LTC1608ACG N41585

Table 1: description of the tested device.

3 Test description

3.1 Irradiation facility

The tests have been performed at BNL in March 2002. The ion beams used are described in Table 2.

Ion	**Energy (MeV)**	**Flux (#/cm2-s)**	**Range (µm)**	**LET (MeVcm^2/mg)**
I-127	313	~5E+04	30	60
Au-197	340	~5E+04	27	82

Table 2: Ions used at TEXAS A&M.

3.2 Test set-up

The part has been tested with the LTC1604/1608 evaluation board. The digital signal is converted back to an analog signal with the 16 bits DAC AD768 evaluation board.

The input signal is a 2 Vpp 1kHz sinewave. The sampling clock is 330 kHz (maximum sampling clock). The output sinewave signal is monitored with an oscilloscope. As soon as the DUT output goes under (or above) a given trigger level set at 150 mV, a SEU is counted. SEU frames are stored on a PC. **With this set-up, only the 6 Most Significant Bits are tested.**

The evaluation board power supply current is monitored during the irradiation. The nominal power supply current is 130 mA. The SEL detection threshold was set at 150 mA.

4 Test results

The test results are shown in Table 3.

Run#	dut#	Angle	Eff LET (MeVcm2/mg)	Eff. Fluence (#/cm2)	SEL	SEU	CrossSection SEL (cm2/dev)	Cross Section SEU (cm2/dev)
139	1	0	59.67	1.04E+07	0	1	0.00E+00	9.62E-08
140	1	0	59.67	1.00E+07	0	2	0.00E+00	2.00E-07
139+140	**1**	**0**	**59.67**	**2.04E+07**	**0**	**3**	**0.00E+00**	**1.47E-07**
141	1	30	68.90	1.00E+07	0	2	0.00E+00	2.00E-07
142	1	45	84.39	1.00E+07	0	3	0.00E+00	3.00E-07
143	1	0	81.78	9.58E+06	0	2	0.00E+00	2.09E-07
144	1	0	81.78	1.00E+07	0	1	0.00E+00	1.00E-07
143+144	**1**	**0**	**81.78**	**1.96E+07**	**0**	**3**	**0.00E+00**	**1.53E-07**
145	1	30	94.43	7.97E+06	1	2	1.25E-07	2.51E-07
146	1	30	94.43	4.86E+05	1	0	2.06E-06	0.00E+00
145+146	**1**	**30**	**94.43**	**8.46E+06**	**2**	**2**	**2.37E-07**	**2.37E-07**
147	1	20	87.03	7.30E+06	1	3	1.37E-07	4.11E-07

Table 3: Test results

The device showed a low SEL sensitivity with LET threshold around 85 MeVcm^2/mg.

A low SEU sensitivity of the 6 Most Significant Bits has been observed. In all cases the device recovered normal functionality after an upset. A typical upset is shown in Figure 1. All upsets show a large deviation from the “normal” output signal.

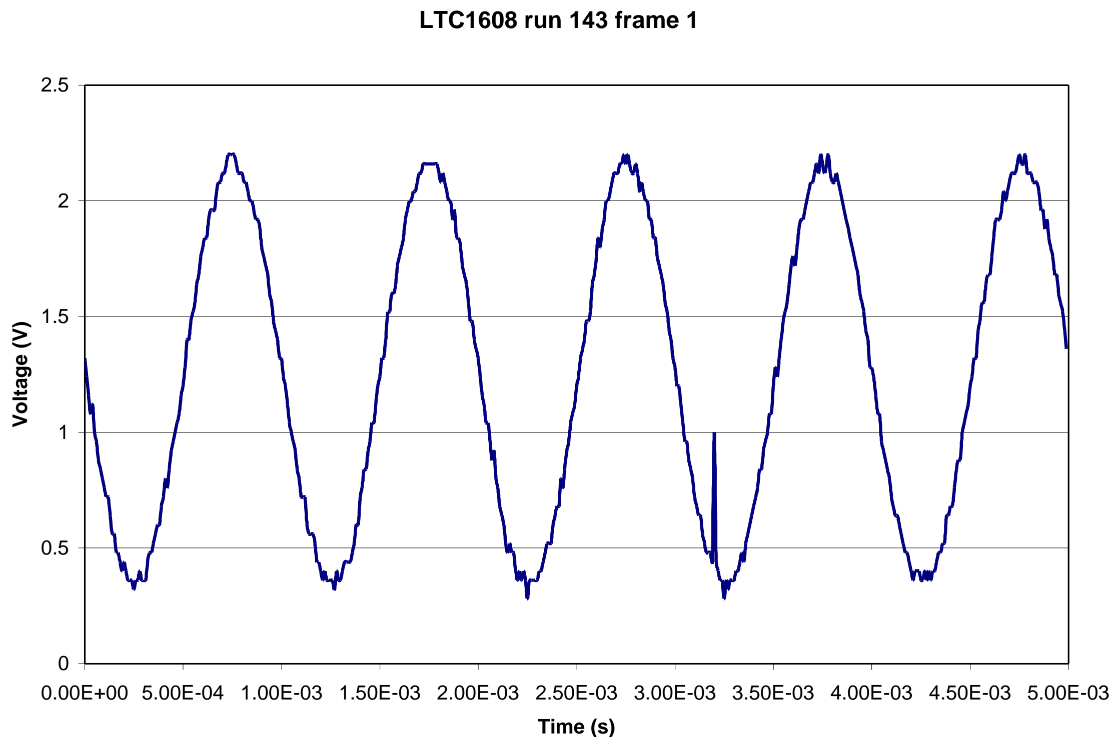

Figure 1: Typical upset, run 143 frame 1.

5 Conclusions

These preliminary tests show that the LTC1608 16 bits ADC has a very low sensitivity to SEL. The SEL LET threshold is around 85 MeVcm^2/mg. The SEU sensitivity of the 6 Most Significant bits is low and no Single Event Functional Interrupt (SEFI) has been observed.

The SEU sensitivity of the Least Significant Bits (LSB) is expected to be higher. An accurate SEU testing is needed in order to validate the use of this device for NGST.