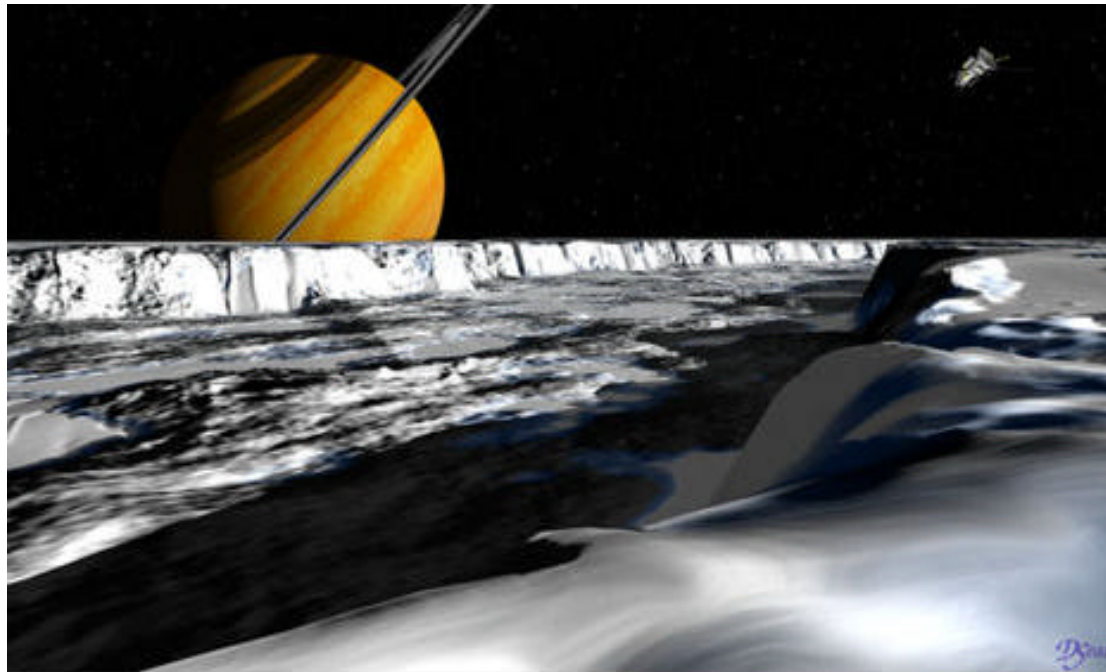
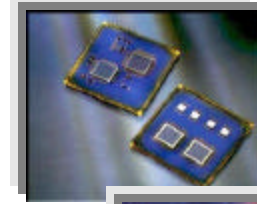




Experience with Plastic Part Evaluations At Cold Temperatures

NASA Electronic Parts and Packaging Program

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Electronic Parts Engineering

AGENDA

Introduction

Cold Temperature Activities

Cold Temperature Capabilities

Test Results

Summary

The work was performed at the Jet Propulsion Laboratory, California Institute of Technology, under contract to the National Aeronautics and Space Administration.



INTRODUCTION



°C	°K	°F
0	273.2	32
-55	218.2	-67
-105	168.2	-157
-125	148.2	-193
-175	98.15	-283

- Missions to MARS/planets/asteroids require electronic parts to operate and survive at extreme cold conditions.
- At extreme cold temperatures many types of cold related failures can occur.
- Office 514 is currently evaluating plastic parts under various cold temperature conditions and applications.
- Evaluations, screens, and qualifications are ongoing on flight parts.



TIMELINE OF COLD TEMPERATURE TEST ACTIVITIES

- **Part performance outside specifications - Now**
- **Temperature cycling – Now**
- **Thermal shock - Now**
- **Cold temperature startup - Future**
- **Extended low temperature operating life – Future**
- **Cold temperature device modeling – Future**
- **Power/temperature cycling – Future**
- **Long term cold storage – Future**



COLD TEMPERATURE ACTIVITIES

Areas requiring further investigation that can impact part reliability under cold temperatures:

- **Material properties & characteristics**
- **Physics/operation of semiconductor devices**
- **Wafer Processing/Component Assembly**
- **Manufacturing/Lead Type**
- **Stress Induced Latent Damage**



TEMPERATURE REQUIREMENTS

(OP/NOP Example)

Allowable Flight

-105°C minimum

Qualification

-125°C minimum

Flight Acceptance

-110°C minimum

Part Test/Eval

-115°C minimum

Part Accept

-110°C minimum

Part Test/Eval

-135°C minimum

Part Accept

-130°C minimum

Part Test/Eval

-120°C minimum

Part Accept

-115°C minimum



EXAMPLES OF PERFORMANCE IMPROVEMENTS NEAR LN₂ TEMPERATURES

- **Copper is seven times more conductive**
- **Chip performance equates to reducing chip geometry by 2X**
- **Devices may operate faster because C_j decreases and m increases**
- **Interconnection delays times are reduced**
- **Sharper signal transitions allow faster clock rates**
- **Memory chips consume less power & require fewer refresh cycles**
- **Thermal management is easier**



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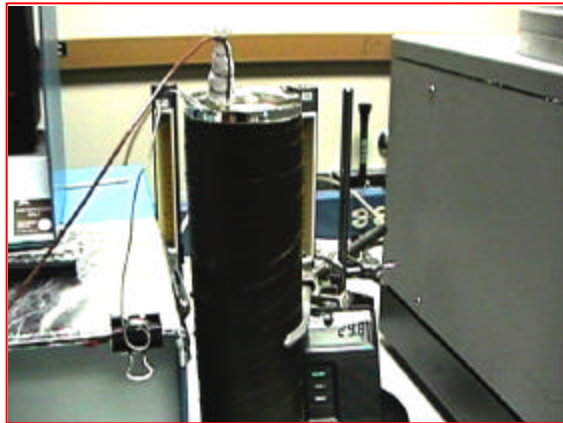
Cold Temperature Capabilities/Developments



-195°C Cold Test Evaluation Chamber



-125°C Cold ATE Digital Tester



-180°C Liquid Nitrogen Bath

IN DEVELOPMENT

-125°C Cold Linear/Mixed Signal Testers



Performance

SCREENING/QUALIFICATION METHODS USED AT COLD TEMPERATURES

GRADE EVALUATED	EXPECTED YIELD	EXPECTED OUTCOME
Commercial 0 to +70C	Low	High No. of Outliers, Large Degradations
Industrial -40C to +85C	Medium	Medium No.of Outliers, Some Degradations
Military -55C to +125C	High	Few Outliers, Few Degradations

Acceptable parts must be within 10-20% of lot parametric distributions at temperature, while accepted lots must yield at least 50% upon completed screening. Qual lots must pass 100%.



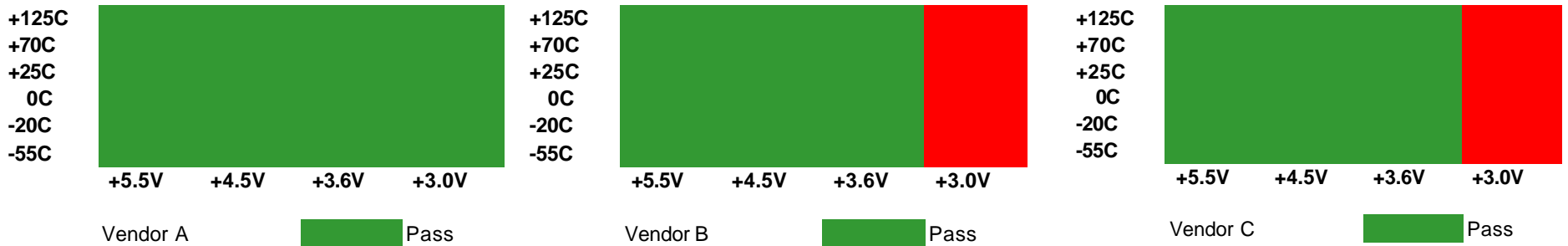
COLD TEMPERATURE TEST RESULTS

COTS SRAMS

Case I

Performance

COTS SRAMS have been evaluated by JPL at military temperature range:



Results:

Three different parts from three different vendors passed.



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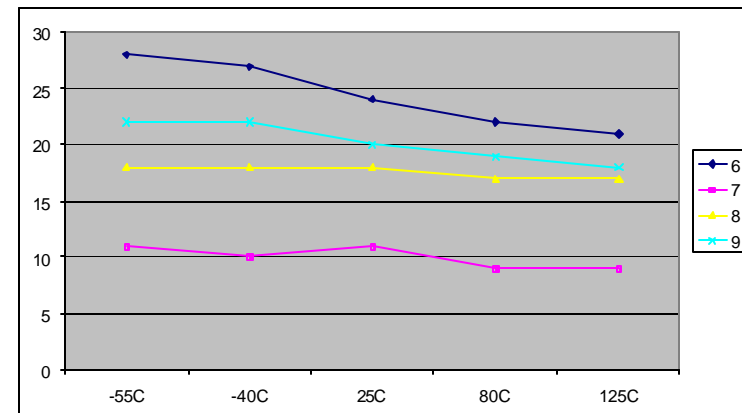
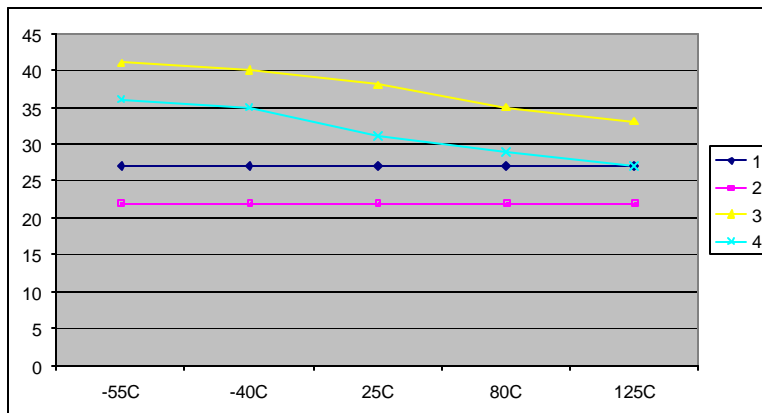
COLD TEMPERATURE TEST RESULTS PROGRAMMABLE COTS OSCILLATORS

Case I-A

Performance

Hermetic Package

			Powered and Measured by the HP E3612A DC Power Supply. All current readings are in mA.				
Voltage	Part No	Programmed Frequency (MHz)	-55C	-40C	25C	80C	125C
5.0	1	32.0000	27	27	27	27	27
5.0	2	66.0000	22	22	22	22	22
5.0	3	99.0000	41	40	38	35	33
5.0	4	133.0000	36	35	31	29	27
3.3	6	25.0000	28	27	24	22	21
3.3	7	50.0000	11	10	11	9	9
3.3	8	75.0000	18	18	18	17	17
3.3	9	100.0000	22	22	20	19	18





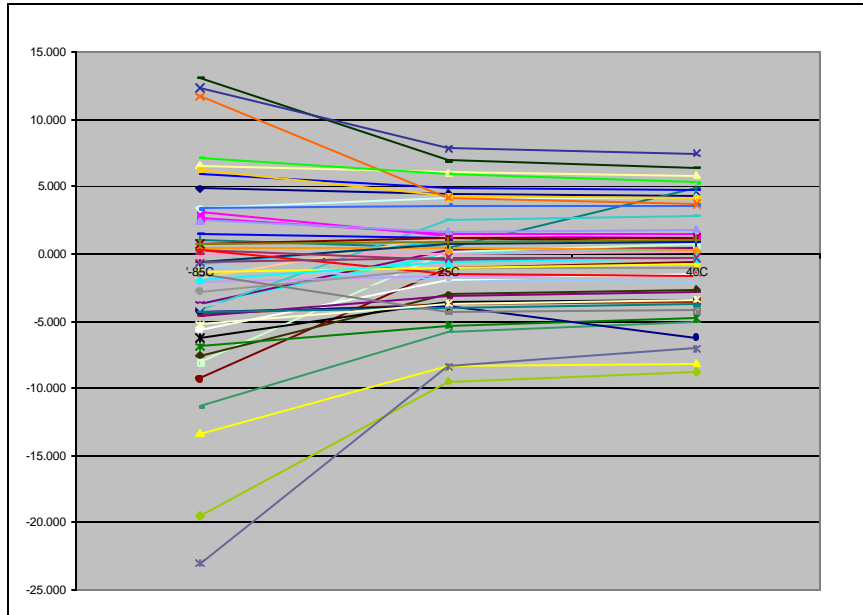
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COLD TEMPERATURE TEST RESULTS - COTS UPSCREEN

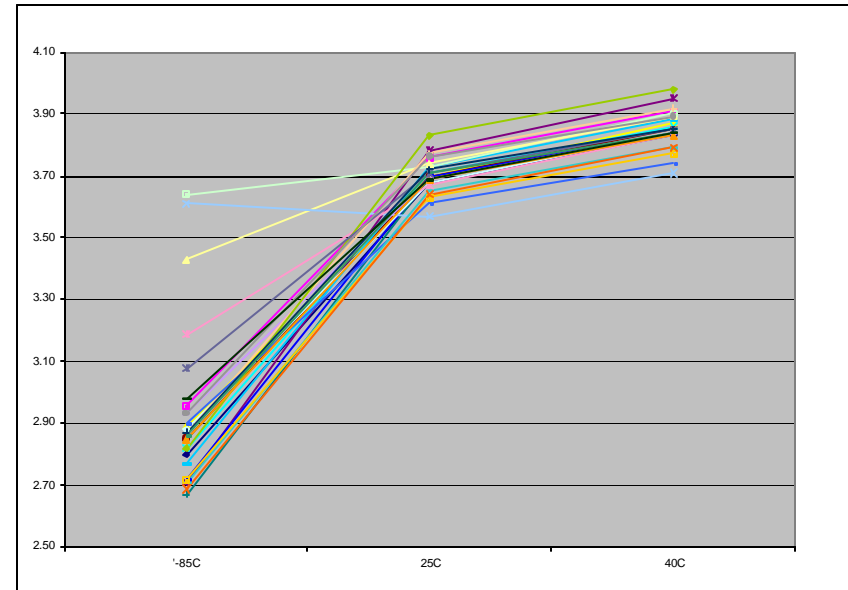
Case I-B

(Examples)

Performance



Part A Ios Range @ -65C



Part A Isc Range @ -65C

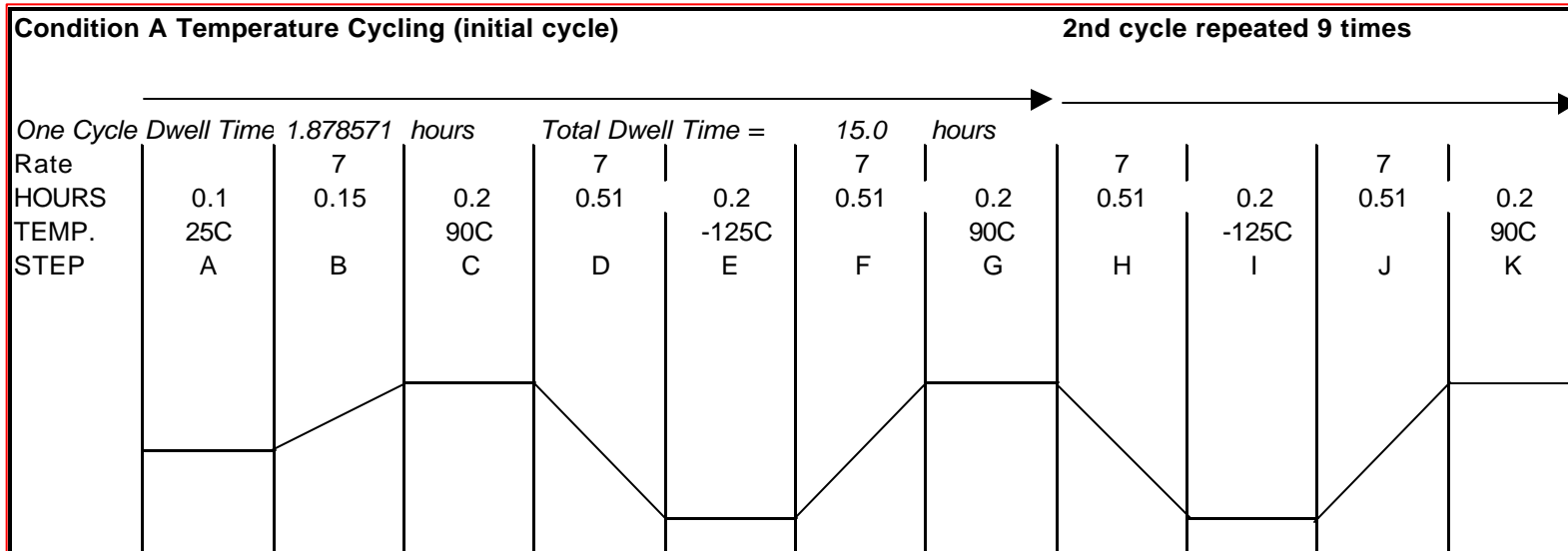
Note: Some devices exhibit more variations and divergence at cold temperatures. Devices >10% from norm are rejected.



TEST RESULTS COTS UPSCREEN

Case II

Temperature
Cycle



Part A Summary: 627 flight parts (PEMs) passed 10 cycles to the above requirement. 20 samples are being qualified to 300 cycles using the same T/C profile.

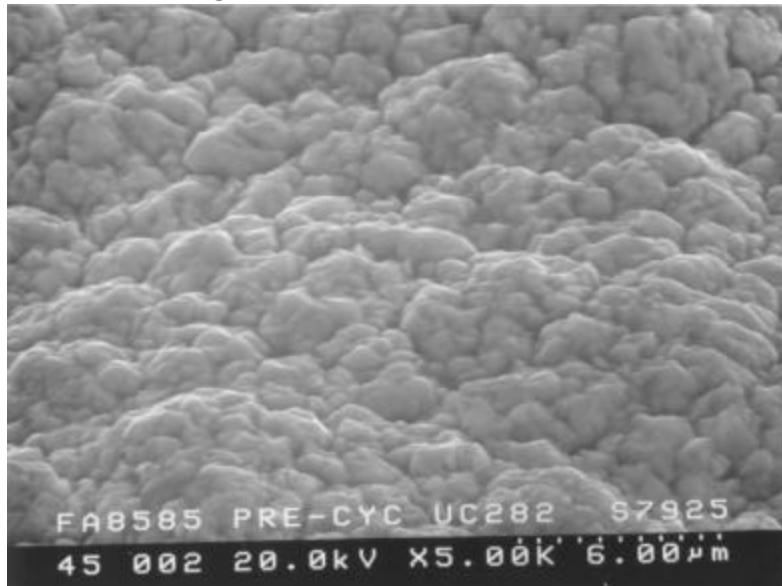


FAILURE ANALYSIS

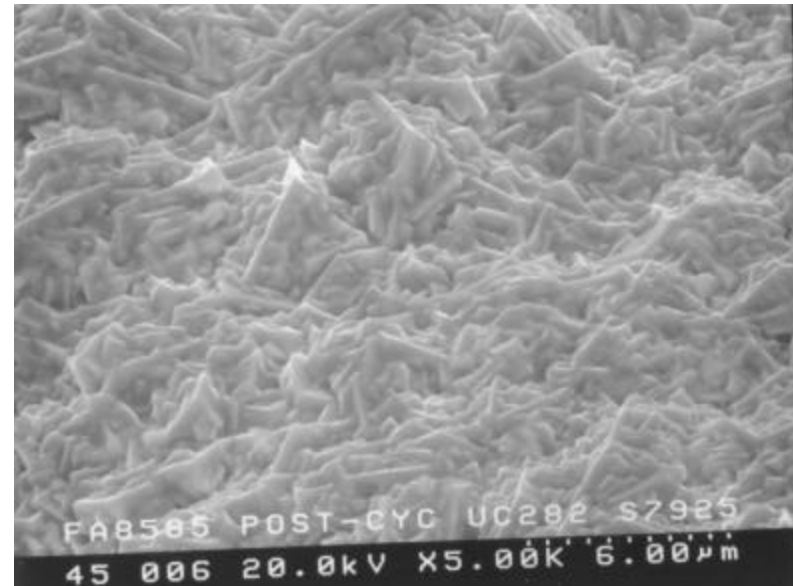
Temperature
Cycle

Case II-A

Oxidation of soldered leads were suspect since the lead surface became dull after T/C and bright after burnishing.



BEFORE



AFTER

5,000X SEM micrograph showing a closeup of the Pb/Sn solder coating on a lead in S/N A. The solder appears to have recrystallized after 10 cycles, resulting a roughening of the surface. Energy dispersive x-ray spectroscopy analysis of the surface revealed only the presence of Pb and Sn. Similar analysis of the pre-temperature cycled device also found only Pb and Sn. There is no apparent solderability problem.



TEST RESULTS for COTS PEMS

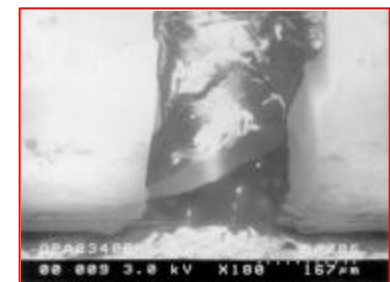
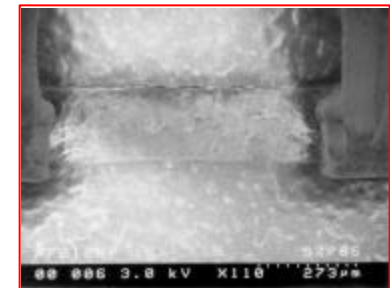
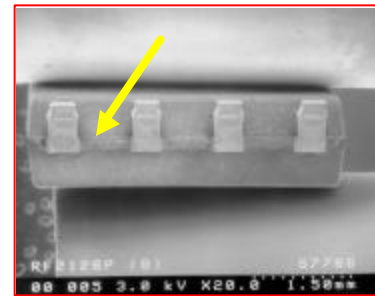
Thermal Shock

Case III

Test Conditions: 30 cycles from
-185° C to +135° C liquid bath

Miniature Cracks Found

Sample 1	PASSED
Sample 2	FAILED →
Sample 3	PASSED
Sample 4	PASSED
Sample 5	PASSED
Sample 6	FAILED →
Sample 7	PASSED





SUMMARY

- Many CMOS commercial devices evaluated beyond their low-end rated temperature ranges have done quite well.**
- Plastic packages have held up under low temperature cycling but show signs of cracking under low temperature shock conditions.**
- Future work is planned to examine long term cold environmental effects such as cold start and operating life degradation.**
- Additional cold temperature test equipment is under development and evaluation.**
- Various part types are planned for reliability evaluation near LN₂ conditions under very long test times.**