Anomalous Radiation Effects in Fully-Depleted SOI MOSFETs Fabricated on SIMOX

Ying Li, Guofu Niu, John D. Cressler, Jagdish Patel, Cheryl J. Marshall, Paul W. Marshall, Hak S. Kim, Robert A. Reed, and Michael J. Palmer

***Abstract*—We investigate the proton tolerance of fully-depleted SOI MOSFETs with H-gate and regular-gate structural configurations. For the front-gate characteristics, the H-gate does not show the edge leakage observed in the regular-gate transistor. An anomalous kink in the back-gate linear I_D-V_{GS} characteristics of the fully-depleted SOI nFETs has been observed at high radiation doses. This kink is attributed to charged traps generated in the bandgap at the buried oxide/silicon film interface during irradiation. Extensive 2-D simulations with MEDICI were used to understand the physical origin of this kink. We also report unusual self-annealing effects in the devices when they are cooled to liquid nitrogen temperature.**

I. Introduction

Silicon-On–Insulator (SOI) technology has recently generated great interest for future system-on-a-chip applications because of its many advantages over bulk technologies, including: total device isolation, speed, and density [1]. Compared to partially-depleted SOI [2], fully-depleted SOI can also reduce short-channel effects and subthreshold swing [3], and suppress the kink in the static I-V curves [4]. Furthermore, by limiting the charge collection volume with the buried oxide layer of the SOI system, SOI technologies are tolerant to radiation-induced latch-up and single event upset phenomena, making them appealing for space applications [5].

However, unless radiation-hardened, the thick buried oxide in SOI technologies introduces a total dose liability since most of the radiation-induced defects are accumulated in the buried oxide. Therefore, total dose effects on fully-depleted SOI MOSFETs using x-ray radiation sources have been of much interest and reported in recent years [6]-[7]. However, the proton tolerance of fully-depleted SOI devices hasn't been reported to date. The purpose of this paper is to evaluate the total dose hardness of fully-depleted SOI MOSFETs on SIMOX with different gate lengths and different gate structures under proton exposure. In this paper, we investigate edge leakage current and kink effects in fully-depleted SOI MOSFETs using proton irradiation. An anomalous kink is observed in the strong inversion region of the back-gate linear I_D-V_{GS} characteristics at the high equivalent gamma doses of 300krad(Si) and 500krad(Si). Analysis of the data reveals the presence of energetically localized traps at the buried oxide/silicon interface. We performed extensive 2-D numerical simulations using MEDICI [8] to understand the physical origins of this unusual kink.

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II. Device Structure

The devices used in this work are from a 0.25µm fully-depleted SOI CMOS technology. The SOI substrate was formed by SIMOX. Two kinds of device structural layouts were used, as shown in Fig. 1: the "H-gate" and "regular" gate [2]. These two structural configurations can be used to isolate and hence study edge effects. The regular gate transistor has MESA edges between the source and the drain. Compared with the regular-gate devices, the H-gate devices do not have a lateral channel along the silicon island/isolation edge, and in addition, also have a body contact.

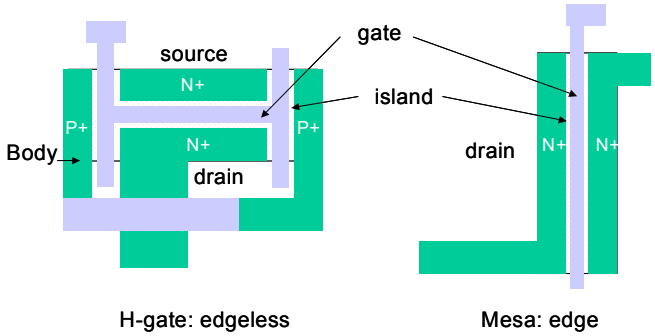

Fig. 1. The top-down views of the H-gate and regular-gate SOI MOSFETs configurations.

An SEM cross-section of the regular-gate device is shown in Fig. 2. The source and drain of the SOI nFET are implanted by the arsenic implantation of $3x10^{14}$ cm^{-2} at 25keV, while the boron implantation of $2x10^{14}$ cm^{-2} at 6keV is used for the source and drain of the SOI pFET, both followed by activation at 1000°C for 30s in an oxygen (25%) and nitrogen environment. The source and drain junctions

extend through the silicon film. In this technology, the front gate oxide thickness is 7.5nm, the silicon film thickness is 50nm, and the buried oxide thickness is 190nm. The silicon film doping is $3.1x10^{17}cm^{-3}$ for the n-MOSFET's. The n+ and p+ polysilicon gates are used for nFET and pFET, respectively. Both H-gate and regular-gate devices were fabricated on the same wafer to facilitate unambiguous comparisons.

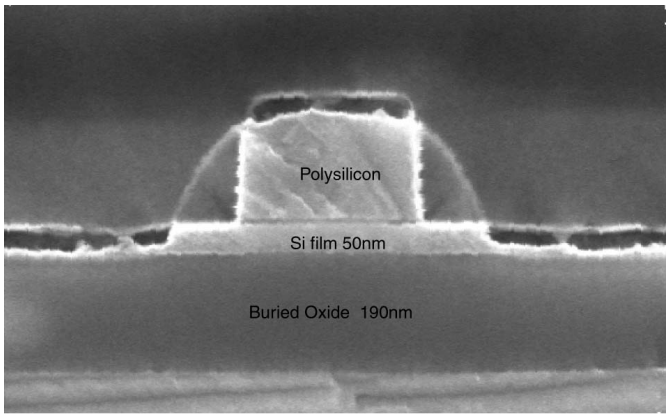

Fig. 2. SEM cross-section of a regular-gate SOI nFET.

III. Experimental Results and Discussion

A. Radiation Experiment

Samples were mounted in 28 pin DIP packages, wire-bonded, and then exposed to 62.5MeV protons at the Crocker Nuclear Laboratory cyclotron located at the University of California at Davis. The dosimetry measurements used a 5-foil secondary emission monitor calibrated against a Faraday cup. Ta scattering foils located several meters upstream of the target establish a beam spatial uniformity of 15% over a 2 cm radius circular area. Beam currents from about 5 pA to 50 nA allow testing with proton fluxes from 10^6 to 10^{11} protons/cm^2 /sec. The dosimetry system has been previously described [9]-[10] and is accurate to about 10%. At a proton fluence of $1x10^{12}$ p/cm^2, the measured equivalent gamma dose was approximately 136 krad(Si).

An array of regular-gate nFETs and pFETs with channel lengths ranging from 0.25 to 8.0μm were irradiated at the room temperature. H-gate nFETs and pFETs with 0.5μm channel lengths were irradiated at the same time to allow comparisons. The device width was 8.0μm for all devices. During irradiation, the front-gate was biased at 2.0V, and all of the other terminals were grounded. The front-gate bias was removed after irradiation and before testing. These devices were measured by using an HP 4155 parametric analyzer before radiation testing and after equivalent total gamma doses ranging from of 10krad(Si) to 500krad(Si) at room temperature.

B. Front-gate Characteristics

Fig. 3 shows I_D as a function of the front-gate V_{GS} for a regular-gate nFET at different radiation doses. With increasing dose, the leakage current increases dramatically, leading to non-ideal subthreshold behavior in the I_D-V_{GS} curve. This leakage current is attributed to the current of the lateral parasitic transistor located at the mesa edge [6]. The H-gate nFET is edgeless and thus does not show this edge leakage, as can be seen in Fig. 4. A shift in threshold voltage is observed in both the regular-gate and H-gate devices.

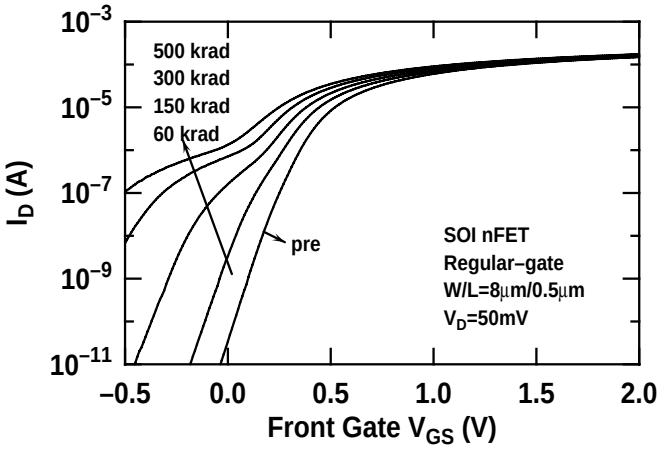

Fig. 3. Front-gate subthreshold characteristics versus dose for a regular-gate SOI nFET.

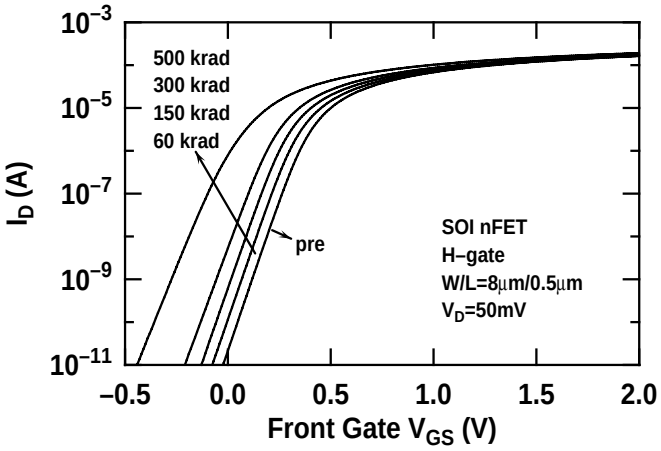

Fig. 4. Front-gate subthreshold characteristics versus dose for an H-gate SOI nFET.

Though the observed threshold voltage shift for the H-gate nFET is high after 500krad irradiation, a thinner front gate oxide will naturally reduce the front gate oxide charge trapping and hence the threshold voltage shift can be readily controlled. Alternatively, one can use a higher nominal threshold voltage to bring the leakage current under control for 500krad irradiation. Therefore, the H-gate structure used for the nFETs holds good potential for total dose hardened applications since there are no edge leakage problems in the H-gate devices.

Fig. 5 shows I_D as a function of the front-gate V_{GS} for a regular-gate pFET. A subthreshold kink was observed, and the kink remains after irradiation. Such a kink, however, was not observed in the H-gate pFETs, as expected, and thus can be attributed to an edge conduction mechanism.

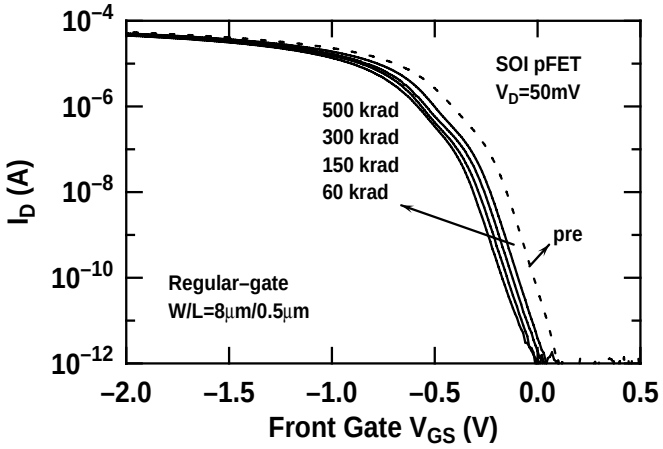

Fig. 5. Front-gate subthreshold characteristics versus dose for a regular–gate SOI pFET.

The pre-radiation front-gate threshold voltage (V_{th1}) and back-gate threshold voltage (V_{th2}) for regular-gate (R) and H-gate (H) nFETs with different channel lengths are shown in Table I.

Table I. The threshold voltage of SOI nFETs

Size (μm/μm)	R 8/0.25	R 8/0.30	R 8/0.50	R 8/8	H 8/0.5
V_{th1} (V)	0.40	0.44	0.45	0.46	0.44
V_{th2} (V)	6.73	7.08	6.77	6.95	6.60

Fig. 6 shows the front-gate threshold voltage shift versus dose for both regular-gate and H-gate devices with various channel lengths. This threshold shift is due to the coupling between front and back gates, since the silicon film is fully depleted. Charge trapped in the thick buried oxide induces a shift of the front-gate threshold voltage through this coupling effect [7]. The threshold voltage shift induced by the trapped charge is smaller at shorter channel lengths. In short channel devices, the surface potential is modulated by not only the vertical electric field, but also the lateral electric field from the source and drain [11]. The lateral electric field penetration is primarily determined by the channel length and source/drain to channel junction built-in potential, and thus does not change much as charges buildup in the buried oxide and front gate oxide. As a result, the threshold voltage shift is less in shorter channel devices, because the vertical electric field plays a less important role. A more complete analysis that takes into account the coupling between vertical and lateral electric field was conducted using a unified surface potential model for short-channel SOI MOSFET's [12], and leads to the same conclusion. In the low dose range, the threshold voltage shift in an H-gate device is smaller than the shift in its regular-gate counterpart.

The back-gate threshold voltage shift versus dose for the same devices in Fig. 6 is shown in Fig. 7 for comparison. For the regular-gate nFET, the back-gate threshold voltage shift is the same for different front channel lengths. For the H-gate device, the back-gate threshold voltage shift is still smaller than the shift in its regular-gate counterpart.

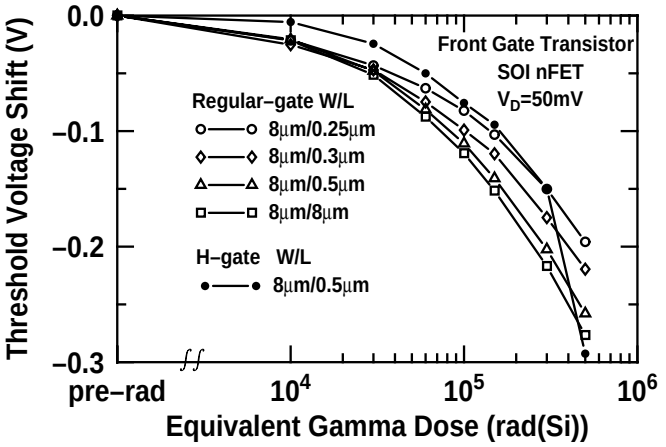

Fig. 6. Front-gate threshold voltage shift versus dose for regular-gate SOI nFETs with different sizes and an H-gate SOI nFET comparison.

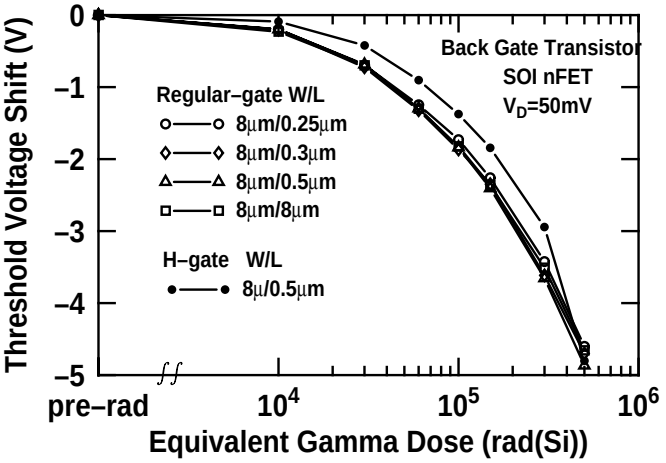

Fig. 7. Back-gate threshold voltage shift versus dose for regular-gate SOI nFET with different sizes and an H-gate SOI nFET.

C. Back Gate Transistor

Fig. 8 shows the back-gate I_D-V_{GS} characteristics of a regular-gate nFET transistor measured at V_D=50mV. An anomalous kink is observed in the strong inversion region of the linear I_D-V_{GS} characteristics at 300krad and 500krad, as shown on the right y-axis. This kink on the linear I_D-V_{GS} curve is clearly distinct from the edge conduction induced subthreshold kink on the logarithmic I_D-V_{GS} curve, because the edge transistor current is negligible compared to the main transistor current at the V_{GS} where the kink occurs. The same strong inversion kink was observed in the back-gate linear I_D-V_{GS} characteristics of the H-gate device, as shown in Figure 9, thus confirming our speculation that the origin of this kink observed in the regular-gate device is not at the isolation edge. A similar back-gate strong inversion kink had been observed in both n- and p-channel FETs fabricated on high dose SIMOX substrate [13], and was attributed to charged traps located in the bandgap at the silicon/buried oxide interface.

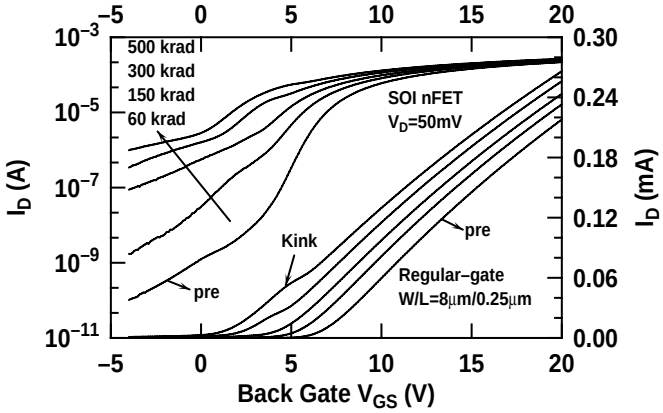

Fig. 8. Back-gate subthreshold and linear characteristics versus dose for a regular-gate SOI nFET.

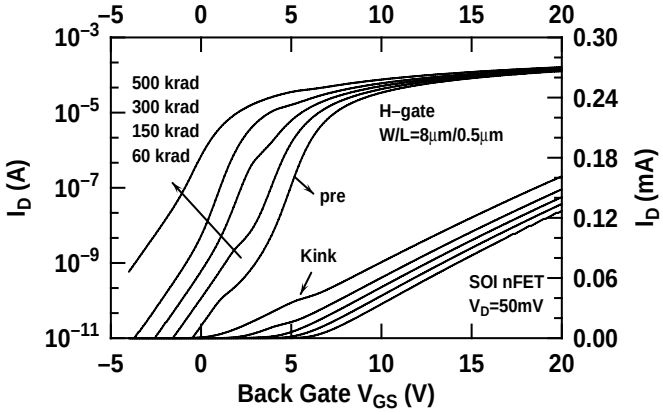

Fig. 9. Back-gate subthreshold and linear characteristics versus dose for an H-gate SOI nFET.

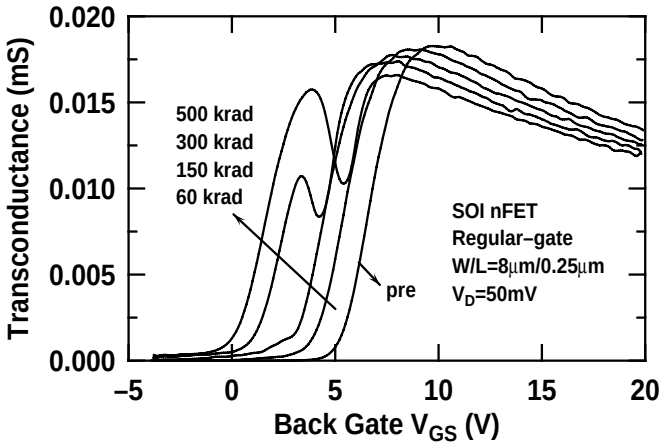

Fig. 10. Back-gate transconductance characteristics versus dose for a regular-gate SOI nFET.

The strong inversion kink in the back-gate linear I_D-V_{GS} curve translates into a temporary decrease of transconductance (g_m) with increasing V_{GS}. As a result, two peaks are observed in the back-gate g_m-V_{GS} characteristics at 300krad and 500krad, as shown in Fig. 10 for the regular-gate device. The H-gate device shows a similar g_m-V_{GS} characteristic, as shown in Fig. 11. No double peak was observed in the front-gate g_m-V_{GS} characteristics (Fig. 12), indicating that the physical origin of the double g_m peak lies at the buried oxide/silicon film interface.

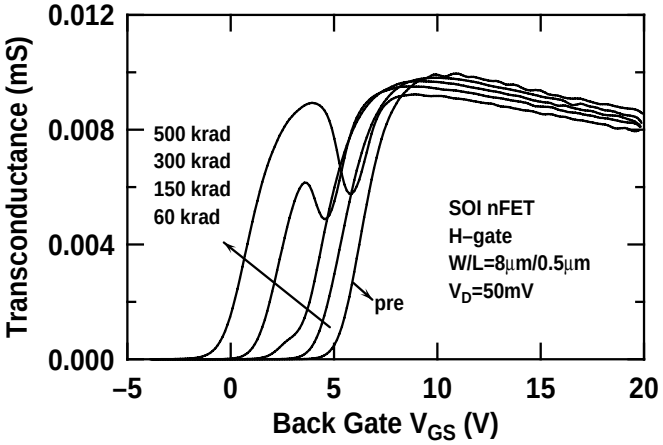

Fig. 11. Back-gate transconductance characteristics versus dose for an H-gate SOI nFET.

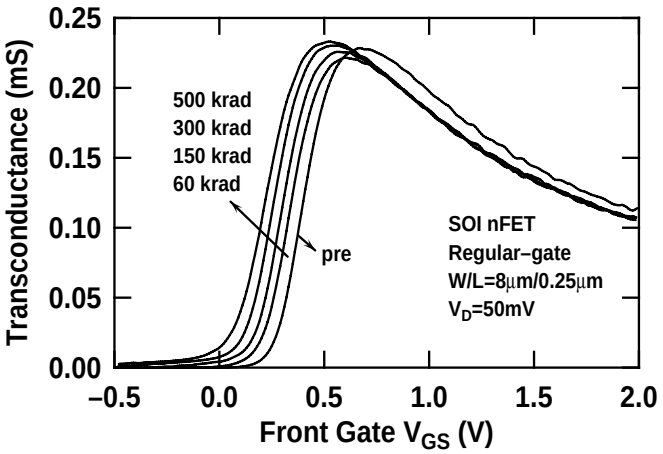

Fig. 12. Front-gate transconductance characteristics versus dose for a regular-gate SOI nFET.

The kink in the back gate linear I_D-V_{GS} curve can also be described as an increase of threshold voltage from low back gate voltage to high back gate voltage, as can be seen in Fig. 13. This typically occurs when the interface traps exist in the forbidden gap. The type and density of such traps can be inferred from the I_D-V_{GS} behavior. The observed increase of threshold voltage is only possible for a donor type electron trap located near the conduction band edge E_C, since number of positive charges associated the traps decreases as gate voltage increases (equivalent to an increase of threshold voltage). The fact that this kink occurs after the device enters into strong inversion operation indicates that the trap must be located fairly close to the conduction band edge E_c. In order to produce a clearly visible kink, the energy distribution must be a delta function in the bandgap, and is very likely a single energy level. The density of traps must be high enough to produce a large enough threshold voltage shift (or the kink).

As the back gate bias increases, the quasi Fermi-level of electrons, E_{fn}, shifts towards the conduction band edge E_C. Strong inversion occurs when E_{fn} is close to E_C, thus increasing the effective back gate to channel capacitance that is responsible for the initial g_m increase. At these lower back gate voltages, the traps are empty and positively charged because the trap energy level is well above E_{fn}. These positive

interface charges effectively reduce the back channel threshold voltage. With further increase of back gate voltage, E_{fn} further moves toward E_c, crosses the trap level E_t at certain back gate voltage, and eventually rises well above the trap energy level E_t. All of the interface charge traps are then occupied by electrons, thus reducing the interface charge density, increasing the threshold voltage, and producing a kink in the linear I_D-V_{GS} (Fig. 13).

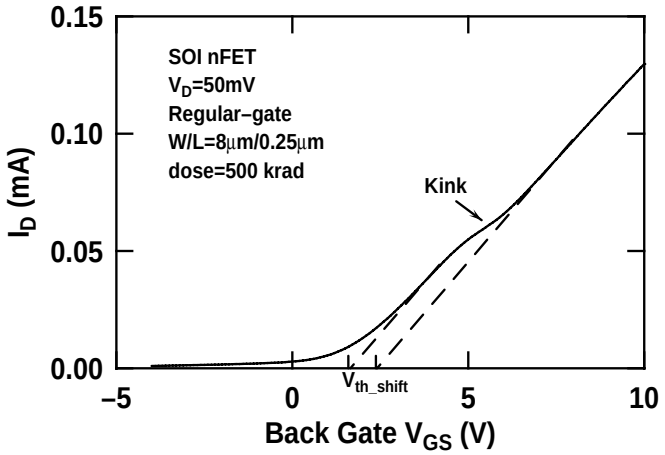

Fig. 13. Back-gate threshold voltage shift for a regular-gate nFET after 500krad irradiation.

To confirm our theoretical analysis, extensive 2-D device simulations were performed using MEDICI [8] for 200 combinations of trap energy level and trap density (10 values of trap densities times 20 values of energy level). In each case, details of the I-V, C-V, and band diagrams were examined as a function of gate voltage against our theoretical expectations. The results indeed confirm that a linear I_D-V_{GS} kink can be obtained only when the trap energy is close to E_c and the trap density is high.

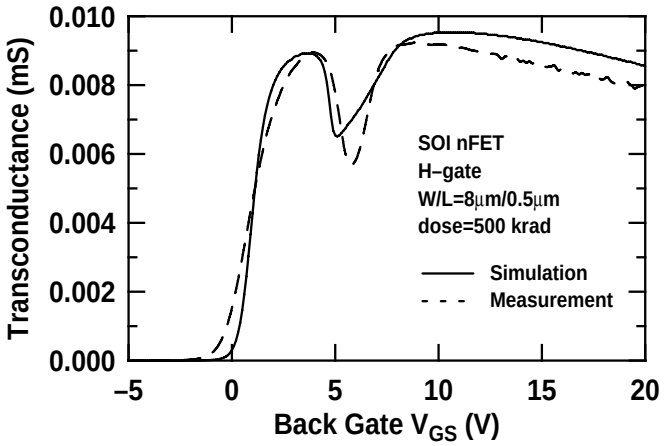

Fig. 14. Comparison of simulated and measured back-gate transconductance versus back-gate voltage.

The details of the double g_m peak, such as the V_{GS} spacing of the two peaks, are a strong function of the energy level in the bandgap and the trap density. It takes a unique combination of trap energy level and trap density to closely reproduce the back-gate I_D-V_{GS} kink or double peak g_m-V_{GS} characteristics. Fig. 14 shows the comparison of simulated and measured back-gate gm-VGS curves for an H-gate nFET transistor at 500krad. The simulated curve is in agreement with that of the measured result.

The trap energy level was determined to be 0.49eV above the intrinsic Fermi-level, and the density (N_{it}) was determined to be $8x10^{11}cm^{-2}$:

$$E_t = 0.49eV + E_i$$

The electron charge density (Q_n) at the Si/buried oxide interface was extracted from the simulation results using an in-house C program to better illustrate the impact of the positively charge electron traps. Fig. 15 shows Q_n (an indicator of I_D) and dQ_n/dV_{BG} (an indicator of g_m) as a function of the back-gate voltage. A kink occurs in the Q_n-V_{BG} curve as the quasi Fermi-level of electrons crosses the trap level, as a result of the trapping of electrons and the associated threshold voltage increase. Correspondingly, a decrease is observed in the dQ_n/dV_{BG} curve. The decrease of dQ_n/dV_{BG} can also be understood as a result of the capacitance associated with the trapping of electrons at the trap energy level. This capacitance has a value of zero when the quasi Fermi-level of electrons is several kT away (either below or above) from the trap level, and is thus not important at all for the gate to channel capacitance at either low or high back gate voltages. The capacitance value peaks when the quasi Fermi-level of electrons crosses the trap level near the g_m valley, resulting in a decrease of dQ_n/dV_{BG} (the gate to channel capacitance) results for certain values of trap energy level. The amount of the increase depends also on the trap density. At higher gate bias, the trap capacitance is zero, and g_m increases again. Eventually g_m decreases, because of mobility degradation at high gate voltage.

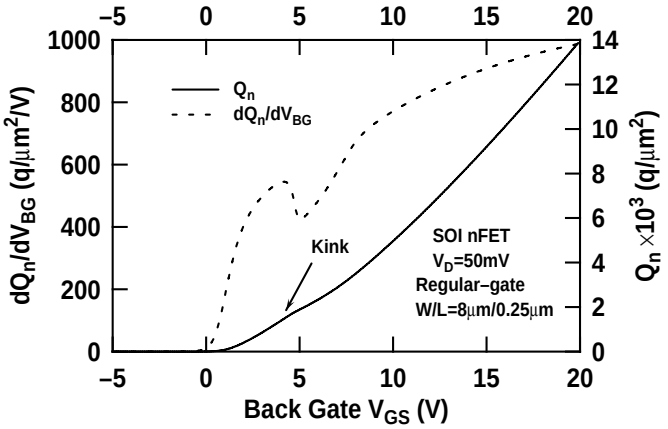

Fig. 15. The electron charge density at the Si/buried oxide interface versus the back-gate voltage, and the differential of the electron charge density with respect to back-gate voltage versus the back-gate voltage.

The theory of Sakurai and Sugnao [14] supports the result obtained in the present work. In [14], they used semi-empirical tight-binding Hamiltonians and Green's functions to calculate the energy levels of defects at Si/SiO_2 interface. The Si-O weak bond or the peculiar bonding parameter at the back interface causes a donor-type electron trap localized in energy

space above the intrinsic Fermi-level. Radiation apparently is further weakening this Si-O bond at the back interface, thus producing the observed double g_m peak.

The strong inversion kink, however, was not observed in the back-gate linear I_D-V_{GS} characteristics of any of the p-channel FETs. A typical back-gate g_m-V_{GS} characteristic is shown in Fig. 16. This is different from the results obtained in [13], where the strong inversion kink was observed in both nFETs and pFETs on high-dose SIMOX wafers. The high-dose SIMOX wafers already have the donor-like electron traps and donor-like hole traps because the SIMOX fabrication process leaves behind the loosely combined Si-O and Si-Si bond states, resulting in these electrically active defects at Si/buried oxide interface. The traps at Si/buried oxide for our SOI devices are introduced by the irradiation. Built-in field and space charge effects determine trapping as dose increases [15]. Therefore, these radiation-induced traps are fundamentally different from those induced by the SIMOX fabrication process. We speculate that the irradiation (up to 500krad) further weakens the Si-O bond and is not capable of weakening the Si-Si bond.

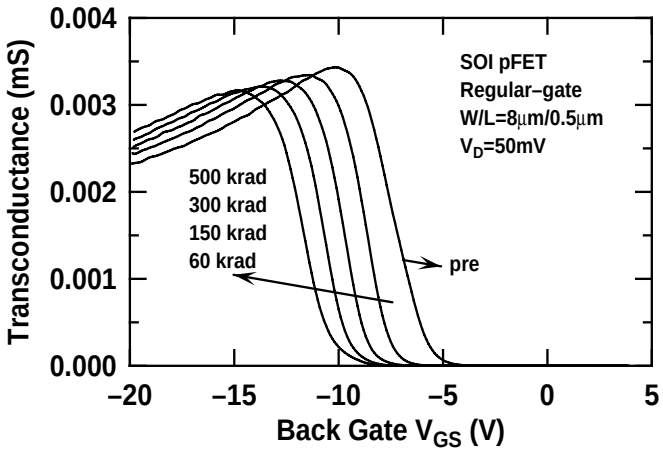

Fig. 16. Back-gate transconductance characteristics versus dose for a regular-gate SOI pFET.

D. Low Temperature Annealing

Interestingly, an unusual low temperature annealing of radiation-induced traps has been found in these post-radiation fully-depleted SOI MOSFETs. Fig. 17 shows the front-gate I_D-V_{GS} characteristics of a regular gate nFET in which this annealing was observed. Before measurement at 77K, the post-irradiated devices remained at room temperature for several months. A conventional spontaneous self-annealing of the edge leakage can be observed. Subsequently, the devices were dipped into liquid nitrogen (77K) directly from the room temperature. The devices were measured by using an HP 4155 parametric analyzer when the devices temperature was 77K. Then the devices were lifted up from liquid nitrogen and warmed back to 300K. The devices were measured again at 300K. This process of dipping into liquid nitrogen, measuring, warming the sample back to 300K, re-measuring, and then dipping again and measuring once more, was repeated several times. As can be seen in Fig. 17, an unusual annealing effect resulted from this process, yielding an almost complete recovery of the pre-irradiated I_D-V_{GS} curve (the post-radiation threshold voltage actually increased to values larger than the pre-rad threshold voltage). This result was repeatable on all devices, and is particularly surprising given that trap population and de-population under annealing should be thermally activated, and hence decrease strongly with cooling. The observed phenomenon can be referred to as a device "rebound" effect [16]. We are currently exploring the physics underlying this annealing effect at low temperature.

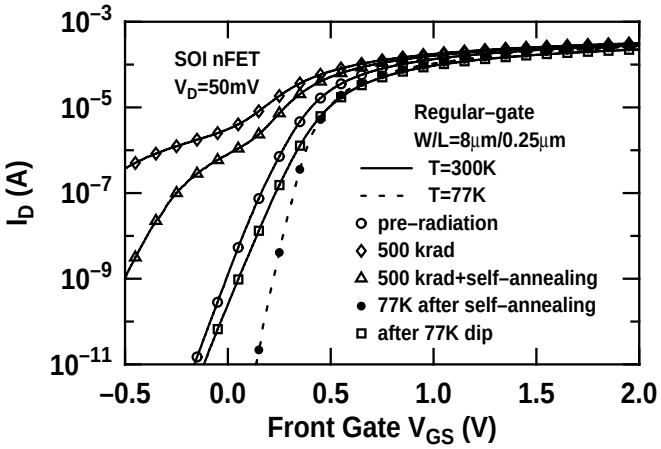

Fig. 17. Front-gate subthreshold characteristics versus dose and temperature for a regular-gate SOI nFET.

IV. SUMMARY

We have presented proton radiation data on 0.25μm fully-depleted SOI MOSFETs fabricated on SIMOX wafers. For the front-gate characteristics, the H-gate transistor is edgeless and hence does not show the edge leakage observed in the regular-gate transistor. Because of the charge trapped in the thick buried oxide, the threshold voltage shift through the coupling effect can be observed. In the low dose range, the threshold voltage shift in an H-gate device is smaller than the shift in its regular-gate counterpart. Moreover, an unusual kink phenomenon has been experimentally observed in the back-gate linear I_D-V_{GS} characteristics at 300krad and 500krad, and 2-D numerical simulations using MEDICI have been performed to understand the mechanism. This kink in the nFETs can be attributed to the presence of energetically-localized donor-like electron trap states at the buried oxide/silicon film interface. The density and the energy level of interface states are related to the dose. Finally, an unusual low temperature "rebound" annealing effect has been found in the post-radiation MOSFETs.

V. ACKNOWLEDGMENTS

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