Charge Collection Analysis and SEU Modeling of SiGe HBTs for High-Speed Digital Logic

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Outline

• Motivation
• SiGe HBT Technology
• Total Dose and SEU Data
• Quasi-3D Charge Collection Analysis
• Circuit-level Modeling of SEU
• Preliminary Full-3D Simulations
• Summary
The Holy Grail of the Space Community:
- IC technology space-qualified without additional hardening

SiGe HBT BiCMOS Technology:
- bandgap engineering in Si (high yield + low cost)
- III-V device performance (> 70 GHz $f_{\text{max}}$)
- system-on-a-chip integration (SiGe HBT + Si CMOS)

Radiation Tolerance:
- robust to total dose and displacement (gamma, neutron, proton)
- But … sensitive to SEU

Question:
Can We Use TCAD to Understand the SEU Charge Collection and Aid in Circuit-level SEU Mitigation?
IBM’s First-Generation SiGe HBT BiCMOS Technology (5HP)
- UHV/CVD epitaxial SiGe base
- deep and shallow trench isolation
- 5 layers of metal

No intentional radiation hardening

SiGe HBT Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drawn Emitter Width (μm)</td>
<td>0.50</td>
</tr>
<tr>
<td>Actual Emitter Width (μm)</td>
<td>0.42</td>
</tr>
<tr>
<td>peak ?</td>
<td>115</td>
</tr>
<tr>
<td>$V_A$ (V)</td>
<td>60</td>
</tr>
<tr>
<td>peak $f_T$ (GHz)</td>
<td>50</td>
</tr>
<tr>
<td>peak $f_{max}$ (GHz)</td>
<td>70</td>
</tr>
<tr>
<td>$BV_{CEO}$ (V)</td>
<td>3.3</td>
</tr>
</tbody>
</table>

Device Cross-section
SiGe HBT Proton Tolerance

- Robust to Very High Proton Fluence (multi-Mrad!)
  - minimal dc and ac degradation at circuit operating bias conditions
Preliminary SEU Data

- Low LET Threshold
- Conventional III-V Hardening (CSH) Doesn’t Work!

Quasi-3D Modeling

- Avant! MEDICI (2D – solve in cylindrical coordinates)
- Use SIMS + device layout
- Various bias conditions on E, B, C, Substrate
- R, C on collector to mimic ECL gate loading
- Top substrate contact, deep substrate to capture physics
- Input time-dependent charge into SPICE to model SEU

\[
i_{cn} = -(i_{bp} + i_{sp} + i_{en})
\]
Loading Effects

• R and C load conditions matter!
• Decrease in charge collection gives worse SEU!
Substrate Effects

- Decreasing substrate doping helps!
- Decreasing substrate bias helps!
- Decreasing substrate thickness helps!

![](chart1.png)

**Graph 1:**
- $V_B=0V, V_E=0V$
- $V_{SUB}=-5.2V$
- $R=1.2k\Omega, C=15fF$
- Lines represent different substrate doping levels:
  - $5 \times 10^{15}/cm^3$
  - $1 \times 10^{17}/cm^3$
  - $1 \times 10^{19}/cm^3$

**Graph 2:**
- $V_{SUB}=-5.2V$
- $V_B=0V, V_E=0V$
- $R=10k\Omega, C=2fF$
Circuit-level SEU

- Use ECL D-Flip flop as high-speed logic metric
- Compare various architectures for same charge profile

Circuit A: Standard ECL

Circuit B: Unhardened CSH

Circuit C: Hardened CSH
Circuit-level Results

- Standard ECL architecture is best!
- Output cross-coupling causes the problem.

Circuit A: Standard ECL

Circuit B: Unhardened CSH
• Full 3D Device Simulation
  - better physics
  - off-center strikes
  - tough problem!

• Tool: ISE (DESSIS)
  - SiGe capability
  - SEU capability

• Typical Run:
  - 15,572 nodes
  - 208 min per timestep!
Time Evolution

- Ion Strike: LET = 10 (0.1 pC/µm), 10 µm depth, center of emitter
- E=B=C=0V, Sx = -5V, $R_C = 1.2$ k ohms, $C_C = 15$ fF

Initial Strike

After 6.0 psec
Time Evolution

After 50 psec

After 200 psec
Summary

• SiGe HBT BiCMOS Technology
  - bandgap engineering in Si (high speed + low cost)
  - inherent dose tolerance, but SEU sensitivity exists

• TCAD Can Be Used To Understand SEU in SiGe HBTs
  - R,C loading and bias effects
  - substrate effects
  - circuit architecture matters! (standard design best – area penalty)
  - adequate SEU immunity appears possible for SiGe HBT logic

To Be Done:
• Full 3D simulations
• 3D versus quasi-3D comparison
• True mixed-mode SEU simulation (not Q(t) + SPICE)
• Microbeam experiment (data versus model)