In-Flight Observations of Multiple-Bit Upset in DRAMs

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Abstract **-- In interplanetary space, the Cassini Solid-State Recorder is experiencing the predicted number of upsets, but a very high rate of uncorrectable errors. An experimental investigation of the flight DRAM's susceptibility to multiple-bit upset (MBU) proved enlightening, revealing an unexpectedly high rate of MBUs (even caused by protons). In combination with an architectural flaw in the error correction circuitry, these explain the flight anomaly.**

I. INTRODUCTION

The Cassini spacecraft, launched in October 1997 to investigate Saturn and its moon Titan, carries two solid-state recorders (SSRs). They contain 2.5 gigabits of memory (2.1 Gb usable for data) and replace magnetic tape recorders for the storage of science data while awaiting relay to earth. TRW designed and built the two identical flight recorders using state-of-the-art (early '90s) 4-Mb OKI DRAMs, organized as 1m addresses by 4 bits. The individual recorders are about bread-box size and contain 640 DRAMs and 18 ASICs on six boards like that shown in Fig. 1.

In 1991 when JPL first seriously considered replacing tape recorders and requested proposals to build the specified SSRs, the expectation was that the large capacity and limited power requirements would drive the proposers to upset-soft commercial devices in combination with error detection and correction (EDAC) circuitry. Unexpectedly, TRW proposed using DRAMs instead of static devices (SRAMs). While DRAMs were (and still are) a factor of four denser than SRAMs and may have a power consumption advantage as well, single event latchup (SEL) was thought to be a universal problem. However, TRW was able to produce data, which JPL subsequently confirmed, showing that some manufacturers' devices had both acceptable total dose (greater than 50 krad(Si)) and latchup immunity to an LET (linear energy transfer) greater than 120 MeV per mg/cm^2; thus, the SSRs are built on the concept of "fortuitously rad hard," which works for commercial DRAMs, in part, because there are so many manufacturers. Note that "commercial DRAMs" is somewhat redundant, as there are no military-spec dynamic RAMs.

It is well known that commercial DRAMs are highly sensitive to single-event upset [1, 2] and the OKI devices are no exception [3]. In addition to the EDAC circuitry, extra shielding (equivalent to 0.500" of Al) was placed around the SSR boxes to reduce the number of single event upsets

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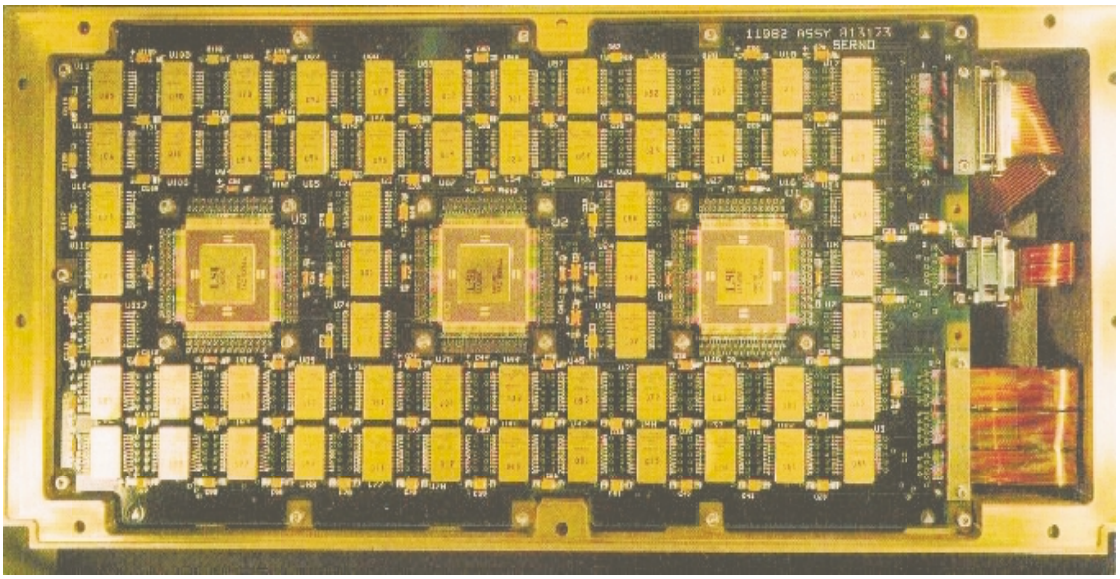

Fig. 1. Photograph of the front side of one memory board from the Cassini SSR design verification unit. The three larger devices are custom ASICs (application specific integrated circuits) which control access, refresh, and error scrub of sub-arrays of 40 DRAMs (20 on each side). The sixty smaller devices are the OKI 4-Mb DRAMs in individual hermetic packages; the dice are the same as in MSM514400 commercial, plastic parts.

(SEUs) from solar particle events. While shielding to reduce SEUs is unusual, it is effective for devices with this low an LET threshold in radiation environments with many low energy particles that the shielding stops. For example, the peak rate from a severe design case flare at 0.6 AU (Cassini at Venus flyby) drops from almost 600,000 upsets/device-day behind 0.060" Al-equivalent to 14,500 for a 0.500" shield or to 5,200 for a full inch.

Extensive radiation tests of the 4-Mb DRAM were done during the design and qualification of this critical subsystem. Those results were used along with the theoretical improvement provided by the EDAC to calculate the error rate expected during flight, but no DRAM irradiations were done with EDAC in place to check the system performance.

This paper discusses the observed error rate from the solid-state recorder, which exhibited a much higher number of uncorrected errors than expected. Further, it presents the results of additional testing to elucidate the role of MBUs in the unexpectedly high error rate.

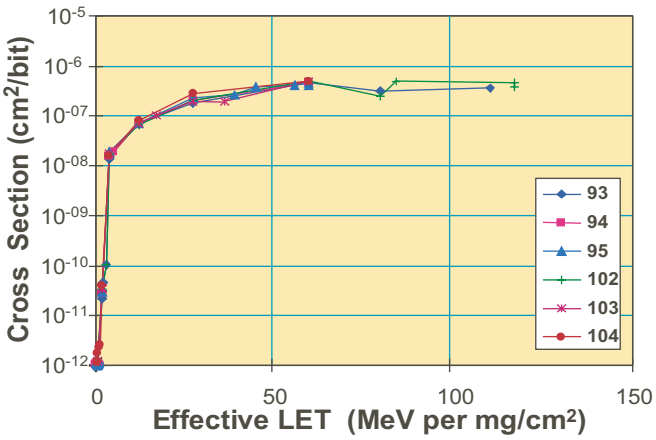

Fig. 2. Heavy-ion upset cross sections for the OKI 4-Mb DRAMs measured during radiation lot acceptance testing (RLAT) showing small part-to-part variation for six devices (serial numbers in the legend). Note that "per bit" is for the entire device, not just the susceptible half. Also note that some data taken with non-zero tilt angles has been removed.

II. DRAM TEST DATA AND ERROR CORRECTION

A. Heavy-Ion Test Data

Samples of 4-Mb OKI DRAMs from the flight lot were tested at Brookhaven National Laboratory. All bits and the overall functional operation of the devices were monitored during these tests. The data pattern consisted of half upsettable bits and half not, in order to simulate expected-flight use.

The "standard" cross section vs. effective LET are shown in Fig. 2, counting each individual error in each cell location; however, some data taken at angles in the threshold region has been removed from the data set because these points are not "well behaved" from the standard point of view. In the modified presentation of Fig. 3, these points are restored. The misfits show that the effective LET (defined as normal-incidence LET over the cosine of the angle of incidence) is not an appropriate model for the response of these DRAMs. A much better fit is obtained if the response is considered to be essentially isotropic. The reason is that the DRAM charge collection is dominated by diffusion over a fairly long time and closely packed charge collection nodes share charge among the nearest to an ionization trail. The isotropic assumption is mathematically similar to assuming an RPP (rectangular parallel piped) charge collection volume with a depth-to-width aspect ratio of one.

The threshold LET -- defined here as the lowest LET at which errors are actually observed -- is very low, below 1 MeV per mg/cm^2 as is typical of DRAM technology. The upset cross section increases rapidly with increasing LET, eventually flattening at an LET of about 15 MeV per mg/cm^2. At high LET, each ion is causing, on average, almost two errors. The cross section continues to increase due to the diffusion-dominated response of the DRAM cell where charge collected for many milliseconds affects the stored charge (the time between refreshes is 40 ms. for the Cassini design).

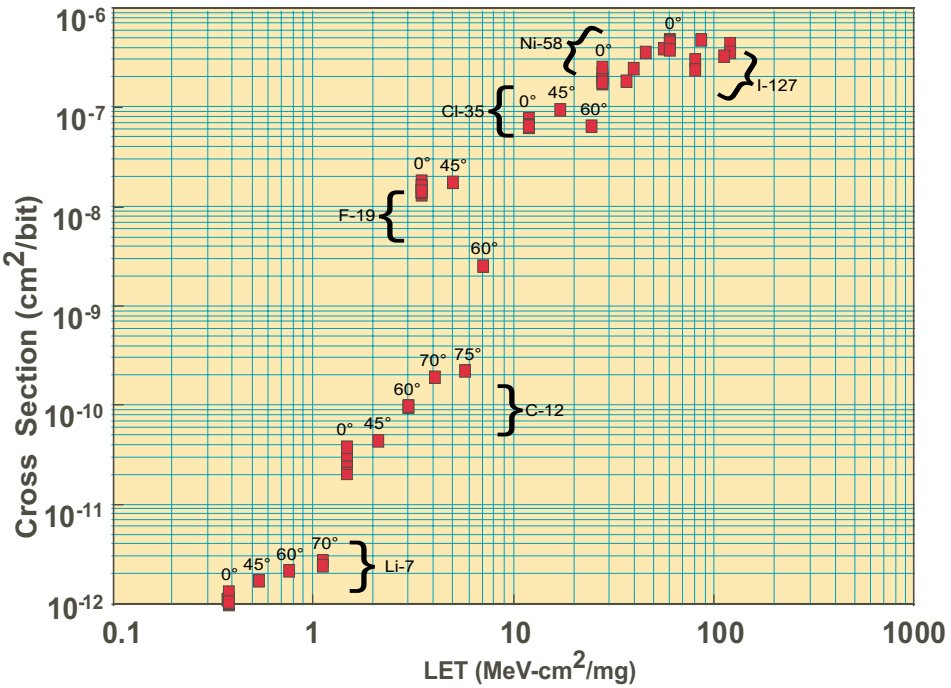

Fig. 3. The complete heavy-ion data set from the RLAT in a slightly modified presentation clearly reveals "cosine law" deviations. All the ions used and most of the angles are noted. Standard errors from counting statistics are less than 10%.

B. Proton Test Data

Because of the low LET threshold, these DRAMs can easily be upset with protons. The proton-induced upset rate can dominate the heavy ion rate during a solar flare, and Cassini's lengthy mission (12 years) practically guarantees that it will experience significant flares. Therefore, proton upset testing was performed at Harvard as part of the radiation lot acceptance testing. These test results are shown in Fig. 4.

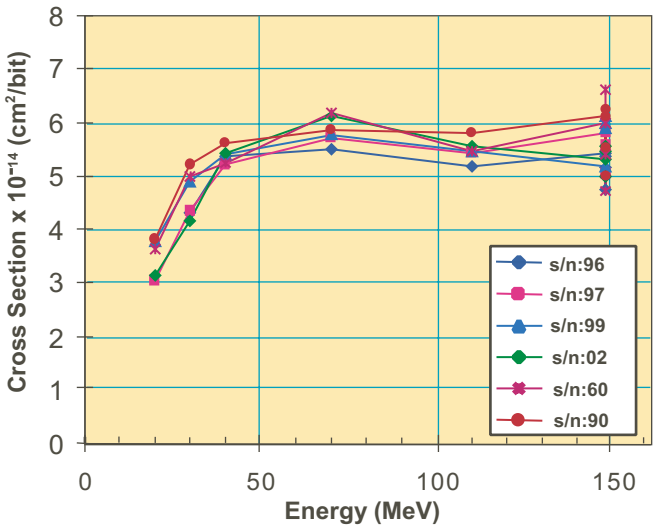

Fig. 4. Proton cross upset sections for the OKI 4-Mb DRAM measured during RLAT showing small part-to-part variation for six devices (serial numbers in the legend). Standard errors from counting statistics are less than 10%.

C. Error Correction Algorithm

The memory subsystem uses words that are 39 bits in length. Thirty-two of these bits store data, and the other 7 are used to store the Hamming code, which provides the ability to detect and correct single-bit errors. Double-bit errors can also be detected with this architecture, but not corrected. Triple-bit and higher errors are either "corrected" erroneously or not detected. A similar EDAC system has been flown with static RAM-based SSRs with zero uncorrectable errors reported [4]. Also, a similar DRAM-based SSR built by SEAKR with similar EDAC has logged several years without excess uncorrectables on Mars Global Surveyor.

Memory subsystems are "scrubbed" of single errors about every nine minutes. A count of the number of single-bit errors that are corrected is maintained. An uncorrectable count is also maintained, but it is difficult to extract useful data from this counter because each uncorrectable error causes the counter to increment every scrub cycle until new data overwrites that area of the SSR. These error counts are transmitted in the engineering telemetry along with other flight data, providing a history of the overall performance of the EDAC system and a record of the radiation environment during flight.

D. Prediction of Space Upset Rates

The proton and heavy ion upset rates were calculated using the JPL standard technique of smoothly integrating the environments and the data set with suitable modification for the isotropic response of the device. This yields an expected upset rate, probably not conservative, certainly not a worst case rate. For solar maximum (which is approaching), the galactic cosmic ray (GCR) background rate is 180 per SSR-day and for solar minimum, the rate is almost a factor of five higher at 890.

To obtain the rate at which errors are presented to the system, that is, the uncorrectable error rate, the Edmonds Approximation to the exact calculation is convenient:

$$\dot{E}_{2-bit} \approx \frac{1}{2} \cdot \frac{T_{scrub}}{N_{EDAC}} \cdot \dot{E}_{1-bit}^{2} \qquad (1)$$

where $\dot{E}_{n-bit}$ is the rate of EDAC word errors with n incorrect bits, T_{scrub} is the time interval to scrub single-bit errors, and N_{EDAC} is the number of EDAC words. For Cassini SSRs, T_{scrub}=8.94 minutes and N_{EDAC}=67,108,864. Thus, the expected rate of double-bit-errors in EDAC words is 0.00055 per year for solar maximum and 0.013 per year for solar minimum.

III. IN-FLIGHT RESULTS

The Cassini spacecraft was launched during a very quiet period in the solar cycle, and little flare activity has been experienced during the first two and a half years of flight. However, shortly after launch a sharp increase in the single-bit error rate was noted in the active solid-state recorder. Fig. 5a shows the single-bit errors that were detected and corrected during successive 24-hour time intervals surrounding the remarkable day. The background level is nearly constant at about 280 errors per day. On November 6, 1997, the number of errors increased by about a factor of four. Fig. 5b shows in finer detail the errors seen by the SSR on that day. Because Cassini was still in the vicinity of earth and the earth-orbiting GOES-9 satellite detected a small solar proton event, the increase in SSR errors can be ascribed to the proton event.

The double-bit error rate observed during the same time period also showed a factor of four increase less than the factor of sixteen expected if the energy spectrum is unchanged. This is consistent with the energy spectrum of the proton event being dominated by low energy protons, which are less effective in causing multiple-bit upsets (MBUs) than protons with higher energy or heavy ions. This dependence is experimentally verified and quantified in Section IV-b.

The observed error rate of ~280 errors per day in late 1997 is near the prediction for solar maximum and the rate has been decreasing towards closer agreement. By the Spring of 2000, the average daily single-bit error rate had dropped by almost a factor of two to 145, as shown in Table I. This is consistent with on-orbit experience of the SOHO (SOlar Heliospheric Observatory) [5].

While this is more than reasonable agreement with the single-bit predictions, surprisingly, the double-bit error rate is far higher than one would expect given the singles rate; with fewer than two single-bit errors - on average - per scrub cycle, the chances that they are coincident in the same 40-bit word out of the over 67 million words is astronomically

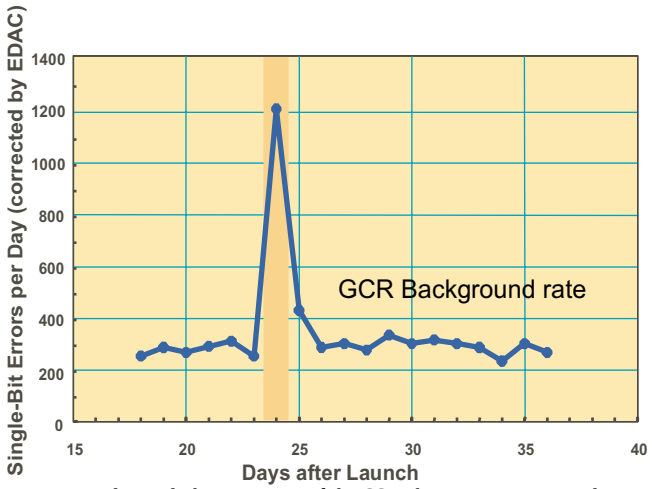

Fig. 5a. Daily single-bit error rate of the SSR showing an increase during a small solar flare.

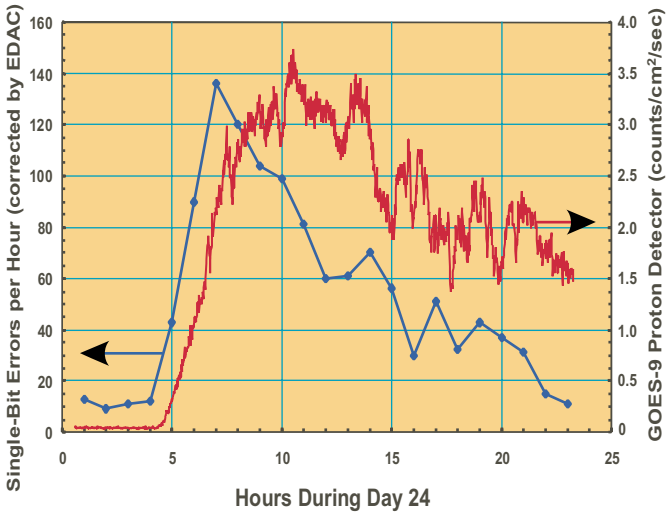

Fig. 5b. Hourly single-bit error rate of the SSR during the day of the small flare. The increase coincides with an increase in protons observed by the GOES-9 satellite, but falls off somewhat faster. For example, the uncorrected counts from the 39 - 82 MeV detector are shown above.

small. Clearly, random coincidence does not explain the rate that uncorrectable errors are being generated. Multiple-bit upsets are expected for this part and have been previously seen in space for 16 Mbit NEC DRAMs [6]. This anomalous performance spurred additional proton and heavy ion testing to investigate the details of single-event multiple-bit upsets in the DRAMs and how the EDAC architecture handles them.

TABLE I
Daily Upsets for Sample Week in 2000

March 21	163
March 22	121
March 23	119
March 24	179
March 25	131
March 26	158
March 27	147*

*=21 hrs. of telemetry, scaled to 24

IV. ANOMALY INVESTIGATION

A. *Recorder Architecture*

The recorder architecture was examined more closely to determine how the EDAC was physically implemented. Data from five different chips were used within the 39-bit EDAC word. Two successive passes were used. The first pass obtained 20 bits of data, four bits from each of the five DRAM chips. The locations of the four bits within each chip were widely separated. During the second pass to obtain the last 19 bits, the address for the bank of five DRAMs was incremented by one. Consequently the data from each bit in the first pass was physically very close to the data from the equivalent bit in the second pass. Fig. 6 shows a physical diagram of this process.

Although it is likely that successive addresses in DRAMs are located close together, that is not necessarily the case. Aided by the results of destructive physical analysis (DPA),

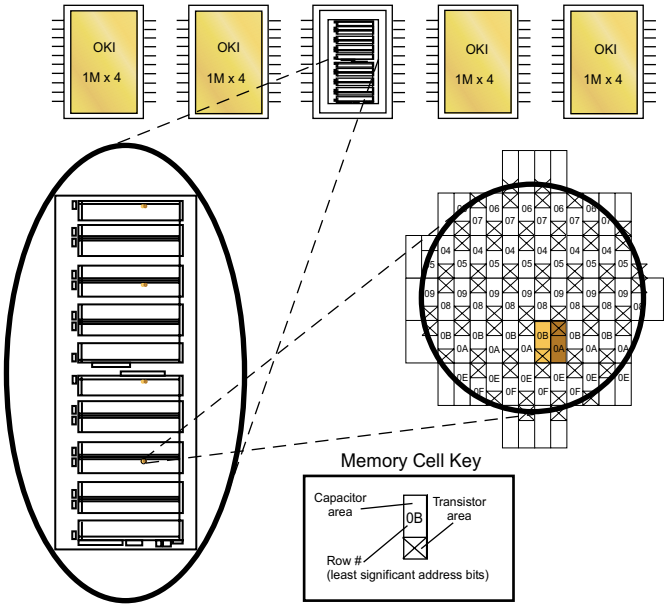

Fig. 6. A 39-bit EDAC word is assembled from two reads (of four bits) from five devices. As illustrated in the die footprint blowups, the first read retrieves four widely space bits within a given device as does the second read. Unfortunately, the widely spaced bits of the second read are adjacent to the widely spaced bits of the first, resulting in 19 pairs of adjacent bits in an EDAC word. Note that the fortieth bit is not used, explaining why there are not 20 pairs.

the physically adjacent bits within the DRAM were mapped by address from tests with Cf^{252} fission fragments. A similar approach has been used by Buchner, et al. using a pulsed laser [7], but it is sometimes impossible to use a laser with DRAMs because of the extensive coverage of the DRAM chip with metal. The Cf^{252} mapping procedure is based on the ability of fission fragments to cause small size MBUs. By irradiating with a low flux so that only one or fewer events is expected for each scan through the device, one is able to deduce that detected upsets are likely physical neighbors. It doesn't require very many events before patterns become

clear, and, at any rate, a long experiment is economical because it can run unattended and incurs no accelerator charges. The full physical-to-logical mapping was eventually obtained from the manufacturer and confirmed that the correct mapping of physically-adjacent logical addresses was obtained. This information is incorporated in Fig. 6 (and also Fig. 7).

B. MBU Characterization of DRAMs

In order to investigate this anomaly, additional tests were done on individual DRAMs from the flight lot. Following the work of Zoutendyk [8], emphasis was place on investigating multiple-bit upsets or MBUs. Devices were irradiated at a very low flux and scanned at a rapid rate, so that raw data on single-event multiple-bit upsets could be obtained. The all-bits-upsettable data pattern was used.

Initial investigations were done at JPL using Cf^{252} fission fragments. An example run had 161 single errors, 63 doubles, 56 triples, and 5 quadruples; the quadruple errors are illustrated against the device physical layout in Fig. 7. It is interesting that the fragments, although their range is quite small, cause almost as many multiple-bit upsets as single errors.

This information was examined in order to count the number of multiples which spanned an even address and the next address, as these would be double errors in a single EDAC word and thus uncorrectable. All the rest of the upsets, including those spanning odd addresses and the next one, were added to the single-bit error tally. The process is illustrated in Fig. 7 for the quadruple errors, with lighter shading for the eight upset bits in the clusters that are in separate EDAC words, and darker shading for pairs causing uncorrectable errors within an EDAC word. Thus, the five four-bit MBUs in this sample corrupted six EDAC words while leaving single, correctable errors in eight others. Also, in the final tally 32 of the 63 doubles spanned different words, while only seven of the 56 triples did not cause uncorrectable EDAC words. The result is that there are 86 EDAC words with uncorrectable (pairs) of errors and 231 correctable errors, or a ratio of 37%.

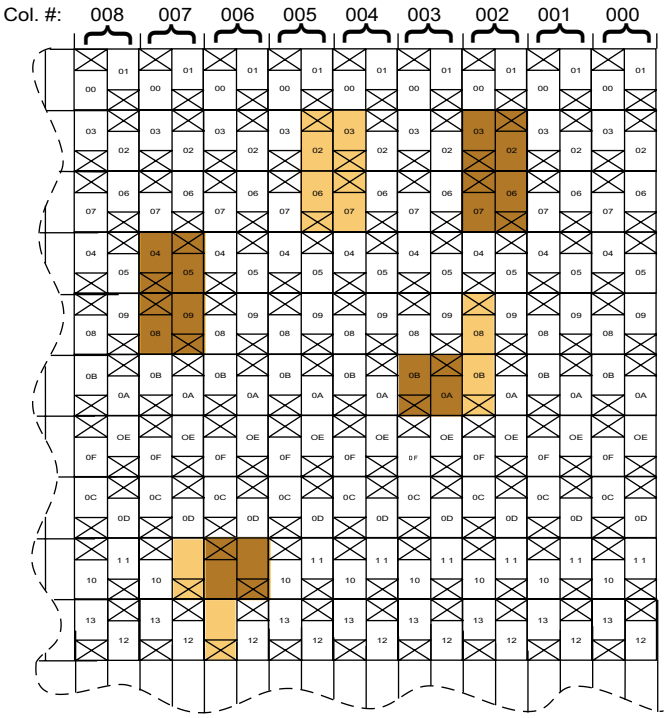

Fig. 7. A small segment of the DRAM physical layout overlayed with the five clusters of four-bit MBUs drawn roughly to scale. Note each cell consists of an access transistor (represented by X's) and, occupying about twice the area of the transistor, a capacitor (designated by row number, see key in Fig. 6). The six horizontal pairs of darker shaded cells are inside EDAC words.

Accelerated heavy-ion MBU testing was conducted at the Brookhaven SEE Test Facility. The data set collected was analyzed using the OKI logical-to-physical map to count the physically clustered groups to obtain the number of events. MBUs cause the ratio of upsets-to-events to be greater than one. The results, presented in Fig. 8, show a complex dependence on the ion used and its angle of incidence. However, in general, the average MBU size increases with increasing effective LET as shown in Fig. 9.

The results of the EDAC analysis of the heavy-ion data are shown in Fig. 10 as a function of LET, and the observed ratio of 0.7% is also noted. This figure shows that the expected number of multiple-bit errors increases rapidly with increasing LET. Therefore, the architectural flaw of not assembling EDAC words from widely separated bits along with the device sensitivity to MBUs explains the anomalously high number of in-flight uncorrectable errors. This explanation requires that most upsets occurring in flight are from low LET ions and protons, which is consistent with a cosmic ray background environment.

Tests were also conducted at the Indiana University Cyclotron Facility to determine the device susceptibility to proton-induced MBUs. The results are summarized in the Table II, again accounting for the way the EDAC words are assembled. In addition to being important for the flares that Cassini is expected to encounter, these results are particularly important to AXAF, which is flying the Cassini spare recorders, also without fixing the EDAC architectural flaw. AXAF orbits the earth, regularly encountering the south Atlantic anomaly.

Confirmation that the EDAC architecture's handling of MBUs is causing the unexpectedly high rate of uncorrectable errors has been found by the Cassini ground operations team. A small portion of the SSR (6.25%) is used to store flight software. Data was retrieved from the spacecraft which con-

TABLE II.
PROTON RESULTS FOR 4MB OKI DRAM
FROM INDIANA UNIVERSITY CYCLOTRON FACILITY

Proton Energy (MeV)	Upsets-to-Events	EDAC Errors-to-Correctable (%)
50	1.032	1.5
99	--	2.6
106	1.063	2.9
153	1.094	4.5
192	1.101	4.5

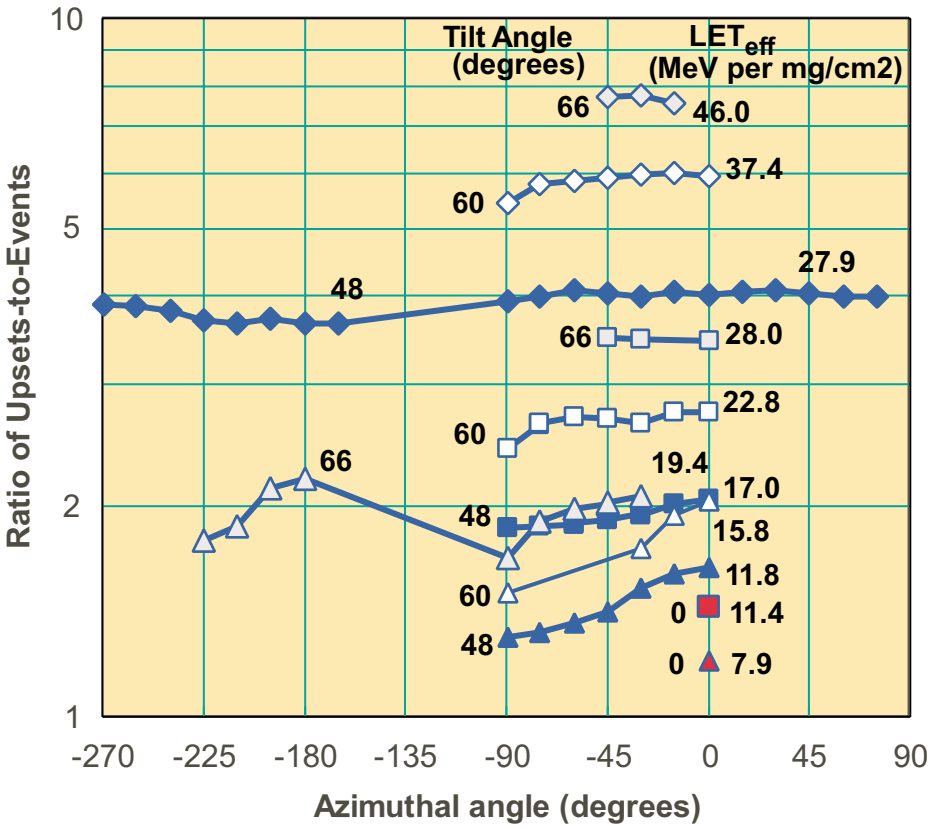

Fig. 8. Multiple-bit upset characterization data for three heavy ions: triangles are 186 MeV Si, squares are 210 MeV Cl, diamonds are 229 MeV Ti.

tained the first six uncorrectable errors that appeared in the flight software. The erroneous bits were paired just as shown in Fig. 6.

V. DISCUSSION

The results in this paper show that although DRAMs are very sensitive to single-event upset, they are still viable choices for space designs that include properly designed EDAC to eliminate single-bit errors. More advanced error correction can also be used to correct for double errors (or even higher numbers of bit errors) at the expense of additional check bits for the same amount of data.

In the case of Cassini, an oversight in the physical distribution of bits within a single word caused the uncorrectable multiple-bit upset rate to be orders of magnitude higher than it should be. It is noted that because the design could have easily fixed the problem by swapping the least significant address line with any other.

Fortunately, the uncorrectable error rate seen so far in the Cassini recorders is so low that it is merely a nuisance. This is mainly due to the fact that a large solar flare has not been encountered so far. Now that the spacecraft is past the Earth and headed toward Saturn, the danger is lessening because the intensity of a given flare falls off with distance from the sun. Further, extra shielding was placed around the DRAM cards to reduce the number of protons and low energy ions. The weak solar flare seen in the first month after launch suggests that only a few multiple-bit errors occur when low-energy protons strike the DRAMs. However, the passage through the trapped particle belts at Saturn three years hence should prove interesting.

One lesson from this experience is that the architecture of DRAM-based designs must be scrutinized carefully if unpleasant surprises are to be avoided. A similar experience with IBM DRAMs on the Hubble Space Telescope [9] reinforces this conclusion. In hindsight, the architectural flaw could have been caught by either a complete understanding of the logical-physical bit map or by ground testing that included the EDAC design. If mapping data are not available, then it

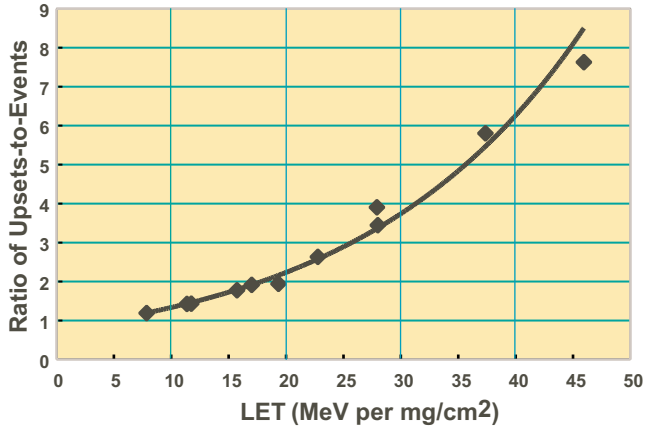

Fig. 9. The ratio of upsets-to-events averaged over azimuthal angle as a function of LET (from the same data set as Fig. 8).

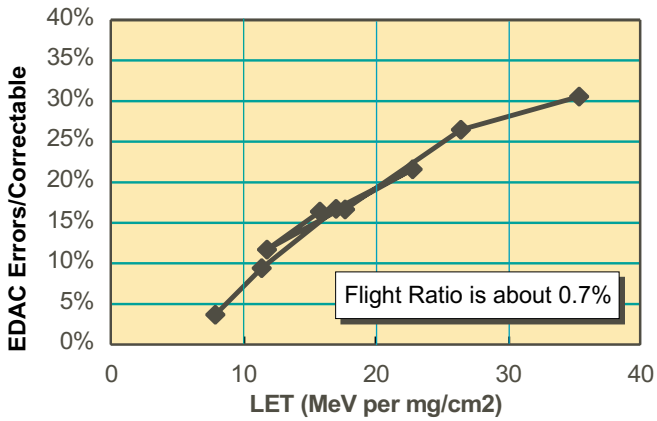

Fig. 10. Ratio of uncorrectable to correctable errors for three heavy ions (Si: LET$_0$=7.9, Cl: LET$_0$=11.4, Ti: LET$_0$=17.7) at three angles (normal, 48, and 60 degrees). Note that the azimuthal angle dependence has been ignored but, if included, would tend to lower the points.

can be developed from laser or Californium testing.

Another important result of this work is that MBUs are more prevalent (at least for DRAMs) than previously suspected. Even protons are capable of causing many MBUs. As DRAMs scale the average size of MBUs will likely increase [10]. More study is needed to correctly model the charge collection that is causing MBUs in DRAMs. Also, more characterization of the complex azimuthal angle dependence hinted at here is needed. The charge collection understanding needs to be able to explain observed angle dependencies.

VI. ACKNOWLEDGEMENTS

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